

AT21CS01 Silicon Errata

The AT21CS01 devices that you have received conform functionally to the current Device Data Sheet (DS20005857B), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for devices listed in [Table 1](#). The silicon issues are summarized in [Table 2](#).

The errata described in this document will be addressed in future revisions of the AT21CS01 silicon.

TABLE 1: AFFECTED PART NUMBERS

| Part Number |
|-------------|
| AT21CS01 |

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of [Table 2](#) apply to the current silicon revision (C0).

TABLE 2: SILICON ISSUE SUMMARY

| Issue Number | Issue Summary | Affected Revision ⁽¹⁾ | | |
|--------------|--|----------------------------------|----|----|
| | | A0 | B0 | C0 |
| 1 | Reset and Discovery Failure with Multiple Devices on Bus | X | X | |

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**C0**).

1. Issue: Reset and Discovery Failure with Multiple Devices on Bus

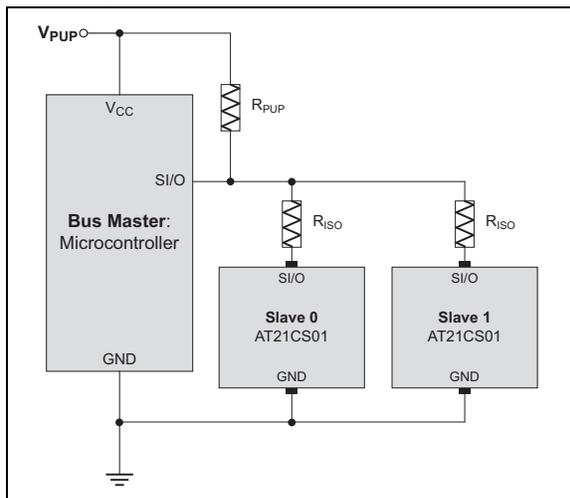
When multiple AT21CS01 devices are present on the single-wire bus, one or more devices may not reset properly after a device Reset or power-up event.

The device(s) that are not reset properly may remain active (driving S/I/O low) following the device Reset or power-up event, resulting in corrupted communication.

Work around

Modify the firmware to force S/I/O high during the entire t_{DACK} period following a device Reset or power-up event. Series resistors must be added to isolate the slave devices and reduce the output current. In addition, narrowing the Pull-Up Voltage V_{PUP} range may be necessary to meet timing and I/O level requirements during communication. [Figure 1](#) is an example Schematic with the isolation resistors R_{ISO} .

FIGURE 1: EXAMPLE SCHEMATIC



Affected Silicon Revisions

| A0 | B0 | C0 |
|----|----|----|
| X | X | |

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (04/2019)

Initial release of this document.

NOTES:

Note the following details of the code protection feature on Microchip devices:

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