MLPF-WB-02D3



Datasheet

2.4 GHz low pass filter matched to STM32WB5x and STM32WB1x in WLCSP and UFBGA packages



Features

- Integrated impedance matching to STM32WB5x and STM32WB1x in WLCSP and UFBGA packages
- 50 Ω nominal impedance on antenna side
- Deep rejection harmonics filter
- Low insertion loss
- Small footprint
- Low profile ≤ 630 µm after reflow
- High RF performances
- RF BOM and area reduction
- ECOPACK2 compliant component

Applications

- Bluetooth 5
- OpenThread
- Zigbee®
- IEEE 802.15.4
- Optimized for STM32WB5x and STM32WB1x in WLCSP and UFBGA packages

Product status lin	k
MLPF-WB-02D3	

Chip scale package on glass 6 bumps

Pin-out top diagram (top view - bumps down)

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GND4

GND3

GND2

GND1

Description

The MLPF-WB-02D3 integrates an impedance matching network and harmonics filter. The matching impedance network has been tailored to maximize the RF performances of STM32WB5x and STM32WB1x in WLCSP and UFBGA packages. This device uses STMicroelectronics IPD technology on non-conductive glass substrate which optimizes RF performances.



1 Characteristics

Table 1. Absolute ratings (T_{amb} = 25 °C)

Symbol	Parameter	Value	Unit
P _{IN}	Input power RF _{IN}	10	dBm
V _{ESD}	ESD ratings human body model (JESD22-A114-C), all I/O one at a time while others connected to GND	2000	V
T _{OP}	Maximum operating temperature	-40 to +105	°C

Table 2. Impedances (T_{amb} = 25 °C)

Symbol	Symbol Parameter		Value				
Symbol	Falameter	Min.	Тур.	Max.	Unit		
Z _{IN}	STM32WBxx single-ended impedance	-	Matched to STM32WB5x and STM32WB1x in WLCSP and UFBGA packages	-	Ω		
Z _{OUT}	Antenna impedance	-	50	-	Ω		

Table 3. Electrical characteristics and RF performances (T_{amb} = 25 °C)

Symbol	Der	Parameter -		Value		11
Symbol	Parameter		Min.	Тур.	Max.	Unit
f	Frequency range		2400		2500	MHz
IL	Insertion loss IS ₂₁ I			1.0	1.2	dB
RL _{IN}	Input return loss IS ₁₁		15	19		dB
RL _{OUT}	Output return loss IS2	2 ¹	16	23		dB
		Attenuation at 2fo (4800 – 5000) MHz	46	47		dB
A#	Harmonic rejection	Attenuation at 3fo (7200 – 7500) MHz	50	54		dB
Att levels IS ₂₁	levels IS ₂₁ I	Attenuation at 4fo (9600 – 10000) MHz	45	61		dB
		Attenuation at 5fo (12000 – 12500) MHz	38	45		dB



1.1 RF measurement









Figure 6. Attenuation 3f0 (dB)









		Figure	8. Atte	enuatio	on 5f0 (dB)	
-30—	S21, dB						
-35—							
-40—							
-45—							
-50—							
-55—							
-60—							
-65—							
-70—							
-75—							f(GHz)
-80— 1	2.0	12.1	12.2		12.3	12.4	1

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2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

2.1 CSPG package information



Figure 9. CSPG package outline (bottom view - bumps up)

Table 4. CSPG 6 bumps mechanical data

	Dimensions							
Ref.	Millimeters							
	Min.	Тур.	Max.					
A	0.580	0.630	0.680					
A1	0.180	0.205	0.230					
A2	0.380	0.400	0.420					
b	0.230	0.255	0.280					
D	1.550	1.600	1.650					
D1		0.577						
D2		0.577						
E	0.950	1.000	1.050					
E1		0.500						
fD1		0.223						
fD2		0.223						
fE1	E1 0.250							
fE2		0.250						



Figure 11. Top view



В А 1 Dot, ST logo ĠŇD3 ÌÙÚŤ ECOPACK[®] Grade **5** G xx = marking z = manufacturing location 2 yww = datecode ΧZ (y = year ww = week) GND2 GND4 ww 3 GND1 ÌŇ

Table 5. Pad description top view (pads down)

Pad ref	Pad name	Description
A1	OUT	Antenna
A2	GND4	Ground
A3	IN	STM32WB5x and STM32WB1x out
B1	GND3	Ground
B2	GND2	Ground
В3	GND1	Ground

Figure 12. Tape and reel outline



Table 6. Tape and reel mechanical data

	Dimensions						
Ref	Millimeters						
	Min	Тур	Мах				
A0	1.06	1.09	1.12				
B0	1.66	1.69	1.72				
D0	1.40	1.50	1.60				
F	3.45	3.50	3.55				
К0	0.69	0.72	0.75				
P0	3.90	4.00	4.10				
P1	1.95	2.00	2.05				
P2	1.95	2.00	2.05				
W	7.90	8.00	8.30				

3 Recommendation on PCB assembly

3.1 Land pattern

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Layout example using STM32WB15CCY.



Transmission line between MLPF and antenna is dimensioned to 50 ohms characteristic impedance. Transmission line between STM32 and MLPF is dimensioned to 61 ohms characteristic impedance. Theses transmission line characteristics impedances have to be followed as close as possible. Moreover, lines physical dimensions will have to be tuned according to specific PCB stack up if different from the one presented in datasheet to keep expected characteristic impedance values.

#	Name	Material		Туре	Weight	Thickness	Dk
	Top Overlay			Overlay			
	Top Solder	Solder Resist		Solder Mask		0.03mm	3.6
1	L1		-	Signal	1/3oz	0.012mm	
	Dielectric 1	1 x 1080				0.065mm	3.5
2	L2				1/3oz	0.012mm	
	Dielectric 2	1 x 2113				0.08mm	3.6
з	L3		-	Signal	1/2oz	0.0175mm	
	Dielectric 3	FR4		Core		1.2mm	4.9
4	L4			Signal	1/2oz	0.0175mm	
	Dielectric 4	1 x 2113				0.08mm	3.6
5	L5			Signal	1/3oz	0.012mm	
	Dielectric 5	1 x 1080				0.065mm	3.5
6	L6			Signal	1/3oz	0.012mm	
	Bottom Solder	Solder Resist		Solder Mask		0.03mm	3.6
	Bottom Overlay			Overlay			

Figure 14. PCB stack-up recommendations



3.2 Stencil opening design



3.3 Solder paste

- 1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
- 2. "No clean" solder paste is recommended.
- 3. Offers a high tack force to resist component movement during high speed.
- 4. Use solder paste with fine particles: powder particle size 20-38 µm.

3.4 Placement

- 1. Manual positioning is not recommended.
- 2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
- 3. Standard tolerance of ±0.05 mm is recommended.
- 4. 1.0 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
- 5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
- 6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

3.5 PCB design preference

- 1. To control the solder paste amount, the closed via is recommended instead of open vias.
- 2. The position of tracks and open vias in the solder area should be well balanced. A symmetrical layout is recommended, to avoid any tilt phenomena caused by asymmetrical solder paste due to solder flow away.

3.6 Reflow profile

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Note: Note: Minimize air convection currents in the reflow oven to avoid component movement.

More information is available in the application note:

AN2348 Flip-Chip: "Package description and recommendations for use"



4 Ordering information

Table 7. Ordering information

Order code	Marking	Package	Weight	Base qty.	Delivery mode
MLPF-WB-02D3	ТХ	CSPG	1.82 mg	5000	Tape and reel

Revision history

Table 8. Document revision history

Date	Revision	Changes	
29-Jul-2022	1	Initial release.	
25-Nov-2022	2	Updated Section 3.1 Land pattern.	

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