

NAVIGATE THE AFE AND DATA-CONVERTER MAZE IN MOBILE WIRELESS TERMINALS

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Abstract: High-speed and low-speed data converters serve critical functions in modern broadband mobile radios. This application note outlines how to determine high-speed data converter performance requirements in baseband sampling radio architectures. Also, system partition strategies and advantages are outlined when considering a high-speed analog front-end (AFE) solution.



[Click here for an overview of the wireless components used in a typical radio transceiver.](#)

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Introduction

Mobile broadband wireless communication systems employ several techniques for improving spectral efficiency. To achieve high data rates, yield optimal system capacity, and ensure reliable quality of service (QoS), modern wireless communication systems use variable channel bandwidths ($BW = 1.25\text{MHz}$ to 20MHz) with high-order modulation (16QAM to 64QAM) and code-division or orthogonal frequency-division multiple access (CDMA, OFDMA) as well as scalable, smart antenna technology (e.g., multiple-input multiple-output or MIMO, spatial diversity).

3GPP standards UMTS, TD-SCDMA, and long-term evolution (LTE) as well as others like IEEE[®] 802.16e, IEEE 802.11n, and IEEE 802.11ac are some common systems that use these techniques. As an example, a 4G LTE radio can achieve a peak data rate greater than 100Mbps with robust performance using 64QAM modulation, orthogonal frequency-division multiplexing (OFDM) with 2048 subcarriers, a 20MHz channel bandwidth, and a 2x2 MIMO architecture.

High-order modulation with OFDM, wide-channel bandwidths, and MIMO architectures all conspire to demand higher performance from the receive analog-to-digital converter (Rx ADC) and the transmit digital-to-analog converter (Tx DAC). The high-speed data converter requirements include faster sample rate, higher dynamic range, improved spectral performance, and multiple channels. Furthermore, since the end-product communication equipment is mobile and battery-powered, the data converters must be low power and miniature in size. These factors present a maze of design challenges when selecting the right high-speed data converter solution. The following topics present a methodology to help designers navigate these challenges.

Radio and Data Converter Functions

Small size, low power, and low cost are important design goals in mobile wireless products like smartphones, data cards, embedded radios, public safety radios, tactical military radios, or mobile satellite radios. Because of this, a direct-conversion zero intermediate frequency (ZIF) architecture is a common radio solution. Compared to heterodyne radios, the ZIF architecture eliminates multiple intermediate frequency components such as IF mixer, VGA, LO synthesizer, and image reject filter. This elimination lowers cost and reduces size. Furthermore, in applications with variable channel bandwidths, like LTE, the ZIF architecture lends itself to programmable baseband filtering.

Figure 1 illustrates the radio lineup used in a typical mobile application. The radio architecture, a ZIF receiver and quasi-direct conversion transmitter, requires a dual-channel high-speed Rx ADC and a dual-channel high-speed Tx DAC for in-phase and quadrature-phase (I/Q) baseband signal sampling and construction. Other low-speed converters are used for RF front-end gain control and ancillary analog signal measurements like RF power amplifier temperature and transmitter RF power level. The converter's digital bus interfaces with a digital baseband processor in the form of a field-programmable gate array (FPGA), a digital signal processor (DSP), or an application-specific integrated circuit (ASIC). The digital baseband processor performs signal-processing functions like channel coding, modulation mapping, and digital filtering. As shown in Figure 1 a single-mode radio might require up to eight data converter channels.

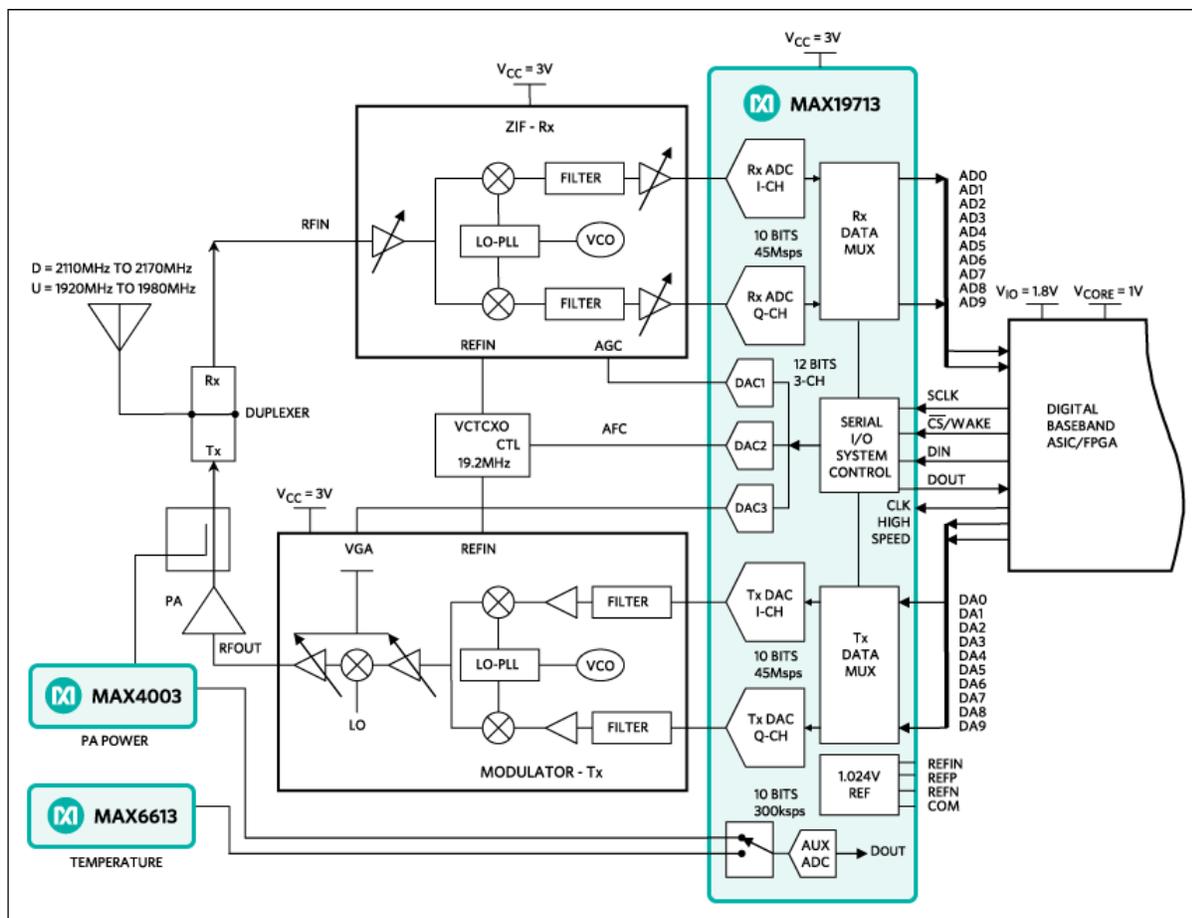


Figure 1. Typical ZIF radios are based on a highly integrated analog front-end chip.

Enter the High-Speed Analog Front-End (AFE)

As shown in Figure 1, there is a 4:1 ratio between high-speed converter channels and a radio transceiver. For every radio transceiver added, the data converter density increases by four. The dramatic 4:1 relationship between data converters and radios can be seen in a 4x4 MIMO design, where four radio transceivers are needed with 16 high-speed data converter channels. This makes the data converter function an important area where dense analog integration can help shrink size, lower cost, and reduce power—all critical for mobile radio designs.

High-speed and low-speed data converters can be combined into a single device to meet size, cost, and power targets for mobile products. A high-speed AFE could function as an integrated converter solution. One such AFE is the MAX19713, shown in Figure 2. The AFE integrates all data converters needed to interface with a radio front-end.

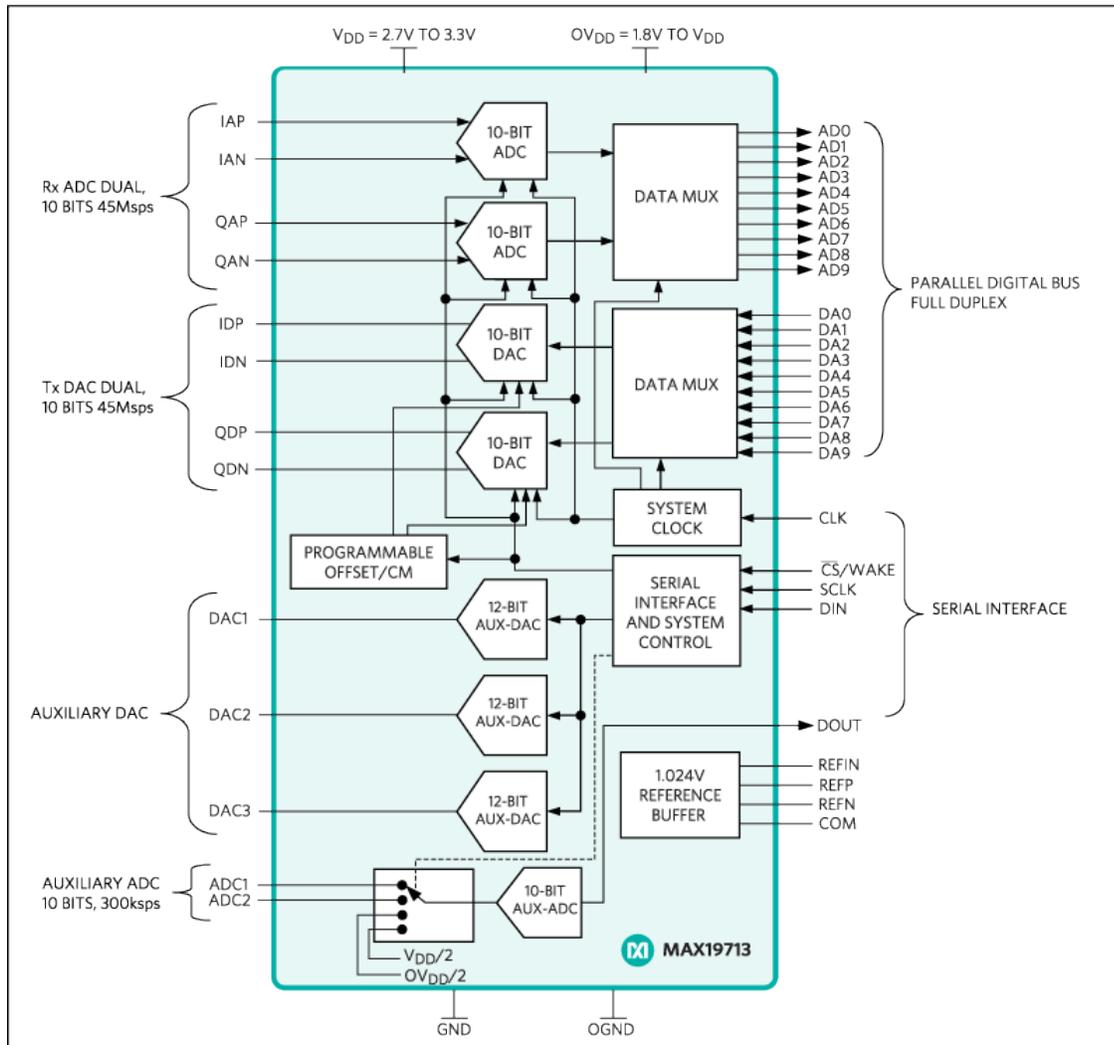


Figure 2. The MAX19713 high-speed AFE block diagram.

A high-speed AFE has applications in multimode designs. One example is a dual-mode radio that supports UMTS with Wi-Fi®- or MIMO-based designs, such as LTE, WiMAX®, and IEEE 802.11n/ac, which require multiple radios and multiple converter channels. The 4:1 relationship between radio data converters and RF transceivers makes the AFE an attractive solution for FPGA-based and DSP-based designs.

Because stand-alone DSPs and FPGAs often are pure digital devices, they do not integrate mixed-signal data converter functionality. A high-speed AFE fulfills the data converter requirements and ideally does the job at low power with a small footprint. Another advantage to the AFE partition is scalability. As a given design scales from 1×1 single-input single-output (SISO) to 2×2 MIMO or 4×4 MIMO, the AFE can be bolted on as needed. This offloads the digital baseband modem from having to integrate multiple AFE configurations to support different MIMO radio scenarios. Moving the converters out of the digital baseband optimizes the modem die size, lowers test cost, and reduces silicon cost. Because of this, a stand-alone AFE partition provides design flexibility and scalability. However, fully understanding the system requirements is a key factor in executing a successful AFE partition.

When selecting a high-speed AFE for wireless communications systems, the target air-interface channel bandwidth, modulation order, and desired symbol error rate (SER) must be known. All data converter functions as related to the radio front-end must be identified. The converter cost and power targets must be established. And the converter dynamic performance requirements and trade-offs must be understood.

Understanding the high-speed converter performance requirements is critical for several reasons. Primarily, the converter's dynamic performance establishes the radio's performance level. The Rx ADC and Tx DAC must faithfully digitize and synthesize receiver and transmitter signals without degrading system signal-to-noise ratio (SNR) and SER. Furthermore, over specifying the converters will result in a larger die size that yields a higher-power and higher-cost solution. Also, to minimize system size and reduce total cost, the analog and digital physical interfaces must work seamlessly with the respective radio front-end and digital baseband processor. A seamless physical interface eliminates external discrete devices needed for level shifting, gain setting, and offset adjustments.

System requirements for modulation order, desired SER, undesired high interference levels, spurious emission levels, and access coding determine the Rx ADC and Tx DAC dynamic specifications. Signals that use high-order modulation require more quantization levels. Channel bandwidth determines the converter sample rate. The signal peak-to-average power ratio (PAPR) dictates dynamic range, and system spurious emission limits determine output spectral purity.

In mobile wireless terminals, the resolution of the Rx ADC or Tx DAC can range from 4 bits used in quadrature phase-shift keying (QPSK) to 12 or 14 bits used in 256QAM, and the conversion rate can vary from 2.5MSPS to 80MSPS for 1.25MHz to 40MHz channel bandwidths.

High-Speed Converter Sample Rate

The Nyquist criterion dictates that converter sampling frequency must be at least twice the highest frequency component of interest or information will be lost. For example, in an 802.11g wireless local-area network (WLAN) radio, the channel bandwidth is 16.25MHz. At baseband, the I/Q frequency components are each 8.125MHz. So theoretically, the Rx ADC and Tx DAC must sample at least 16.25Mps (FCLK = 16.25MHz).

This sample rate requires a “brick wall” (i.e., high order) filter that attenuates out-of-band frequency components to prevent aliasing by the Rx ADC or spurious emissions in the DAC transmit path. When the sample rate is increased by four or eight times, the baseband I/Q filter order requirement can be relaxed because alias and image frequencies are moved beyond the first Nyquist region.

Also, attenuation due to the Tx DAC $\sin(x)/x$ response can be minimized by increasing FCLK. The normalized Tx DAC output amplitude is given by the following equation:

$$A_{OUT} = \sin(\pi f_{OUT}/f_C) \times (\pi f_{OUT}/f_C)^{-1}$$

f_{OUT} = output frequency
 f_C = clock frequency

The normalized output amplitude equation shows that for $f_{OUT} = FCLK/8$, the $\sin(x)/x$ attenuation is reduced to 0.22dB. Process gain is an added benefit to oversampling since the converter SNR improves by 3dB with a twofold increase in FCLK.

As air-interface channel bandwidths increase, the data converter sample rate must increase. A minimum 2x oversampling rate is desirable to reduce baseband filter requirements, improve SNR, and minimize $\sin(x)/x$ effects. To address 4G variable channel bandwidths covering 1.4MHz up to 20MHz, the high-speed data converter should be at a minimum 2x oversampling rate, ranging from 2.8Mps to 40Mps.

Rx ADC: How Many Bits?

The Rx ADC dynamic-performance requirements can be calculated using the example Rx ADC SNR budget analysis in **Figure 3**. The analysis determines the required Rx ADC dynamic range for reliable signal recovery. In baseband sampling applications, the important ADC parameter is signal-to-noise and distortion (SINAD), which translates to effective number of bits (ENOB). Dynamic performance represented as ENOB, not absolute resolution in bits, is the key parameter. ENOB and SINAD are related by the following equation:

$$SINAD = 6.02n + 1.76dB + 10\log_{10}(f_S/(2 \times BW))$$

n = effective number of bits
 f_S = sampling frequency
 BW = signal bandwidth

PROCESS GAIN

The SINAD parameter accounts for noise and distortion within the Nyquist band and for process gain due to oversampling. RF front-end sensitivity, noise figure, and filtering are selected to meet the baseband demodulation signal-processing requirement for a desired SER. It is the primary job of the Rx ADC to quantize the ZIF receiver’s analog I/Q output signals without significantly degrading SNR. Furthermore, the Rx ADC cannot introduce distortion that inhibits reliable signal recovery.

The analysis in Figure 3 uses 64QAM modulation with OFDM, channel bandwidth = 5MHz, and 1e-5 SER and accounts for ADC SNR degradation, ADC gain/offset errors, and RF front-end automatic gain control (AGC) error. The analysis is applicable to any air interface standard, including LTE, high-speed packet access (HSPA), and 802.11a/b/g/n/ac.

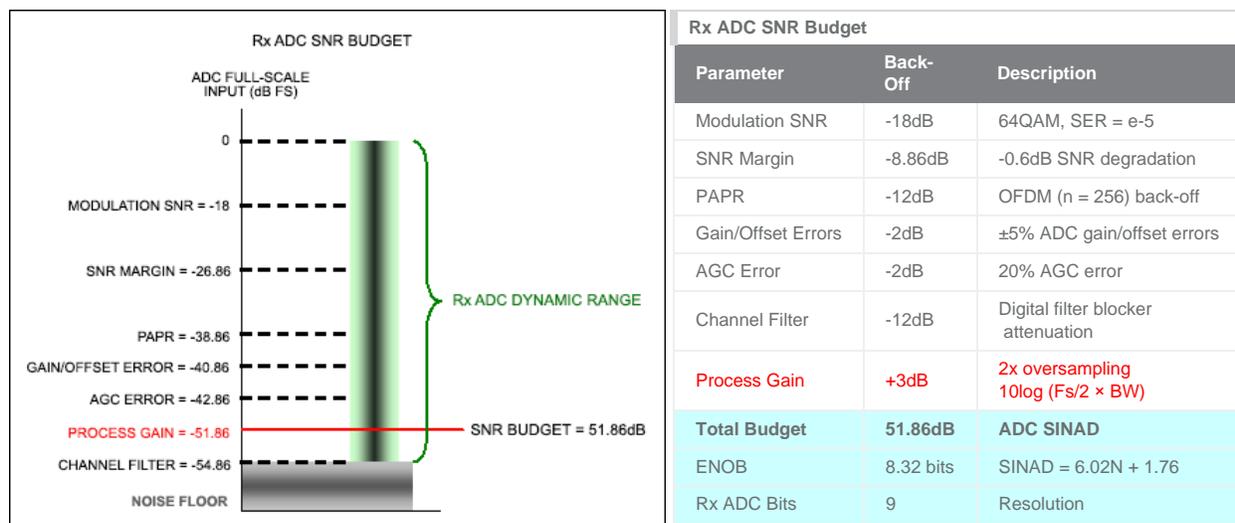


Figure 3. The RX ADC SNR budget shows how different system aspects contribute to the total dynamic range requirement.

The Rx ADC SNR budget involves several factors:

- **Modulation SNR:** For 64QAM modulation with SER = 1e-5, the digital demodulator requires 18dB SNR. This is based on known symbol error probability theory (Figure 4).
- **SNR margin:** Since an ADC has internal noise sources, it does not behave like an ideal quantizer. The ADC inherently adds noise and distortion to

the input signal. The design objective is to select an ADC with noise and distortion at an acceptable level that meets the digital demodulator SNR requirements. Typically, a good figure of merit is 0.6dB degradation. This means that the ADC will not degrade the input SNR by more than 0.6dB. Therefore, the ADC must have 8.86dB better SNR than the input signal SNR level. In other words, if the input signal has an 18.6dB SNR, to achieve an SNR of 18dB, the ADC needs 26.89dB SNR to prevent degrading the input by more than 0.6dB. The following equation calculates system SNR:

$$\text{System SNR} = -20\log(10^{-\text{SNRa}/10} + 10^{-\text{SNRb}/10} + \dots + 10^{-\text{SNRn}/10})^{1/2}$$

- **PAPR:** For 2^n -carrier (subcarriers = 256, 512, 2048) OFDM signaling, the PAPR is 8dB to 12dB. This means the ADC input must be backed off by 12dB to prevent clipping during peaks. ADC clipping should be avoided since it creates distortion that degrades SER performance.
- **Gain/offset errors:** The major contributor to gain error for an ADC is the internal voltage reference. The internal reference can have $\pm 5\%$ tolerance over temperature. Offset is residual from the internal ADC amplifier voltage offsets. Gain and offset errors are important considerations in the ADC error budget because they reduce the usable dynamic range. If the gain error and offset errors are each 10% of full scale, then each contributes a 1dB reduction in dynamic range. Because of this error, the ADC must be backed off 1dB to prevent input clipping and another 1dB to account for limited dynamic range. Using the internal ADC voltage reference saves cost and size, and it eliminates an extra component in inventory. A reasonable cost-size trade-off is to use a high-speed AFE with an integrated reference and to add 2dB dynamic range margin.
- **AGC error:** A typical ZIF receiver integrates AGC to set baseband analog I/Q output voltage signal levels. The AGC level can have a 20% ($\pm 10\%$) accuracy error due to variations over process, temperature, and supply voltage. This translates to an error of 2dB in the AGC. To maintain the desired SNR level and PAPR back-off at the Rx ADC input, the AGC error should be considered in an SNR budget analysis. For example, if the actual AGC setting is 2dB lower from the expected setting, then SNR will be 2dB lower.
- **Channel filter:** There are circumstances where the RF receiver cannot sufficiently filter undesirable adjacent-channel interferers. In such a case, the Rx ADC must have adequate dynamic range to handle the blocker signal level and the desired signal while maintaining the required SINAD for digital demodulation of the desired signal. Additional dynamic range is used to digitally filter the undesired interferer. Or, to lower cost and die size, the baseband analog filter order can be reduced and additional filtering can be done digitally. A dB-for-dB relationship exists between the analog and digital filter order, so a 6dB reduction in analog filtering must be made up by boosting the Rx ADC's dynamic range by 6dB. For this example, 12dB blocker attenuation is assumed.
- **Process gain:** Assume that the Rx ADC is 2x oversampling the baseband analog I/Q signal. Since the baseband signal is $BW = 2.5\text{MHz}$ and $F_{CLK} = 10\text{MHz}$, the resulting process gain is 3dB. The process gain improves SNR by 3dB, which can be subtracted from the required Rx ADC SNR.

The above analysis concludes that an Rx ADC with SINAD = 51.86dB at $F_{CLK} = 10\text{Mps}$ ensures digital demodulator signal recovery of a 5MHz, 64QAM OFDM signal at $SER = 1e-5$.

Note on Rx ADC dynamic range: It is important to look closely at the Electrical Characteristics table in an Rx ADC data sheet for the specified SINAD and input full-scale level. To take advantage of the full Rx ADC dynamic range, the RX ADC input full-scale level should closely match the ZIF receiver's analog I/Q output signal level. For instance, assume that the Rx ADC full-scale input is $2V_{p,p}$ with SINAD specified at 50dB. Now assume that the ZIF receiver's maximum full-scale output is $1V_{p,p}$. This means that the Rx ADC is effectively backed off by 6dB, which results in a 6dB reduction in SINAD for $A_{IN} = 1V_{p,p}$. As a result, the achievable SINAD is 44dB at $A_{IN} = 1V_{p,p}$. Conversely, if the Rx ADC were designed with a full-scale input of $A_{IN} = 1V_{p,p}$ and specified SINAD = 50dB, then the full 50dB dynamic range could be used.

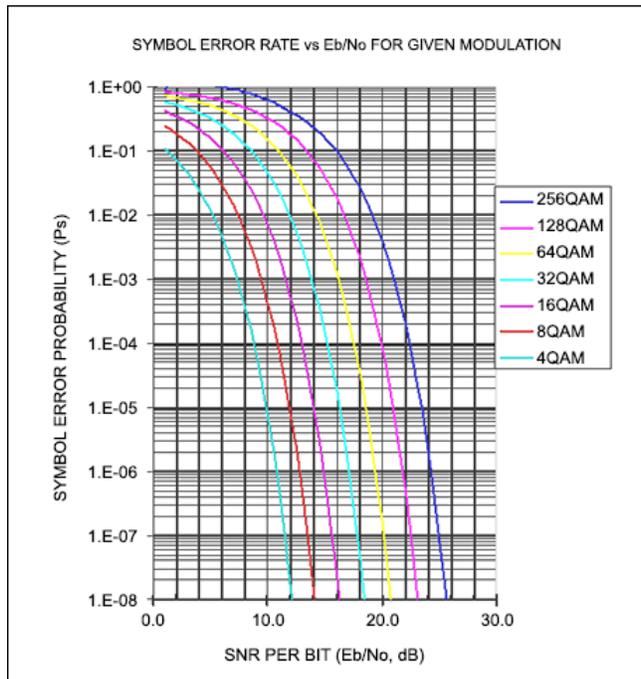


Figure 4. This graph shows the required SNR for a given symbol error probability and different orders of modulation.

Tx DAC: How Many Bits?

The Tx DAC dynamic-performance requirements can be calculated using the example Tx DAC SNR budget analysis in Figure 5. The analysis is based on the error vector magnitude (EVM) specification for a ZIF transmitter lineup. EVM is a modulation quality metric used in many air interface standards

(3G, 4G, and 802.11) and is defined as the ratio of RMS constellation error magnitude to peak constellation symbol magnitude. Expressed as a percentage, it is a measure of total transmitter performance, including impairments such as gain/phase errors, symbol error, and in-channel spurious emissions. EVM is related to SNR by the following equation, and thereby can be related to SER:

$$\text{SNR} = -20\log(\text{EVM}/100\%)$$

The performance budget analysis in Figure 5 uses 16QAM modulation with OFDMA, 1e-6 SER, channel bandwidth = 8.75MHz, and allowances for Tx DAC degradation, DAC gain/offset errors, and PAPR. The analysis uses the WiBro[®] air interface standard as an example but is applicable to any wireless broadband standard.

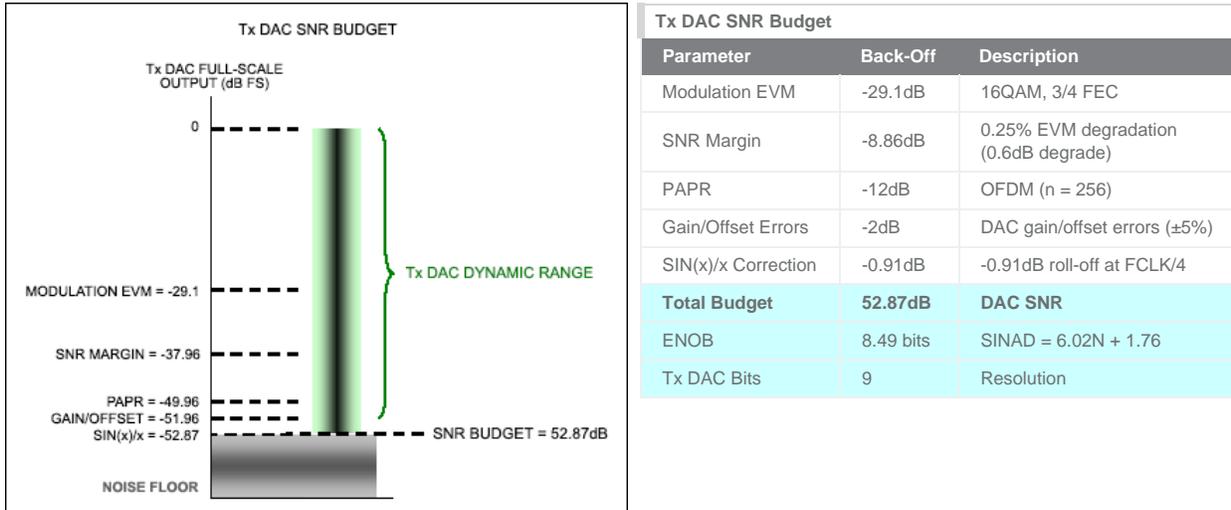


Figure 5. The Tx DAC SNR budget includes many factors that contribute to the overall dynamic range. Using this method, designers can determine the required TX DAC ENOB.

The Tx DAC SNR budget involves several factors:

- Modulation EVM:** A given air-interface reference design, such as WiBro, that uses the MAX2837 RF transceiver provides a 3.5% transmit EVM for 16QAM and a 3/4 forward error correction (3/4-FEC) coded signal with POUT = 23dBm. The EVM specification is antenna-referenced and includes RF modulator and power amplifier (PA) impairments. The 3.5% EVM performance translates to -29.1dB SNR.
- SNR margin:** Assume that the Tx DAC cannot degrade system SNR by more than 0.6dB, which translates to a Tx EVM degradation of 0.25%. Overall, Tx EVM, including the Tx DAC contribution, must be 3.75% (3.5% + 0.25%) or 28.5dB SNR. The modulator and PA yield 29.1dB SNR based on 16QAM modulation. Consequently, the Tx DAC must have 8.86dB better SNR to yield 0.6dB degradation. The Tx DAC requires 37.96dB SNR (29.1dB + 8.86dB).
- PAPR:** For 2ⁿ-carrier (subcarriers = 256, 512, 2048) OFDMA signaling, the PAPR is 8dB to 12dB. This means the Tx DAC output must be backed off -12dB to prevent clipping during peaks. DAC clipping creates signal distortion, resulting in spurious emissions that degrade SER performance.
- Gain/offset errors:** The major contributor to gain error in a DAC is the internal voltage reference. The internal reference can have ±5% tolerance over temperature. Offset is residual from the internal DAC amplifier voltage offsets. Gain and offset errors are important considerations in the DAC error budget because they reduce the usable dynamic range. If the gain and offset errors are each 10% of full scale, then each contributes a 1dB reduction in dynamic range. Because of this error, the DAC must be backed off 1dB to prevent output clipping and another 1dB to account for limited dynamic range.
- Sin(x)/x correction:** The sin(x)/x frequency response at f_C/f_{OUT} = 4 results in -0.91dB attenuation at f_{OUT} = FCLK/4. A finite impulse response (FIR) filter implemented in digital baseband can correct for this. Alternatively, if this roll-off is acceptable, then a +0.91dB margin can be added to the SNR budget, which accounts for -0.91dB SNR degradation at f_{OUT} = FCLK/4.

The above analysis concludes that a Tx DAC with SNR = 52.87dB at FCLK = 17.5Mpsps can synthesize an 8.75MHz, 16QAM OFDMA WiBro signal spectrum at SER = 1e-6.

Auxiliary DAC

The auxiliary DAC channels are primarily used for level control functions like receiver AGC and PA output power. Factors influencing auxiliary DAC resolution and conversion rate include gain control voltage levels, gain range, gain step size, and settling time. Typical ZIF radios have approximately a 60dB receiver AGC baseband gain range with a 0.5dB step size, a 50dB transmitter VGA range with a 1dB step size, and a 30dB AFC range. The auxiliary functions typically have a 2V full-scale range and 100ms settling time. To calculate auxiliary DAC resolution, the AGC function provides a 60dB gain range and a 0.5dB step size = 120 steps. Therefore, 2ⁿ = 120 and n = 6.9 bits.

The DAC channels need to be guaranteed monotonic with less than ±2 LSB integral nonlinearity (INL). Absolute accuracy is not required because the DAC channels are used in a closed-loop system. However, guaranteed monotonic is important to maintain loop stability. To ensure system linearity, INL over a specified usable code range is adequate.

Auxiliary ADC

The auxiliary ADC parameters are primarily determined by input signal level and accuracy. However, in some applications such as 802.11a, a fast RSSI

conversion ($t < 5\mu\text{s}$) is needed. Generally, measurements such as PA power level, voltage standing-wave ratio (VSWR), and temperature sensing are not critical for speed. A typical RF power detector like the MAX4003 operating at $\text{RFIN} = 1900\text{MHz}$ has an analog output voltage range of 360mV ($P_{\text{IN}} = -45\text{dBm}$) to 1.58V ($P_{\text{IN}} = 0\text{dBm}$). A typical temperature sensor like the MAX6613 has an analog output range of 400mV to 2V with $\pm 4^\circ\text{C}$ accuracy. The resolution and conversion rate of general-purpose converters typically range from 8- to 10-bit and 50ksps to 300ksps, respectively.

Converter Summary

When interfacing with a ZIF radio, the following data converter parameters can support 64QAM downlink, 16QAM uplink with OFDM; and 1.25MHz to 5MHz channel bandwidth at 8x oversampling or up to 10MHz channel bandwidth with 4x oversampling:

- Dual, 10-bit, 40Msps high-speed Rx AD, SINAD = 51.86dB
- Dual, 10-bit, 40Msps high-speed Tx DAC, SNR = 52.87dB

A single integrated high-speed AFE device, such as the MAX19713, can meet the above system requirements and provide the following features and benefits:

- Dual, 10-bit, 45Msps high-speed Rx ADC, SINAD = 54.3dB with 2.4dB margin
- Dual, 10-bit, 45Msps high-speed Tx DAC, SNR = 56.1dB with 3.2dB margin
- Tx DAC common-mode adjust with I/Q offset trim
- Triple, 10-bit, low-speed auxiliary DAC with serial interface
- 10-bit, low-speed auxiliary ADC with 2:1 multiplexer and serial interface
- Production tested over temperature
- Ultra-low power at 87mW (29mA, 3.0V) in FD mode at 40Msps

Conclusion

To achieve high spectral efficiency and deliver high data throughput, today's wireless broadband systems employ advanced communication techniques like high-order modulation with OFDM, wide variable channel bandwidths, and MIMO radio architectures. These advanced communication techniques increase the performance requirements of radio-related high-speed data converters, including dense integration of more converter channels, faster sampling rates, higher dynamic range, lower power, and smaller size. As CMOS geometry for digital baseband processors scale from 45nm to 28nm in an effort to decrease power and increase processing speed, the integration of high performance, high-speed data converters into a large-scale ASIC becomes more difficult, more costly, and higher risk.

Designers also face shorter product development cycles. They must achieve fast time to market with limited capital expenditure in order to control cost. Compounding these issues, the unstoppable trend in wireless end-products is to integrate more radio features such as WLAN, WAN, PAN, GPS, and mobile TV. This trend of radio feature integration forces designers to contend with a multiplicity of high-speed converter channels that must interface with an array of different radios to support a diverse set of air interface standards.

High-speed AFEs present an attractive solution to help combat these inter-related IC-process and product-development trends. High-speed AFEs like the MAX19713 yield several product-development benefits, including fast time to market, low initial investment, and proven capability. These devices also provide a reliable and flexible off-the-shelf solution to seamlessly interface with high sensitivity RF front-ends and sub-micron digital baseband processor modems.

Further Reading

Agilent application note, "8 Hints for Making and Interpreting EVM Measurements," <http://cp.literature.agilent.com/litweb/pdf/5989-3144EN.pdf>.

Agilent application note, "WiMAX Concepts and RF Measurements: IEEE 802.16-2004 WiMAX PHY layer operation and measurements," <http://cp.literature.agilent.com/litweb/pdf/5989-2027EN.pdf>.

Maxim reference schematic 4274, "WiBro Reference Design with the MAX2837."

Razavi, Behzad. *RF Microelectronics*. Upper Saddle River, N.J.: Prentice Hall, 1998.

Sklar, Bernard. *Digital Communications: Fundamentals and Applications*. Englewood Cliffs, N.J.: Prentice Hall, 1988.

The author would like to thank Scott Anderson of Maxim for contributing the data in Figure 4.

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WiBro is a registered trademark of the Telecommunications Technology Association.

WiMAX is a registered certification mark and registered service mark of the WiMAX Forum.

Related Parts		
MAX19713	10-Bit, 45Msps, Full-Duplex, Analog Front-End	Free Samples
MAX2208	RF Power Detectors in UCSP	
MAX2837	2.3GHz to 2.7GHz Wireless Broadband RF Transceiver	
MAX6613	Low-Voltage Analog Temperature Sensor in an SC70 Package	Free Samples

More Information

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For Samples: <https://www.maximintegrated.com/en/samples>

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Application Note 5519: <https://www.maximintegrated.com/en/an5519>

APPLICATION NOTE 5519, AN5519, AN 5519, APP5519, Appnote5519, Appnote 5519

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