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TFT | CHARACTER | UWVD | FSC | SEGMENT | CUSTOM | REPLACEMENT

# TFT Display Module

Part Number

E24RE-I-CW400-C

Overview:

- 2.4-inch TFT (42.92x60.26)
- 240 320
- Parallel, SPI, and RGB Interfaces
- ‡ ̇u ̈ erature
- All View

- Transmissive, IPS
- Capacitive Touch Panel
- 400 NITS
- TFT IC: ST7789V
- RoHS Compliant

## Description

This is a color active matrix TFT (Thin Film Transistor) LCD (Liquid Crystal Display) that uses amorphous silicon TFT as a switching device. This model is composed of a transmissive type TFT LCD Panel, driver circuit, a capacitive touch panel and a backlight unit. The resolution of the 2.4" TFT LCD contains 240RGB)x320 pixels and can display up to 262k colors.

## TFT Features

Low Input Voltage: 3.3V
Display Colors: 65k/262k
TFT Interfaces: 8/9/16/18-bit parallel MCU
              3/4-wire SPI+16/18-bit RGB
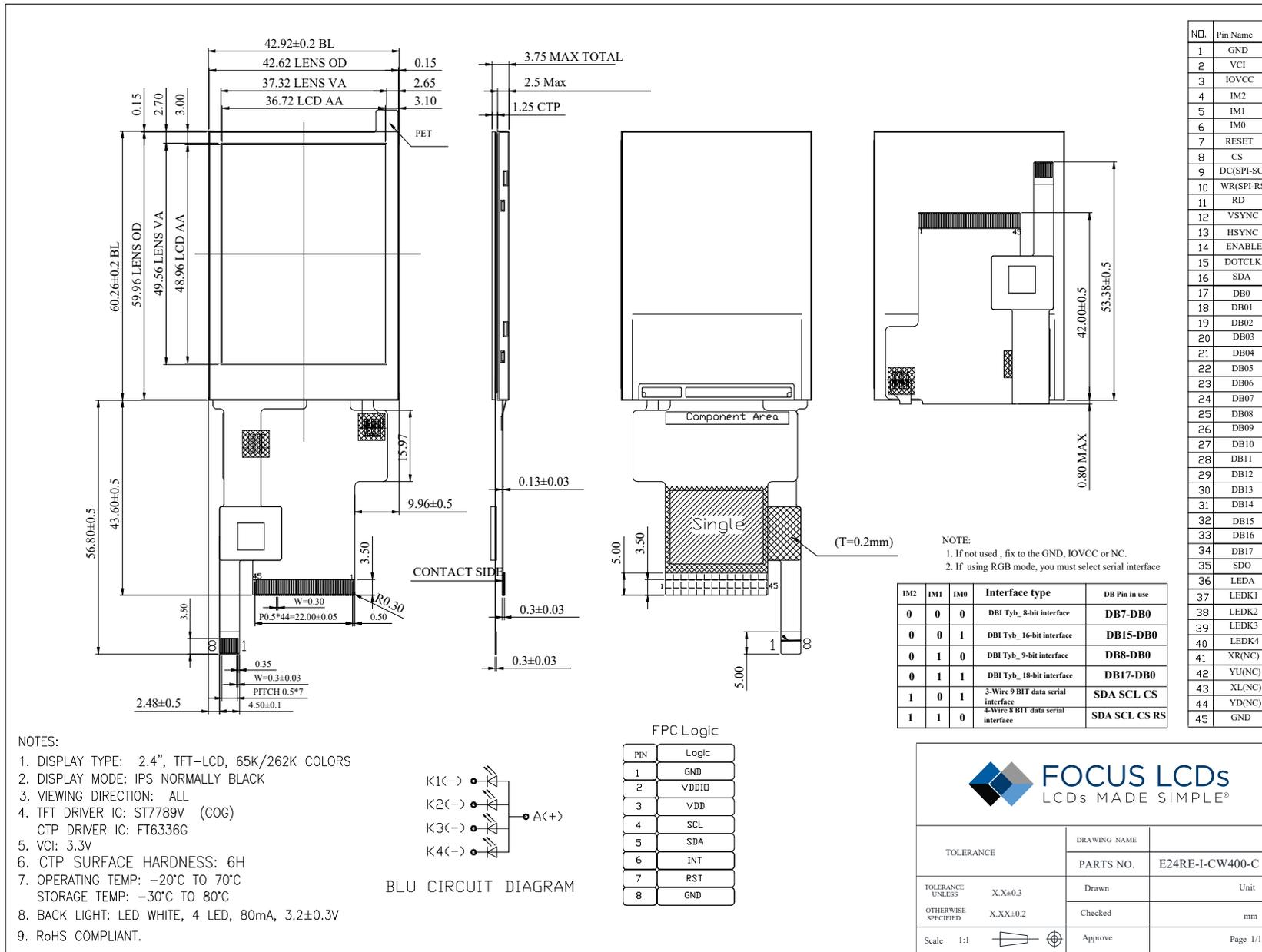              3/4-wire Serial
CTP Interface: I2C

| General Information Items | Specification<br>Main Panel | Unit | Note |
|---|---|---|---|
| TFT Display area (AA) | 36.72(H) x 48.96(V) (2.40 inch) | mm | - |
| Driver Element | TFT active matrix | - | - |
| Display Colors | 65k/262k | colors | - |
| Number of pixels | 240(RGB)x320 | dots | - |
| TFT Pixel arrangement | RGB vertical stripe | - | - |
| Pixel Pitch | 0.153(H)x0.153(V) | mm | - |
| Viewing angle | All | o'clock | - |
| TFT Controller IC | ST7789V | - | - |
| CTP Driver IC | FT6336G | - | - |
| Display mode | Transmissive, Normally Black | - | - |
| Touch Mode | Single point and gestures | - | - |
| Bonding Type | Tape | - | - |
| Operating temperature | -20-+70 | °C | - |
| Storage temperature | -30-+80 | °C | - |

## Mechanical Information

| Item | | Min | Typ. | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Module Size | Horizontal (H) | | 42.92 | | mm | - |
| | Vertical (V) | | 60.26 | | mm | - |
| | Depth (D) | | 3.75 | | mm | - |
| | Weight | | -- | | g | |

# 1. Outline Dimensions



**Dimensions (left view):**
- 42.92±0.2 BL
- 42.62 LENS OD
- 37.32 LENS VA
- 36.72 LCD AA
- 0.15
- 2.65
- 3.10
- 0.15, 2.70, 3.00
- 60.26±0.2 BL
- 59.96 LENS OD
- 49.56 LENS VA
- 48.96 LCD AA
- 56.80±0.5
- 43.60±0.5
- 15.97
- 9.96±0.5
- 3.50
- 2.48±0.5
- 3.50
- 0.35
- W=0.3±0.03
- PITCH 0.5*7
- 4.50±0.1
- W=0.30
- P0.5*44=22.00±0.05
- R0.30
- 0.50
- CONTACT SIDE

**Cross section (middle):**
- 3.75 MAX TOTAL
- 2.5 Max
- 1.25 CTP
- PET
- 0.13±0.03
- 0.3±0.03
- 0.3±0.03

**Right views:**
- 53.38±0.5
- 42.00±0.5
- 0.80 MAX
- Component Area
- Single
- (T=0.2mm)
- 5.00, 3.50
- 5.00
- 1 ... 45
- 1 ... 8

NOTE:
1. If not used , fix to the GND, IOVCC or NC.
2. If using RGB mode, you must select serial interface

## Pin Table

| NO. | Pin Name |
|-----|----------|
| 1 | GND |
| 2 | VCI |
| 3 | IOVCC |
| 4 | IM2 |
| 5 | IM1 |
| 6 | IM0 |
| 7 | RESET |
| 8 | CS |
| 9 | DC(SPI-SCL) |
| 10 | WR(SPI-RS) |
| 11 | RD |
| 12 | VSYNC |
| 13 | HSYNC |
| 14 | ENABLE |
| 15 | DOTCLK |
| 16 | SDA |
| 17 | DB0 |
| 18 | DB01 |
| 19 | DB02 |
| 20 | DB03 |
| 21 | DB04 |
| 22 | DB05 |
| 23 | DB06 |
| 24 | DB07 |
| 25 | DB08 |
| 26 | DB09 |
| 27 | DB10 |
| 28 | DB11 |
| 29 | DB12 |
| 30 | DB13 |
| 31 | DB14 |
| 32 | DB15 |
| 33 | DB16 |
| 34 | DB17 |
| 35 | SDO |
| 36 | LEDA |
| 37 | LEDK1 |
| 38 | LEDK2 |
| 39 | LEDK3 |
| 40 | LEDK4 |
| 41 | XR(NC) |
| 42 | YU(NC) |
| 43 | XL(NC) |
| 44 | YD(NC) |
| 45 | GND |

## Interface Table

| IM2 | IM1 | IM0 | Interface type | DB Pin in use |
|-----|-----|-----|----------------|---------------|
| 0 | 0 | 0 | DBI Tyb_ 8-bit interface | DB7-DB0 |
| 0 | 0 | 1 | DBI Tyb_ 16-bit interface | DB15-DB0 |
| 0 | 1 | 0 | DBI Tyb_ 9-bit interface | DB8-DB0 |
| 0 | 1 | 1 | DBI Tyb_ 18-bit interface | DB17-DB0 |
| 1 | 0 | 1 | 3-Wire 9 BIT data serial interface | SDA SCL CS |
| 1 | 1 | 0 | 4-Wire 8 BIT data serial interface | SDA SCL CS RS |

## NOTES:

1. DISPLAY TYPE:   2.4", TFT-LCD, 65K/262K COLORS
2. DISPLAY MODE: IPS NORMALLY BLACK
3. VIEWING DIRECTION:   ALL
4. TFT DRIVER IC: ST7789V  (COG)
   CTP DRIVER IC: FT6336G
5. VCI: 3.3V
6. CTP SURFACE HARDNESS: 6H
7. OPERATING TEMP: −20°C TO 70°C
   STORAGE TEMP: −30°C TO 80°C
8. BACK LIGHT: LED WHITE, 4 LED, 80mA, 3.2±0.3V
9. RoHS COMPLIANT.

## BLU CIRCUIT DIAGRAM

- K1(−)
- K2(−)
- K3(−)
- K4(−)
- A(+)

## FPC Logic

| PIN | Logic |
|-----|-------|
| 1 | GND |
| 2 | VDDIO |
| 3 | VDD |
| 4 | SCL |
| 5 | SDA |
| 6 | INT |
| 7 | RST |
| 8 | GND |

## FOCUS LCDs — LCDs MADE SIMPLE®

| TOLERANCE | DRAWING NAME | |
|-----------|--------------|--|
| | PARTS NO. | E24RE-I-CW400-C |
| TOLERANCE UNLESS X.X±0.3 | Drawn | Unit |
| OTHERWISE SPECIFIED X.XX±0.2 | Checked | mm |
| Scale 1:1 | Approve | Page 1/1 |

## 2. Block Diagram

## 3. Input Terminal Pin Assignment

Recommmended TFT Connnector: FH12S-45S-0.5SH(55)　　　|　　　Recommended CTP Connector: FH12-8S-0.5SH(55)

| NO. | Symbol | Description | I/O |
|---|---|---|---|
| 1 | GND | Ground | P |
| 2 | VCI | Supply voltage (3.3V) | P |
| 3 | IOVCC | I/O supply voltage (1.65-3.3V) | P |
| 4 | IM2 | Interface Selection: <br><br>| IM2 | IM1 | IM0 | Interface type | DB Pin in use |<br>|---|---|---|---|---|<br>| 0 | 0 | 0 | DBI Tyb_ 8-bit interface | DB7-DB0 |<br>| 0 | 0 | 1 | DBI Tyb_ 16-bit interface | DB15-DB0 |<br>| 0 | 1 | 0 | DBI Tyb_ 9-bit interface | DB8-DB0 |<br>| 0 | 1 | 1 | DBI Tyb_ 18-bit interface | DB17-DB0 |<br>| 1 | 0 | 1 | 3-Wire 9 BIT data serial interface | SDA SCL CS |<br>| 1 | 1 | 0 | 4-Wire 8 BIT data serial interface | SDA SCL CS RS | | I |
| 5 | IM1 | | I |
| 6 | IM0 | | I |
| 7 | RESET | Reset signal of the device. Must be applied to properly initialize the chip. | I |
| 8 | CS | Chip select pin, low enabled. Fix to VCI or GND when not in use. | I |
| 9 | D/C(SPI_SCL) | Data or command selection pin in the parallel MCU interface. D/C=1, data is selected. D/C=0, command is selected. Pin is also used as the serial interface clock. | I |
| 10 | WR(SPI_RS) | Write signal for the parallel MCU interface. Also acts as the second data pin in the serial interface. Fix to VCI or GND when not in use. | I |
| 11 | RD | Read signal for the parallel MCU interface. Reads data at the rising edge. Fix to VCI or GND when not in use. | I |
| 12 | VSYNC | Frame synchronizing signal for the RGB interface. Fix to VCI or GND when not in use. | I |
| 13 | HSYNC | Line synchronizing signal for the RGB interface. Fix to VCI or GND when not in use. | I |
| 14 | ENABLE | Data enable signal for the RGB interface. Fix to VCI or GND when not in use. | I |
| 15 | DOTCLK | Dot clock signal for the RGB interface. Fix to VCI or GND when not in use. | I |
| 16 | SDA | Serial data input signal. The data is latched at the rising edge of the SCL signal. Fix to VCI or GND when not in use. | I |
| 17-34 | DB0-DB17 | 18-bit parallel bi-directional data bus for the parallel MCU and RGB interfaces. Fix to GND when not used. | I/O |
| 35 | SDO | Serial interface output pin. The data is output on the falling edge of the SCL signal. Leave this pin open when not used. | O |
| 36 | LEDA | Anode pin of the backlight | P |
| 37-40 | LEDK1-LEDK4 | Cathode pin of the backlight | P |
| 41-44 | NC | Not connected | |
| 45 | GND | Ground | P |

*I: Input, O: Output, P: Power*

### 3.2    CTP

| NO. | Symbol | Description | I/O |
|---|---|---|---|
| 1 | GND | Ground | P |
| 2 | VDDIO | I/O power supply voltage | P |
| 3 | VDD | Supply voltage | P |
| 4 | SCL | I2C clock input | I |
| 5 | SDA | I2C data input and output | I/O |
| 6 | INT | External interrupt pin | I |
| 7 | RST | Reset signal, low is active. | I |
| 8 | GND | Ground | P |

# 4. LCD Optical Characteristics

## 4.1 Optical Specifications

| Item | | Symbol | Condition | Min | Typ. | Max | Unit | Note |
|---|---|---|---|---|---|---|---|---|
| Color Gamut | | S | Normal viewing angle θ=0 | -- | 70 | -- | % | (3) |
| Contrast Ratio | | CR | | 600 | 800 | -- | % | (2) |
| Response Time | Rising | $T_R$ | | -- | 16 | 21 | ms | (4) |
| | Falling | $T_F$ | | -- | 19 | 24 | | |
| Color Filter Chromaticity | White | $W_X$ | | 0.274 | 0.314 | 0.354 | | (5)(6) |
| | | $W_Y$ | | 0.314 | 0.345 | 0.385 | | |
| | Red | $R_X$ | | 0.613 | 0.633 | 0.653 | | |
| | | $R_Y$ | | 0.315 | 0.335 | 0.355 | | |
| | Green | $G_X$ | | 0.304 | 0.324 | 0.344 | | |
| | | $G_Y$ | | 0.594 | 0.614 | 0.634 | | |
| | Blue | $B_X$ | | 0.130 | 0.150 | 0.170 | | |
| | | $B_Y$ | | 0.027 | 0.047 | 0.067 | | |
| Viewing Angle | Hor. | ΘL | CR≥10 | -- | 80 | -- | degrees | (1)(6) |
| | | ΘR | | -- | 80 | -- | | |
| | Ver. | ΘT | | -- | 80 | -- | | |
| | | ΘB | | -- | 80 | -- | | |
| Option View Direction | | All | | | | | | (1) |

**Optical Specification Reference Notes:**

(1) Definition of Viewing Angle: The viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3,9 o'clock direction and the vertical or 6,12 o'clock direction with respect to the optical axis which is normal to the LCD surface.
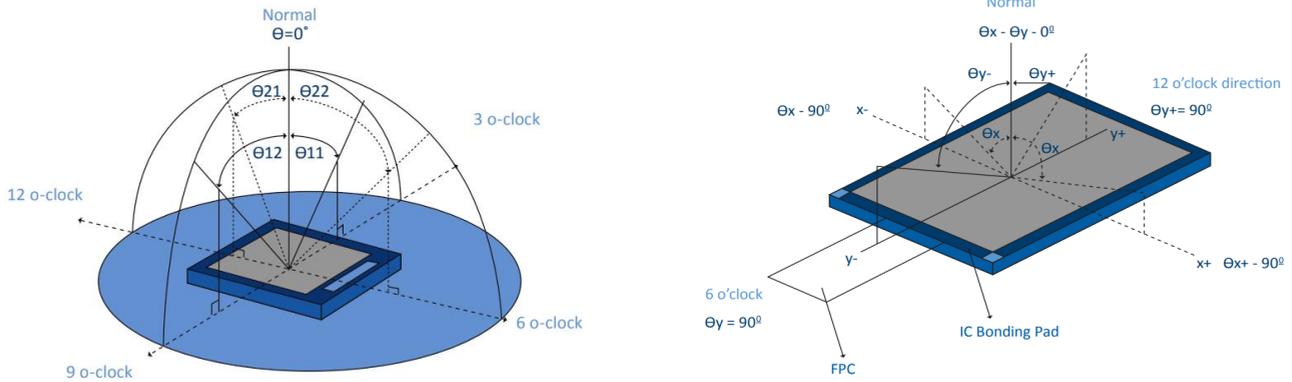


(2) Definition of Contrast Ratio (Cr): measured at the center point of panel. The contrast ratio (Cr) measured on a module, is the ratio between the luminance (Lw) in a full white area (R=G=B=1) and the luminance (Ld) in a dark area (R=G=B=0).

$$Cr = \frac{Lw}{Ld}$$

(3) Definition of transmittance (T%): The transmittance of the panel including the polarizers is measured with electrical driving. The equation for transmittance Tr is:

$$Tr = \frac{It}{Io} \, x \, 100\%$$
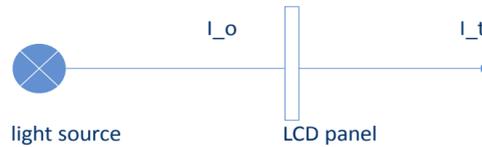


Io = the brightness of the light source.
It = the brightness after panel transmission

(4) Definition of Response Time (Tr, Tf): The rise time 'Tr' is defined as the time for luminance to change from 90% to 10% as a result of a change of the electrical condition. The fall time 'Tf' is defined as the time for luminance to change from 10% to 90% as a result of a change of the electrical condition.
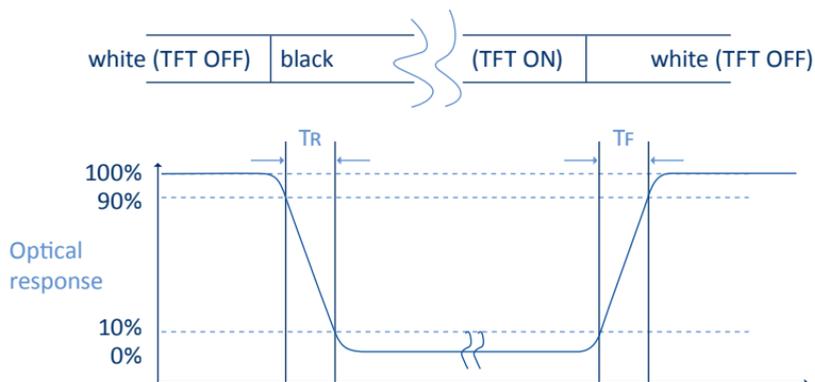
(5) Definition of Color Gamut:

Measuring machine CFT-01. NTSC's Primaries: R(x,y,Y),G(x,y,Y), B(x,y,Y). FPM520 of Westar Display Technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.The color chromaticity shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.
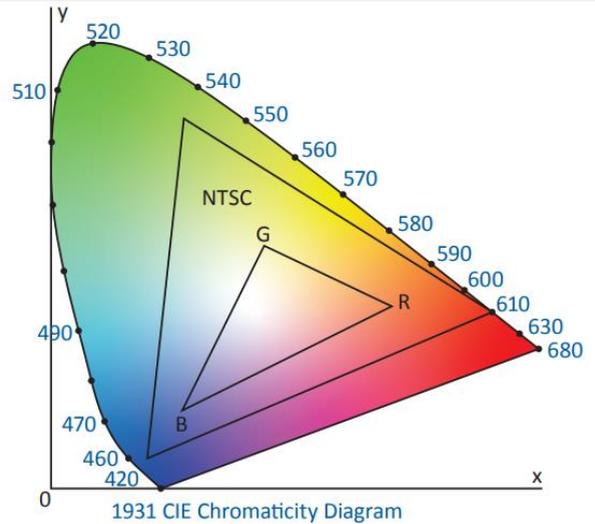


Fig. 1931 CIE chromacity diagram

$$\text{Color gamut: } S = \frac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}} \times 100\%$$

(6) Definition of Optical Measurement Setup:

The LCD module should be stabilized at a given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 20 minutes.
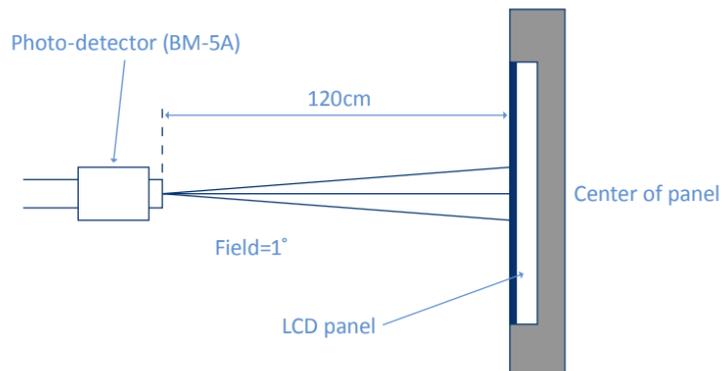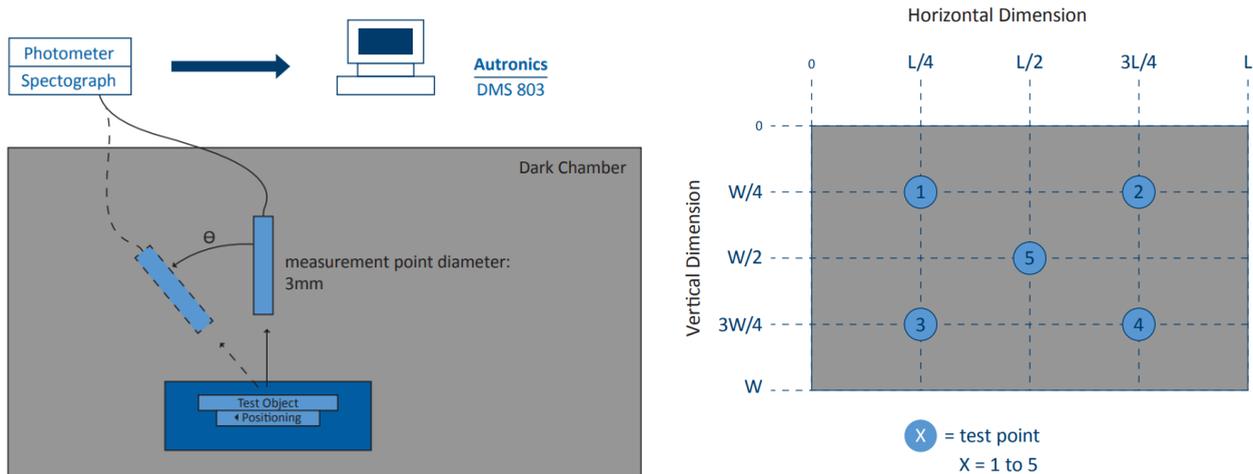
## 5. TFT Electrical Characteristics

### 5.1 Absolute Maximum Rating (Ta=25 ˚C, VSS=0V)

| Characteristics | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Digital Supply Voltage | VCI | -0.3 | 4.6 | V |
| Analog Interface Supply Voltage | IOVCC | -0.3 | 4.6 | V |
| Operating Temperature | TOP | -20 | +70 | °C |
| Storage Temperature | TST | -30 | +80 | °C |

*NOTE: If the absolute maximum rating of the above parameters is exceeded, even momentarily, the quality of the product may be degraded. Absolute maximum ratings specify the values which the product may be physically damaged if exceeded. Be sure to use the product within the range of the absolute maximum ratings.*

### 5.2 DC Electrical Characteristics

| Characteristics | Symbol | Min | Typ. | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Digital Supply Voltage | VCI | 2.4 | 3.3 | 3.6 | V | |
| I/O Supply Voltage | IOVCC | 1.65 | 1.8 | 3.3 | V | |
| Normal Mode Current Consumption | IDD | -- | 7 | -- | mA | |
| Level Input Voltage | $V_{IH}$ | 0.7*IOVCC | -- | IOVCC | V | |
| | $V_{IL}$ | GND | -- | 0.3IOVCC | V | |
| Level Output Voltage | $V_{OH}$ | 0.8IOVCC | -- | IOVCC | V | |
| | $V_{OL}$ | GND | -- | 0.2IOVCC | V | |

## 5.3 LED Backlight Characteristics

| Item | Symbol | Min | Typ. | Max | Unit | Note |
|------|--------|-----|------|-----|------|------|
| Forward Current | IF | 60 | 80 | -- | mA | |
| Forward Voltage | VF | -- | 3.2 | -- | V | |
| LCM Luminance | LV | 400 | -- | -- | cd/m2 | Note 3 |
| LED lifetime | Hr | -- | 50000 | -- | hour | Note1 & 2 |
| Uniformity | AVg | 80 | -- | -- | % | Note 3 |

The back-light system is edge-lighting type with 4 white LEDs.

Note 1: LED lifetime (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25±3 °C, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note 2: The "LED lifetime" is defined as the module brightness decrease to 50% original brightness at Ta=25°C and IL=80mA. The LED lifetime could be decreased if operating IL is larger than 80mA. The constant current driving method is suggested.
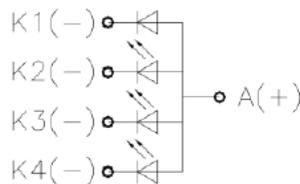


**Backlight LED Circuit**

Note 3: Luminance Uniformity of these 9 points is defined as below:
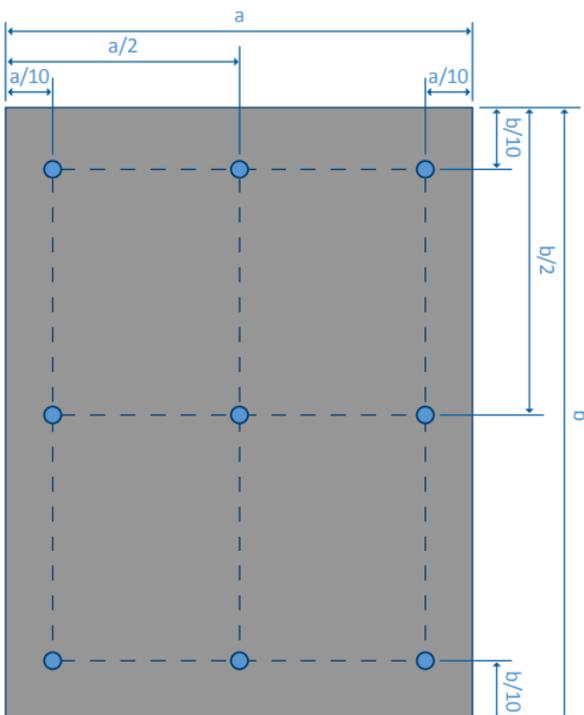


$$Luminance = \frac{(Total\ Luminance\ of\ 9\ points)}{9}$$

$$Uniformity = \frac{minimum\ luminance\ in\ 9\ points(1-9)}{maximum\ luminance\ in\ 9\ points(1-9)}$$

# 6. AC Characteristic

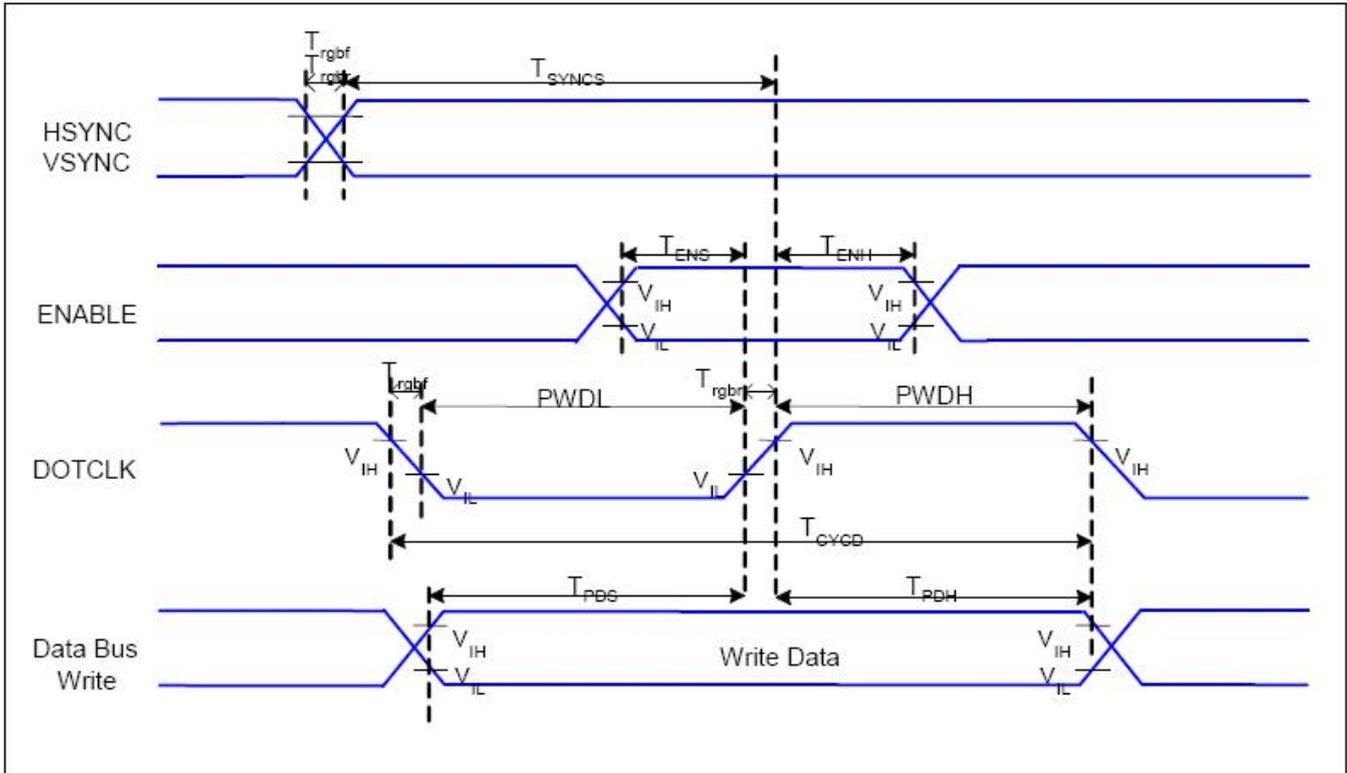## 6.1 Parallel RGB Interface Characteristics



*Figure 6.1: Parallel RGB Interface Timing Diagram*

| Signal | Symbol | Parameter | Min | Max | Unit | Description |
|--------|--------|-----------|-----|-----|------|-------------|
| HSYNC, VSYNC | $T_{SYNCS}$ | VSYNC, HSYNC Setup Time | 30 | - | ns | |
| ENABLE | $T_{ENS}$ | Enable Setup Time | 25 | - | ns | |
| | $T_{ENH}$ | Enable Hold Time | 25 | - | ns | |
| DOTCLK | PWDH | DOTCLK High-level Pulse Width | 60 | - | ns | |
| | PWDL | DOTCLK Low-level Pulse Width | 60 | - | ns | |
| | $T_{CYCD}$ | DOTCLK Cycle Time | 120 | - | ns | |
| | $T_{RGHR}, T_{RGHF}$ | DOTCLK Rise/Fall Time | - | 20 | ns | |
| DB | $T_{PDS}$ | PD Data Setup Time | 50 | - | ns | |
| | $T_{PDH}$ | PD Data Hold Time | 50 | - | ns | |

*Table 6.1: Parallel RGB Interface Timing Characteristics*

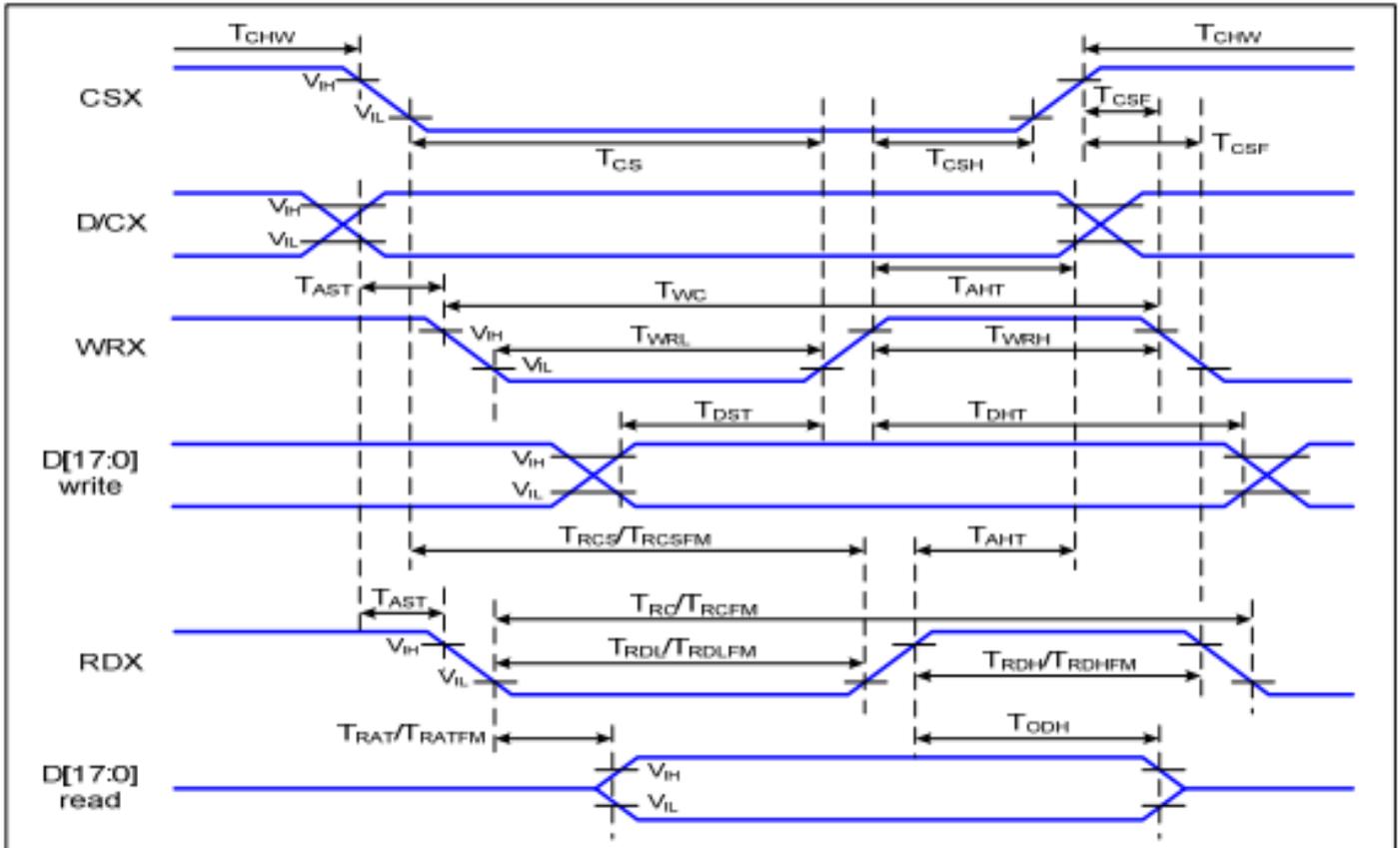## 6.2    8080 Series MCU Parallel Interface Characteristics: 18/16/9/8-bit Bus



*Figure 6.2: Parallel Interface Timing Characteristics (8080-Series MCU Interface)*

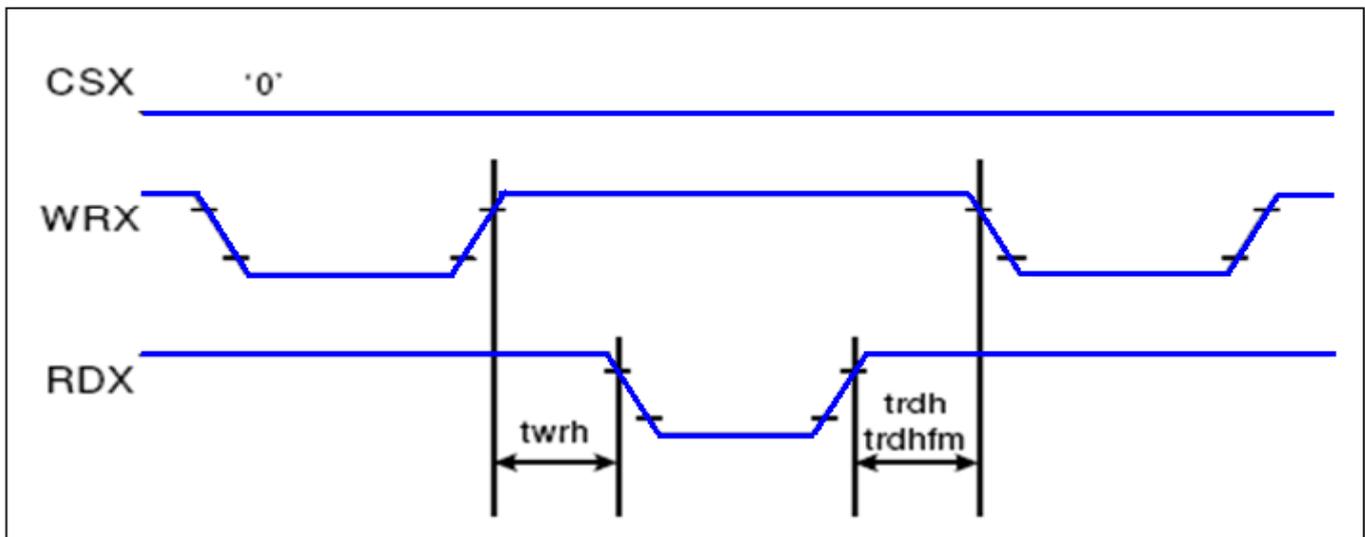| Signal | Symbol | Parameter | Min | Max | Unit | Description |
|--------|--------|-----------|-----|-----|------|-------------|
| D/CX | $T_{AST}$ | Address setup time | 0 | - | ns | |
| | $T_{AHT}$ | Address hold time (Write/Read) | 10 | - | ns | |
| CSX | $T_{CHW}$ | Chip select "H" pulse width | 0 | - | ns | |
| | $T_{CS}$ | Chip select setup time (Write) | 15 | - | ns | |
| | $T_{RCS}$ | Chip select setup time (Read ID) | 45 | - | ns | |
| | $T_{RCSFM}$ | Chip select setup time (Read FM) | 355 | - | ns | |
| | $T_{CSF}$ | Chip select wait time (Write/Read) | 10 | - | ns | |
| | $T_{CSH}$ | Chip select hold time | 10 | - | ns | |
| WRX | $T_{WC}$ | Write cycle | 66 | - | ns | |
| | $T_{WRH}$ | Control pulse "H" duration | 15 | - | ns | |
| | $T_{WRL}$ | Control pulse "L" duration | 15 | | ns | |
| RDX (ID) | $T_{RC}$ | Read cycle (ID) | 160 | - | ns | |
| | $T_{RDH}$ | Control pulse "H" duration (ID) | 90 | - | ns | |
| | $T_{RDL}$ | Control pulse "L" duration | 45 | - | ns | |
| RDX (FM) | $T_{RCFM}$ | Read cycle (FM) | 450 | - | ns | |
| | $T_{RDHFM}$ | Control pulse "H" duration (FM) | 90 | - | ns | |
| | $T_{RDLFM}$ | Control pulse "L" duration (FM) | 355 | - | ns | |
| D[17:0] | $T_{DST}$ | Write data setup time | 10 | - | ns | |
| D[15:0], | $T_{DHT}$ | Write data hold time | 10 | - | ns | For max CL=30pF |
| D[8:0], | $T_{RAT}$ | Read access time (ID) | - | 40 | ns | |
| D[7:0] | $T_{RATFM}$ | Read access time (FM) | - | 340 | ns | For min CL=8pF |
| | $T_{ROD}$ | Output disable time | 20 | 80 | ns | |

*Table 6.2:  8080 Series MCU Parallel Timing Characteristics*

CSX timings:
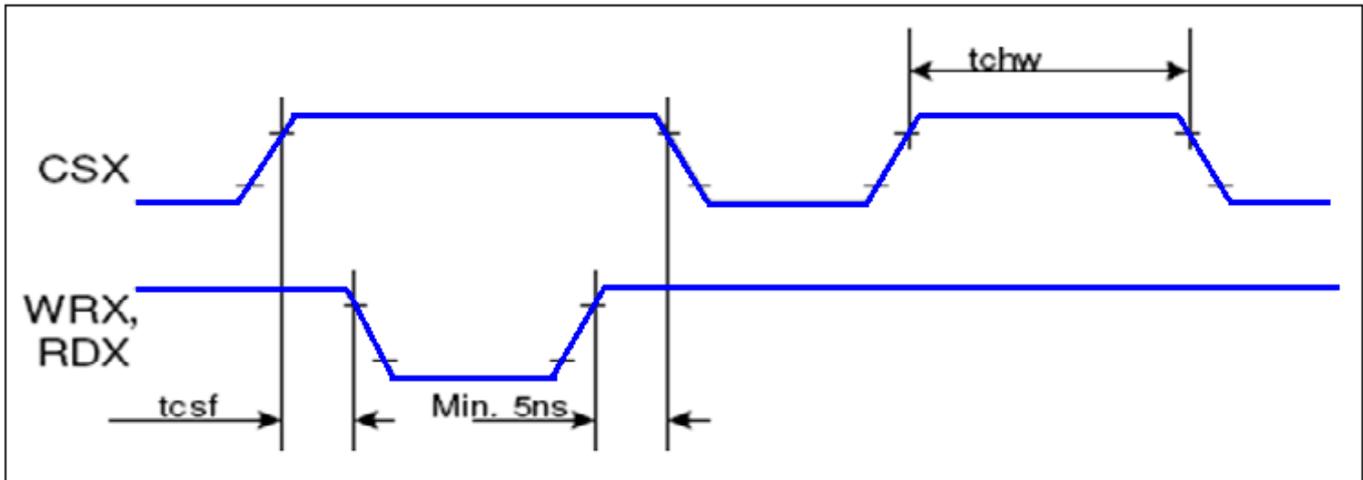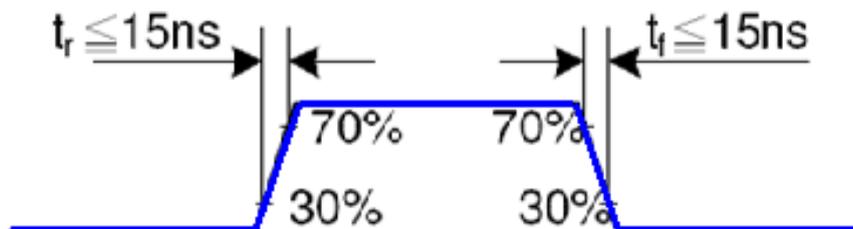


Note: Logic high and low levels are specified as 30% and 70% of IOVCC for input signals.

Write to read or read to write timings:



Note: Ta = -30 to 70 C, IOVCC = 1.65V to 2.8V, VCI = 2.6V to 3.3V, GND = 0V.

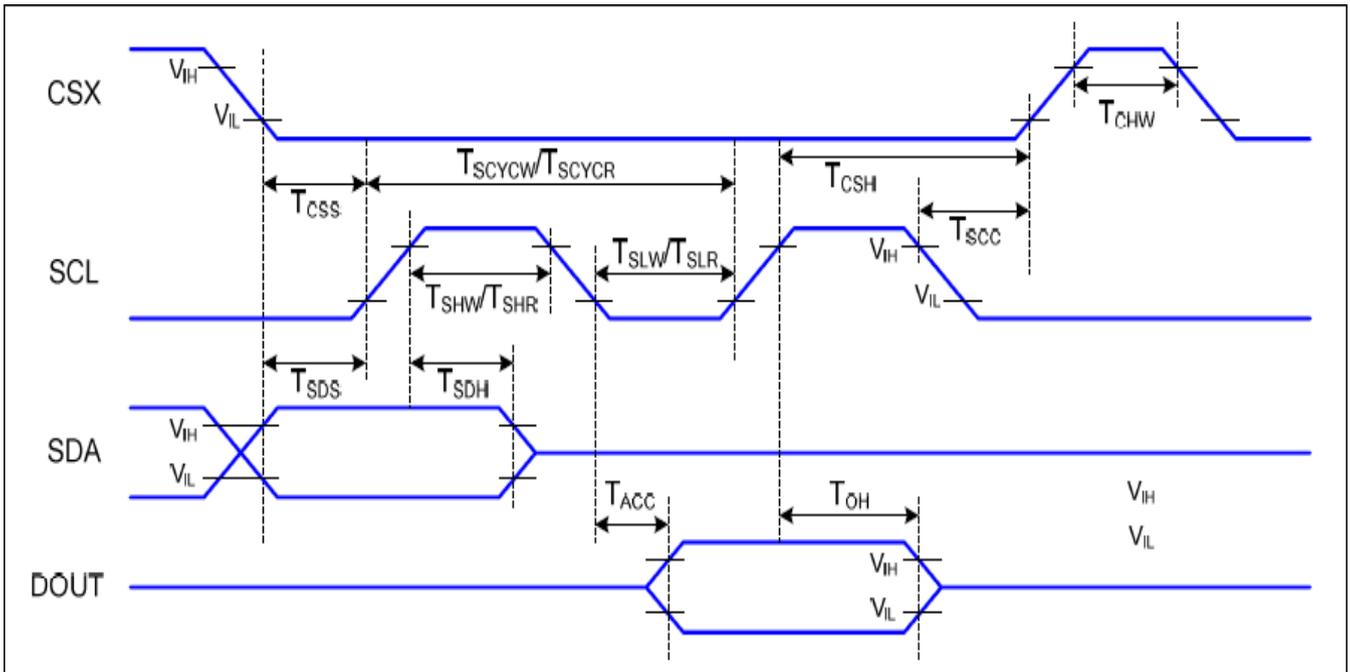## 6.3 Display Serial Interface Characteristics (3-line SPI system)



*Figure 6.3: Serial Interface 3-SPI Timing Diagram*

*VDDI = 1.64 to 3.3V, VDD = 2.4 to 3.3V, AGND=DGND=0V, Ta=-30 to 70 C°*

| Signal | Symbol | Parameter | Min | Max | Unit | Description |
|--------|--------|-----------|-----|-----|------|-------------|
| CSX | $T_{CSS}$ | Chip select setup time (write) | 15 | | ns | |
| | $T_{CSH}$ | Chip select hold time (write) | 15 | | ns | |
| | $T_{CSS}$ | Chip select setup time (read) | 60 | | ns | |
| | $T_{SCC}$ | Chip select hold time (read) | 65 | | ns | |
| | $T_{CHW}$ | Chip select "H" pulse width | 40 | | ns | |
| SCL | $T_{SCYCW}$ | Serial clock cycle (write) | 66 | | ns | |
| | $T_{SHW}$ | SCL "H" pulse width (write) | 15 | | ns | |
| | $T_{SLW}$ | SCL "L" width (write) | 15 | | ns | |
| | $T_{SCYCR}$ | Serial clock cycle (read) | 150 | | ns | |
| | $T_{SHR}$ | SCL "H" pulse width (read) | 60 | | ns | |
| | $T_{SLR}$ | SCL "L" pulse width (read) | 60 | | ns | |
| SDA (DIN) | $T_{SDS}$ | Data setup time | 10 | | ns | |
| | $T_{SDH}$ | Data hold time | 10 | | | |
| DOUT | $T_{ACC}$ | Access time | 10 | 50 | ns | For max CL=30pF For min CL=8pF |
| | $T_{OH}$ | Output disable time | 15 | 50 | | |

*Table 6.4: 3-line Serial Interface Timing Characteristics*

*Note: The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals*

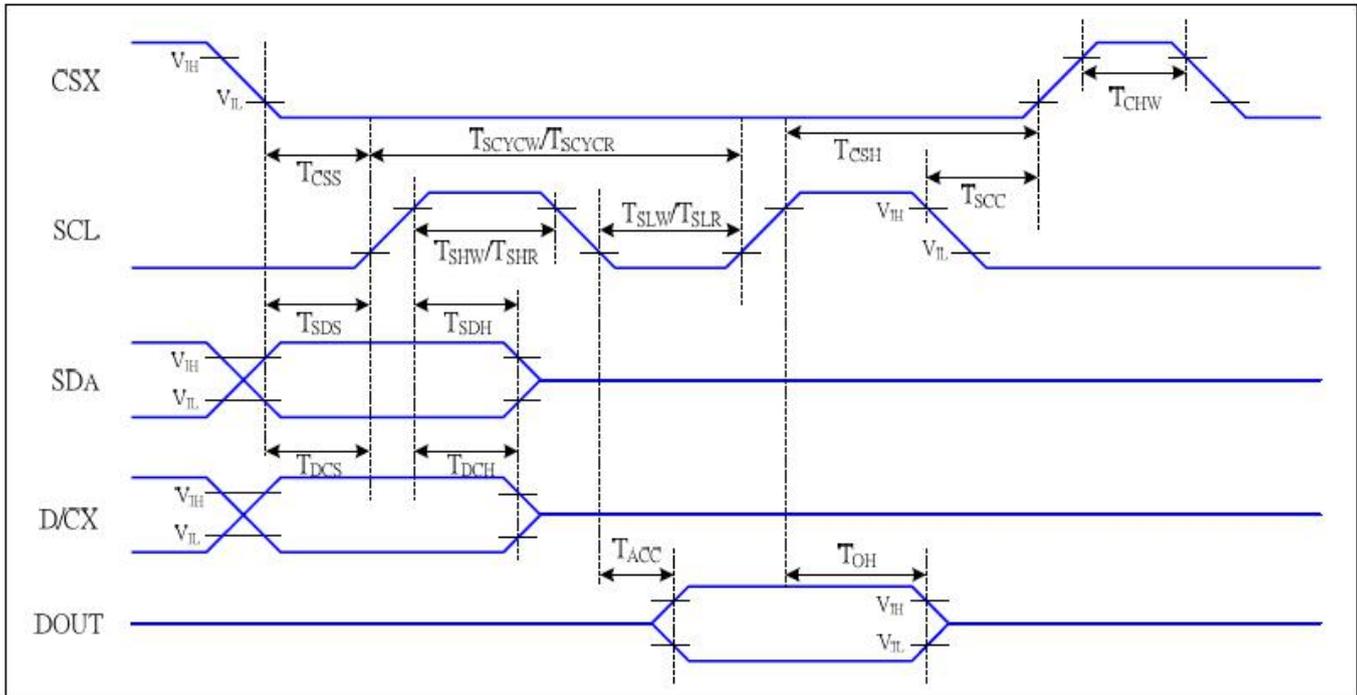## 6.4 Display Serial Interface Characteristics (4-line SPI serial)



*Figure 6.4: Serial Interface 4-SPI Timing Diagram*

| Signal | Symbol | Parameter | Min | Max | Unit | Description |
|---|---|---|---|---|---|---|
| CSX | $T_{CSS}$ | Chip select setup time (write) | 15 | | ns | |
| | $T_{CSH}$ | Chip select hold time (write) | 15 | | ns | |
| | $T_{CSS}$ | Chip select setup time (read) | 60 | | ns | |
| | $T_{SCC}$ | Chip select hold time (read) | 65 | | ns | |
| | $T_{CHW}$ | Chip select "H" pulse width | 40 | | ns | |
| SCL | $T_{SCYCW}$ | Serial clock cycle (write) | 66 | | ns | write command & data ram |
| | $T_{SHW}$ | SCL "H" pulse width (write) | 15 | | ns | |
| | $T_{SLW}$ | SCL "L" width (write) | 15 | | ns | |
| | $T_{SCYCR}$ | Serial clock cycle (read) | 150 | | ns | read command & data ram |
| | $T_{SHR}$ | SCL "H" pulse width (read) | 60 | | ns | |
| | $T_{SLR}$ | SCL "L" pulse width (read) | 60 | | ns | |
| D/CX | $T_{DCS}$ | D/CX setup time | 10 | | ns | |
| | $T_{DCH}$ | D/CX hold time | 10 | | ns | |
| SDA (DIN) | $T_{SDS}$ | Data setup time | 10 | | ns | |
| | $T_{SDH}$ | Data hold time | 10 | | ns | |
| DOUT | $T_{ACC}$ | Access time | 10 | 50 | ns | For max CL=30pF For min CL=8pF |
| | $T_{OH}$ | Output disable time | 15 | 50 | ns | |

*Table 6.5: 4-line Serial Interface Timing Characteristics*

*Note: The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.*
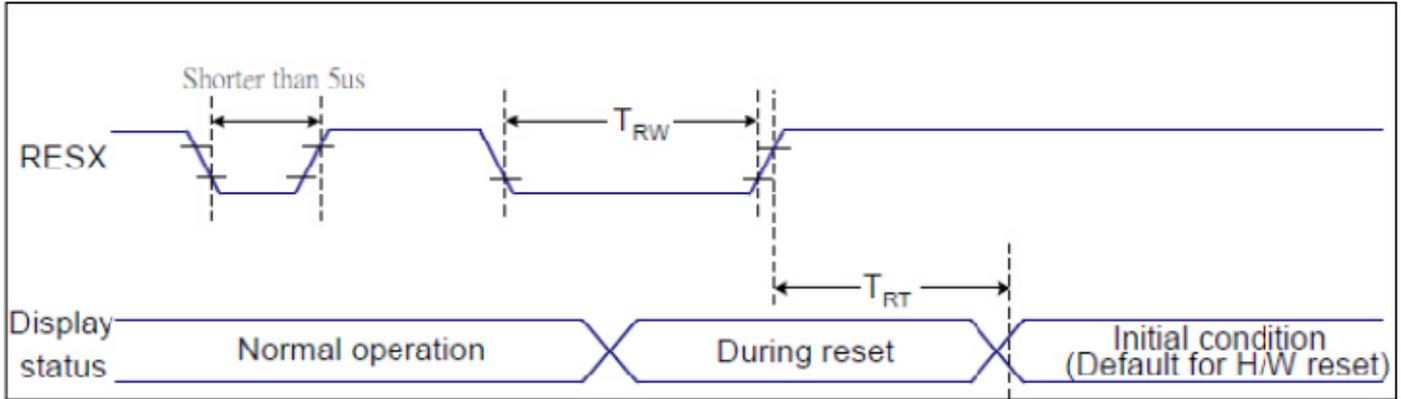
## 6.5 Reset Timing



*Figure 6.5: Reset Timing Diagram*

| Related Pins | Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|---|
| RESX | TRW | Reset pulse duration | 10 | - | us |
| | TRT | Reset cancel | - | 5 (Note 1,5) | ms |
| | | | | 120 (Note 1, 6, 7) | ms |

Notes:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not because irregular system reset according to the table below:

| RESX Pulse | Action |
|---|---|
| Shorter than 5us | Reset Rejected |
| Longer than 9us | Reset |
| Between 5us and 9 us | Reset starts |

3. During the resetting period, the display will be blanked (the display is entering blanking sequence, which maximum time is 120ms, when reset starts in Sleep Out mode. The display remains the blank state in Sleep in mode) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:
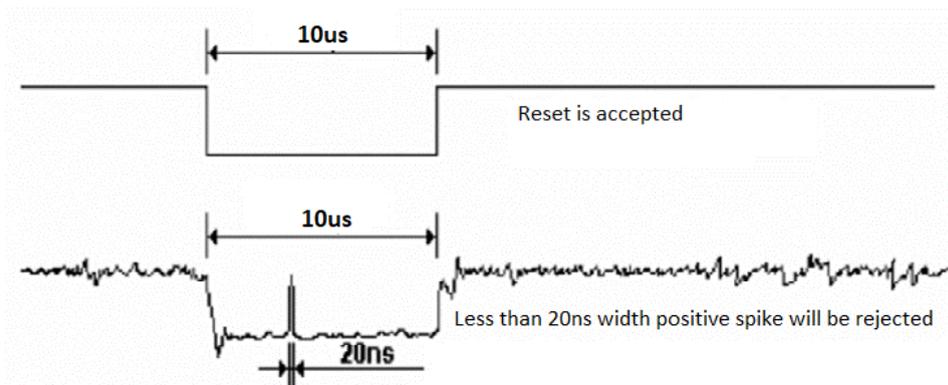


5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5ms after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120ms.

## 7.    CTP Electrical Characteristics

### 7.1    Absolute Maximum Rating

| Item | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Power Supply Voltage | VDD | -0.3 | 3.6 | V | 1 |
| I/O Digital Voltage | VDDIO | 1.8 | 3.6 | V | 1 |
| Operating Temperature | $T_{OP}$ | -30 | +70 | ℃ | - |
| Storage Temperature | $T_{ST}$ | -30 | +80 | ℃ | - |

*Note 1: If used beyond the absolute maximum ratings, FT6336G may permanently damage. It is strongly recommended that the device be used within the electrical characteristics in normal operations. If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device.*

### 7.2    DC Electrical Characteristics (Ta=25℃)

| Item | Symbol | Condition | Min | Typ. | Max | Unit | Note |
|---|---|---|---|---|---|---|---|
| Digital supply voltage | VDD | | 2.8 | 3.3 | 3.6 | V | |
| I/O Digital supply voltage | VDDIO | | 1.8 | 3.3 | 3.6 | V | |
| Normal operation mode current consumption | $I_{OPr}$ | VDD=2.7V | | 4 | | mA | |
| Monitor mode current consumption | $I_{mon}$ | Ta=25℃ MCLK=17.5M | | 1.5 | | mA | |
| Sleep mode current consumption | $I_{sip}$ | Hz | | 50 | | uA | |
| Level input voltage | $V_{IH}$ | | 0.7VDDIO | | VDDIO | V | |
| | $V_{IL}$ | | -0.3 | | 0.3VDD | V | |
| Level output voltage | $V_{OH}$ | $I_{OH}$=-0.1mA | 0.7VDDIO | | | V | |
| | $V_{OL}$ | $I_{OL}$=0.1mA | | | 0.3VDDIO | V | |

### 7.3    AC Characteristics

| Item | Symbol | Test Condition | Min | Typ. | Max | Unit | Note |
|---|---|---|---|---|---|---|---|
| OSC clock 1 | fosc1 | VDDA=2.7V; Ta=25℃ | 49 | 50 | 51 | MHz | |
| Sensor acceptable clock | ftx | VDDA=2.8V; Ta=25℃ | 0 | 100 | 300 | kHz | |
| Sensor output rise time | Ttxr | VDDA=2.8V; Ta=25℃ | - | 100 | - | Ns | |
| Sensor output fall time | Ttxf | VDDA=2.8V; Ta=25℃ | - | 80 | - | Ns | |
| Sensor input voltage | Trxi | VDDA=2.8V; Ta=25℃ | - | 5 | - | V | |

## 7.4    I2C Interface

The I2C is always configured in the slave mode. The data transfer format is shown below.
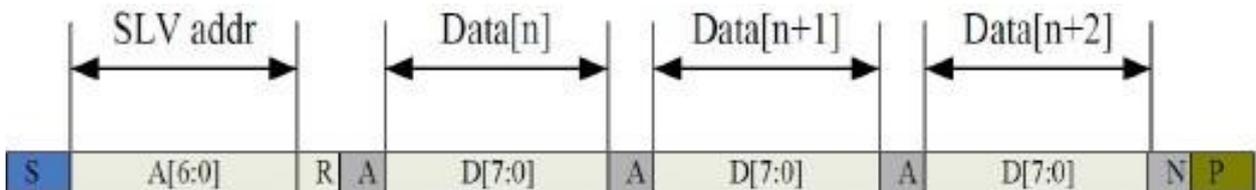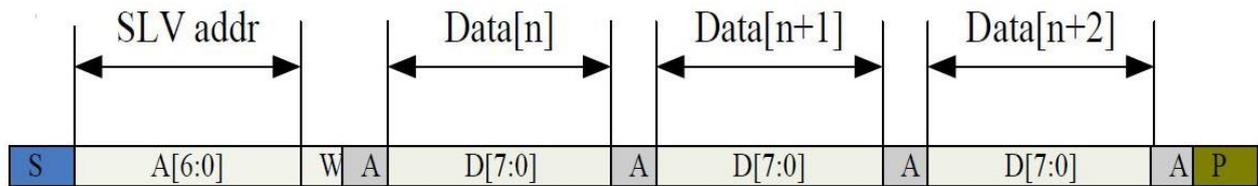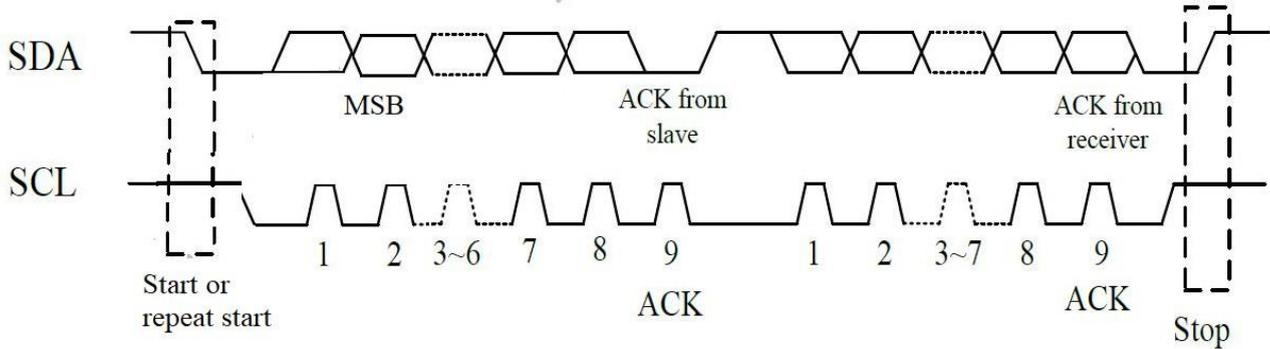






The following table lists the meanings of the mnemonics used in the above figures.

| Mnemonics | Description |
|---|---|
| S | I2C start or I2C restart |
| A [6:0] | Slave address |
| R/W | Read/Write bit, '1' for read, '0' for write |
| A(N) | ACK(NACK) |
| P | Stop: the indication of the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet) |

**I2C Interface Timing Characteristics**

| Parameter | Min | Max | Unit |
|---|---|---|---|
| SCL frequency | 10 | 400 | kHz |
| Bus free time between a stop and start condition | 4.7 | - | us |
| Hold time (repeated) start condition | 4.0 | - | us |
| Data setup time | 250 | - | ns |
| Setup time for a repeated start condition | 4.7 | - | us |
| Setup time for stop condition | 4.0 | - | us |

# 8. Cautions and Handling Precautions

## 8.1 Handling and Operating the Module

1. When the module is assembled, it should be attached to the system firmly. Do not warp or twist the module during assembly work.
2. Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
3. Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
4. Do not allow drops of water or chemicals to remain on the display surface. If you have the droplets for a long time, staining and discoloration may occur.
5. If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
6. The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
7. If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
8. Protect the module from static; it may cause damage to the CMOS ICs.
9. Use fingerstalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
10. Do not disassemble the module.
11. Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
12. Pins of I/F connector shall not be touched directly with bare hands.
13. Do not connect, disconnect the module in the "Power ON" condition.
14. Power supply should always be turned on/off by the item Power On Sequence & Power Off Sequence.

## 8.2 Storage and Transportation

1. Do not leave the panel in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35 °C and relative humidity of less than 70%
2. Do not store the TFT-LCD module in direct sunlight.
3. The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
4. It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module. In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
5. This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.

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