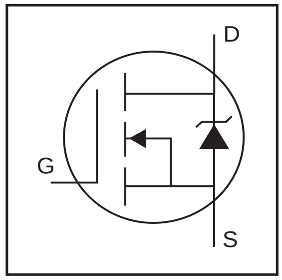
International
IOR Rectifier

PD - 91644A

IRL1004S
IRL1004L

HEXFET® Power MOSFET

- Logic-Level Gate Drive
- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated



V_{DSS} = 40V

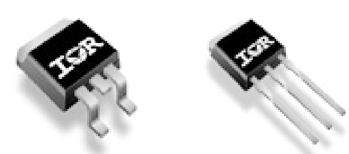
$R_{DS(on)}$ = 0.0065Ω

I_D = 130A⑤

Description

Fifth Generation HEXFET® power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D2Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D2Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.
The through-hole version (IRL1004L) is available for low-profile application.



D2Pak
IRL1004S

TO-262
IRL1004L

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V⑥	130 ⑤	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V⑥	92 ⑤	
I_{DM}	Pulsed Drain Current ①⑥	520	
P_D @T_A = 25°C	Power Dissipation	3.8	W
P_D @T_C = 25°C	Power Dissipation	200	W
	Linear Derating Factor	1.3	W/°C
V_{GS}	Gate-to-Source Voltage	± 16	V
E_{AS}	Single Pulse Avalanche Energy⑥	700	mJ
I_{AR}	Avalanche Current①	78	A
E_{AR}	Repetitive Avalanche Energy①	20	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑥	5.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	0.75	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted,steady-state)*	——	40	

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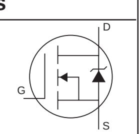
Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.04	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.0065	Ω	V_{GS} = 10V, I_D = 78A ④
		—	—	0.009		V_{GS} = 4.5V, I_D = 65A ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—		V	V_{DS} = V_{GS}, I_D = 250µA
g_{fs}	Forward Transconductance	63	—	—	S	V_{DS} = 25V, I_D = 78A⑥
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	µA	V_{DS} = 40V, V_{GS} = 0V
		—	—	250		V_{DS} = 32V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 16V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -16V
Q_g	Total Gate Charge	—	—	100	nC	I_D = 78A
Q_{gs}	Gate-to-Source Charge	—	—	32		V_{DS} = 32V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	43		V_{GS} = 4.5V, See Fig. 6 and 13 ④⑥
$t_{d(on)}$	Turn-On Delay Time	—	16	—	ns	V_{DD} = 20V,
t_r	Rise Time	—	210	—		I_D = 78A,
$t_{d(off)}$	Turn-Off Delay Time	—	25	—		R_G = 2.5Ω,
t_f	Fall Time	—	14	—		R_D = 0.18Ω, See Fig. 10 ④⑥
L_S	Internal Source Inductance	—	7.5	—	nH	Between lead, and center of die contact
C_{iss}	Input Capacitance	—	5330	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	1480	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	320	—		f = 1.0MHz, See Fig. 5⑤⑥

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)⑦	—	—	130⑤	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①⑦	—	—	520		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 78A, V_{GS} = 0V④
t_{rr}	Reverse Recovery Time	—	78	120	ns	T_J = 25°C, I_F = 78A
Q_{rr}	Reverse RecoveryCharge	—	180	270	nC	di/dt = 100A/µs④⑥
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting T_J = 25°C, L = 0.23mH R_G = 25Ω, I_{AS} = 78A. (See Figure 12)

③ $I_{SD} \leq$ 78A, di/dt ≤ 370A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq$ 175°C

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

⑤ Calculated continuous current based on maximum allowable junction temperature; for recommended current-handing of the package refer to Design Tip # 93-4

⑥ Uses IRL1004 data and test conditions

* When mounted on 1" square PCB (FR-4 or G-10 Material).
For recommended footprint and soldering techniques refer to application note #AN-994.

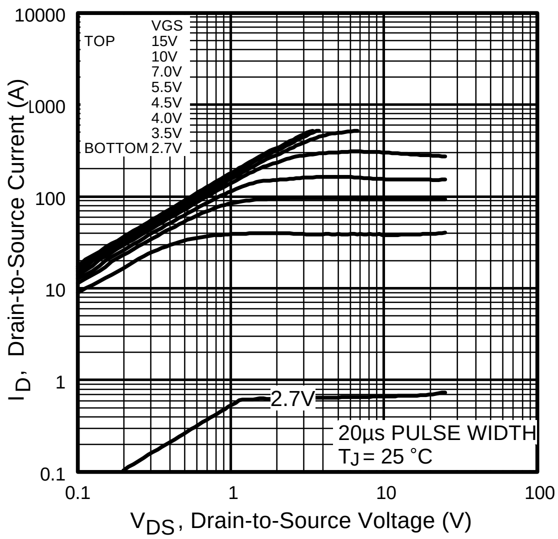


Fig 1. Typical Output Characteristics

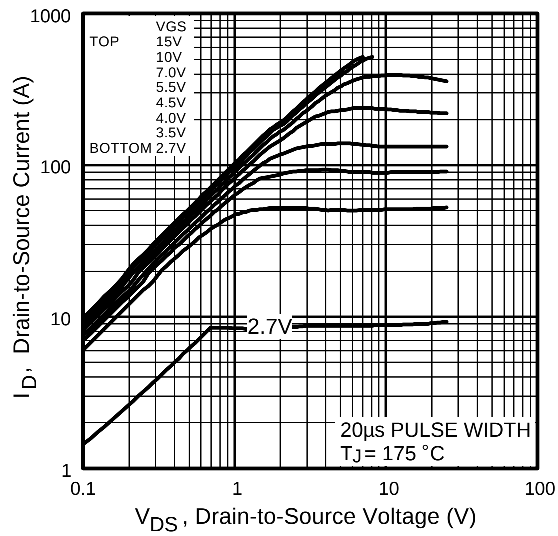


Fig 2. Typical Output Characteristics

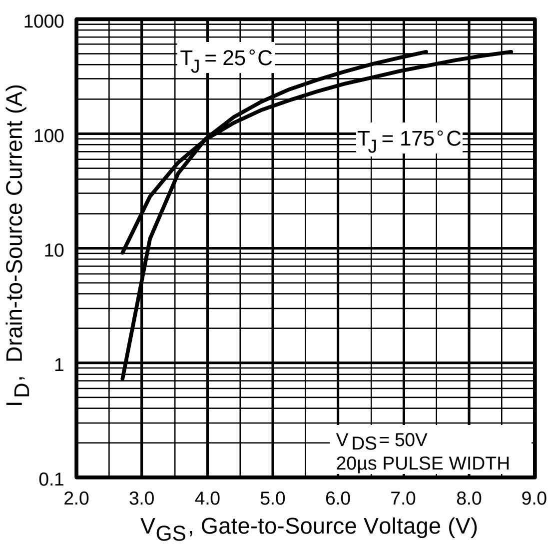


Fig 3. Typical Transfer Characteristics

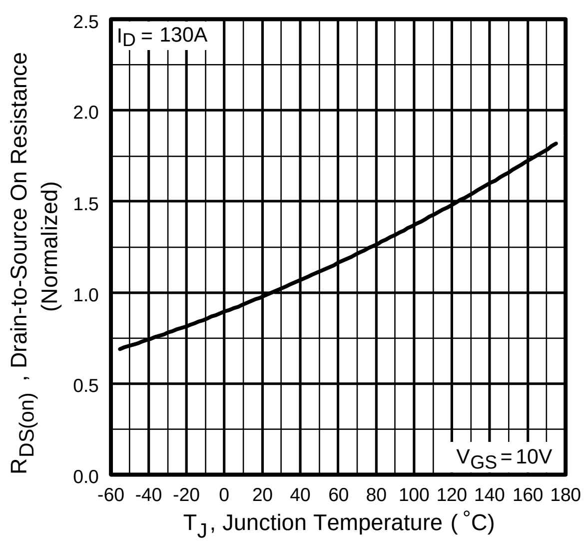


Fig 4. Normalized On-Resistance Vs. Temperature

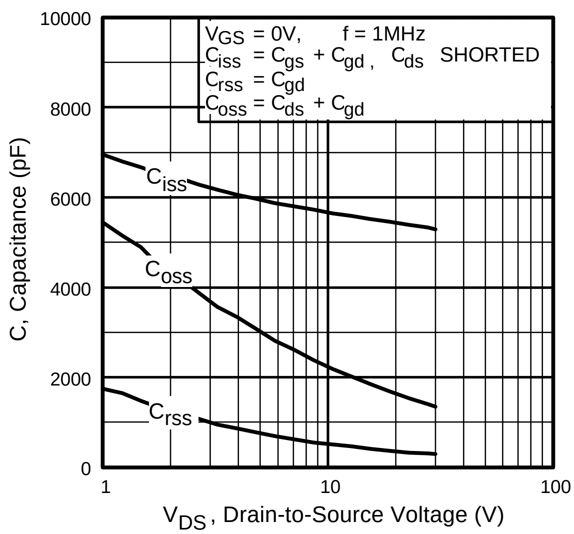


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

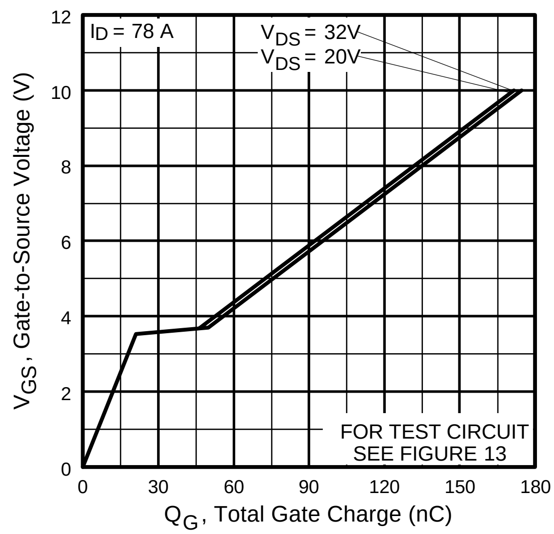


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

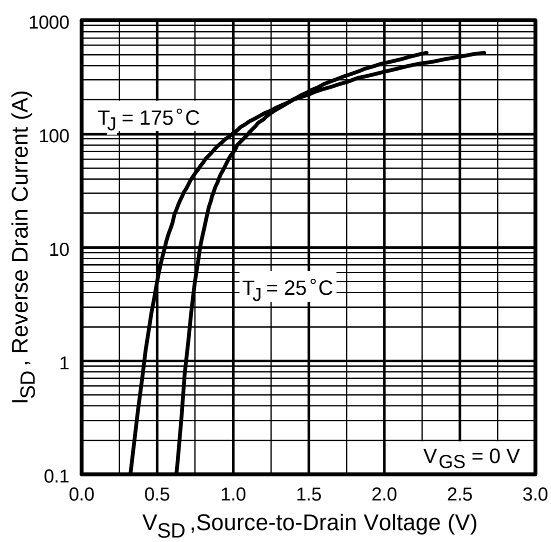


Fig 7. Typical Source-Drain Diode Forward Voltage

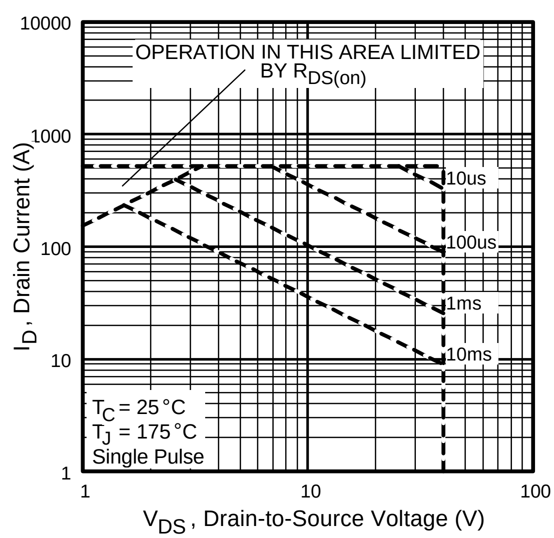


Fig 8. Maximum Safe Operating Area

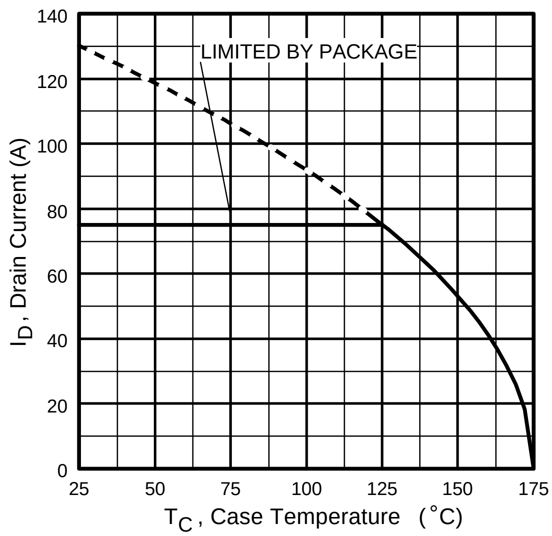


Fig 9. Maximum Drain Current Vs. Case Temperature

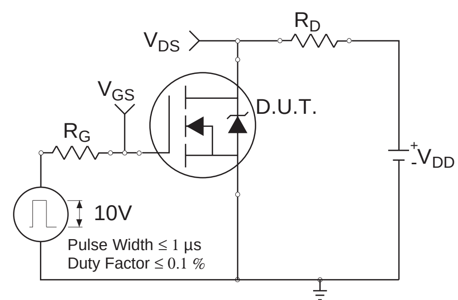


Fig 10a. Switching Time Test Circuit

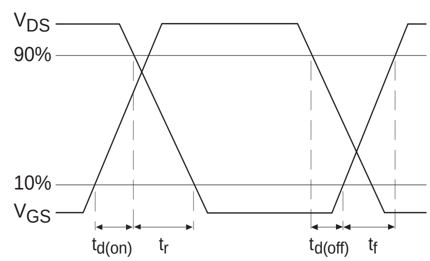


Fig 10b. Switching Time Waveforms

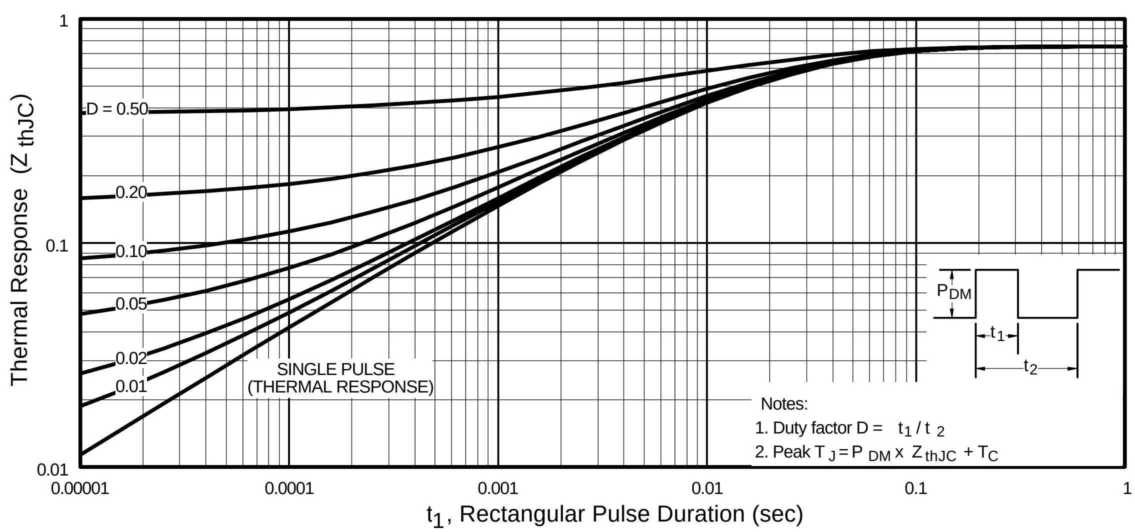


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

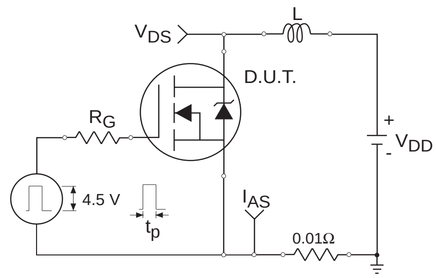


Fig 12a. Unclamped Inductive Test Circuit

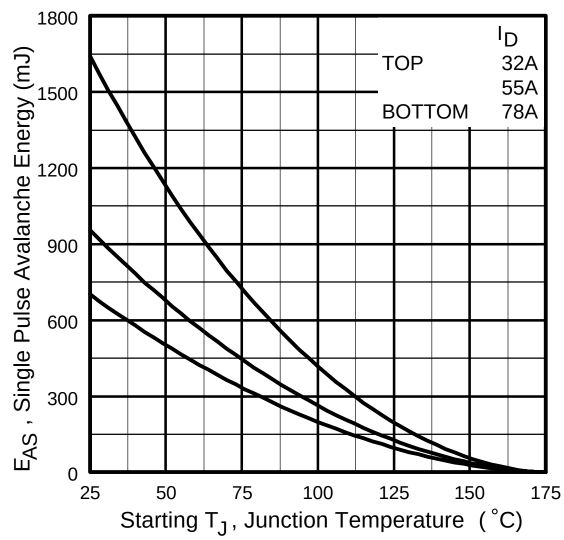


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

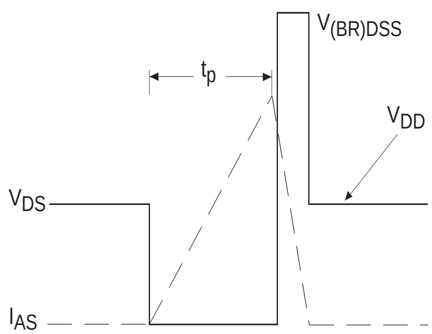


Fig 12b. Unclamped Inductive Waveforms

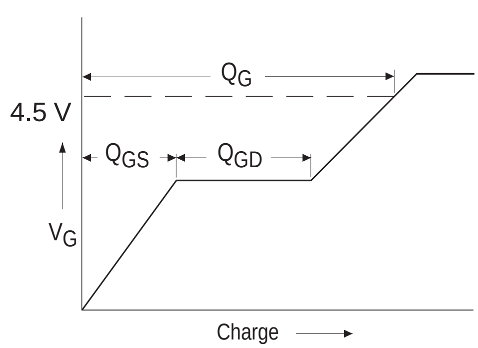


Fig 13a. Basic Gate Charge Waveform

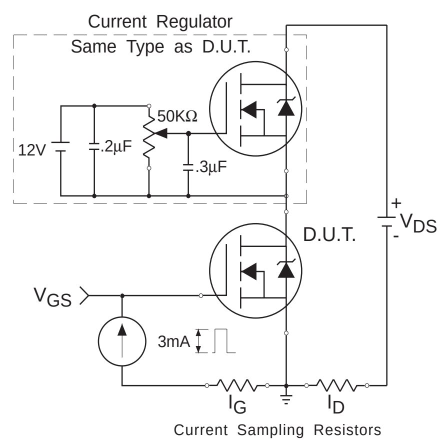
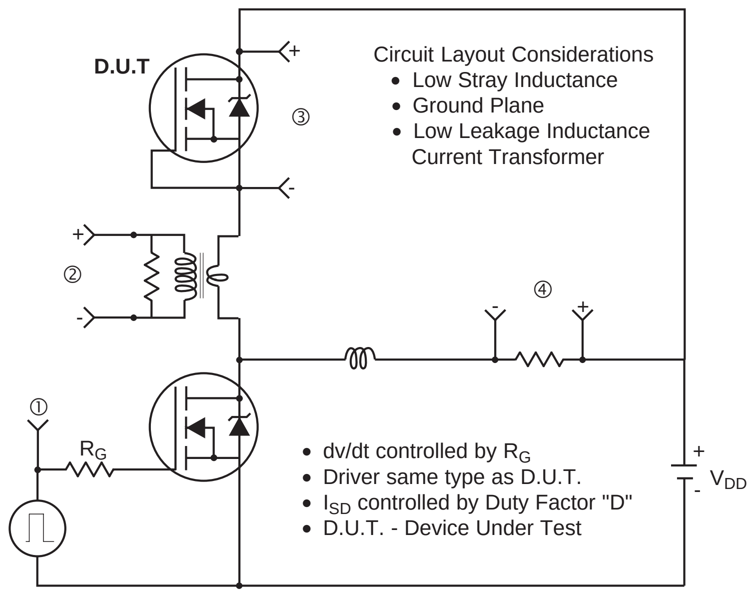
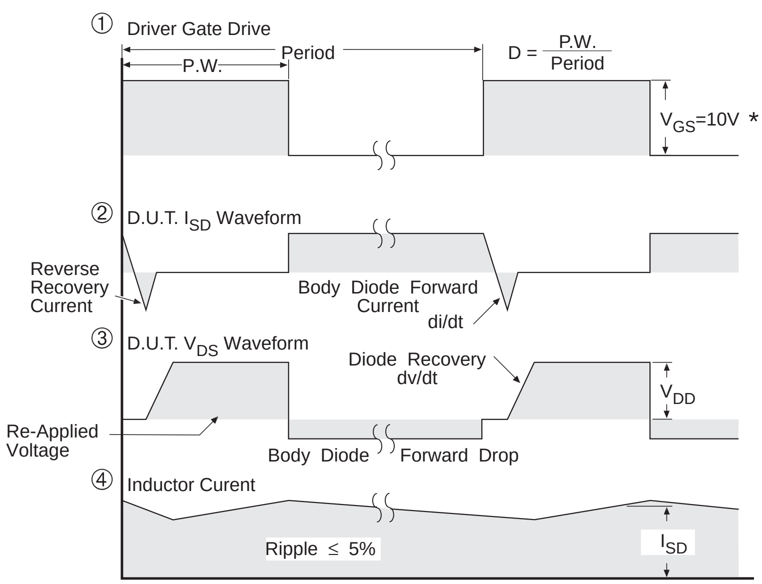


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit

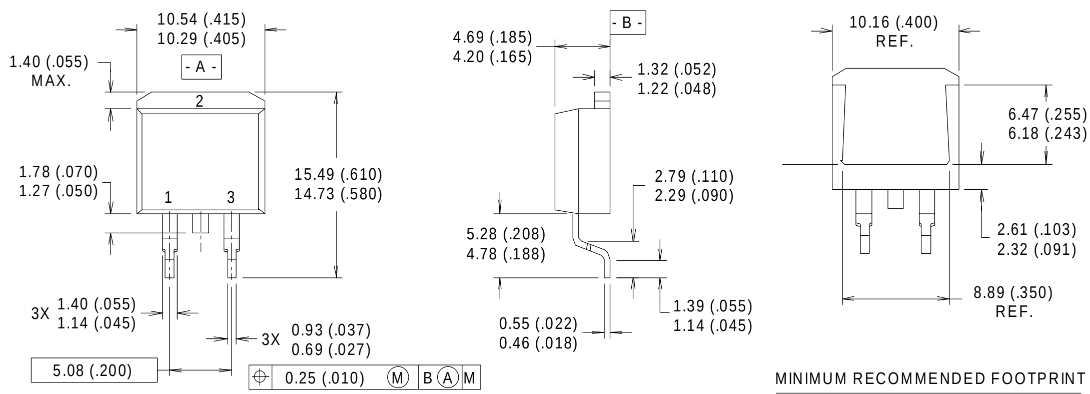




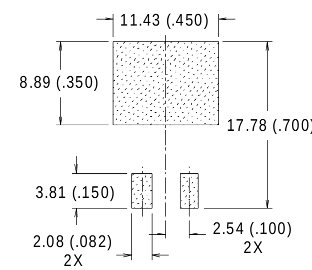
* V_{GS} = 5V for Logic Level Devices

Fig 14. For N-channel HEXFET® Power MOSFETs

D²Pak Package Outline



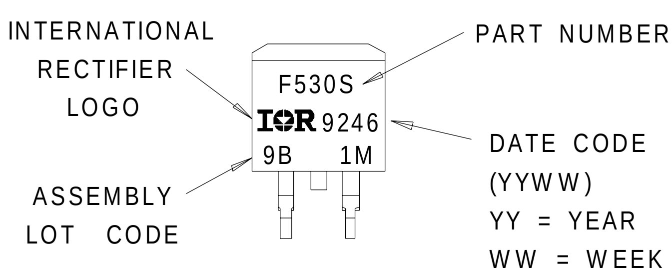
MINIMUM RECOMMENDED FOOTPRINT



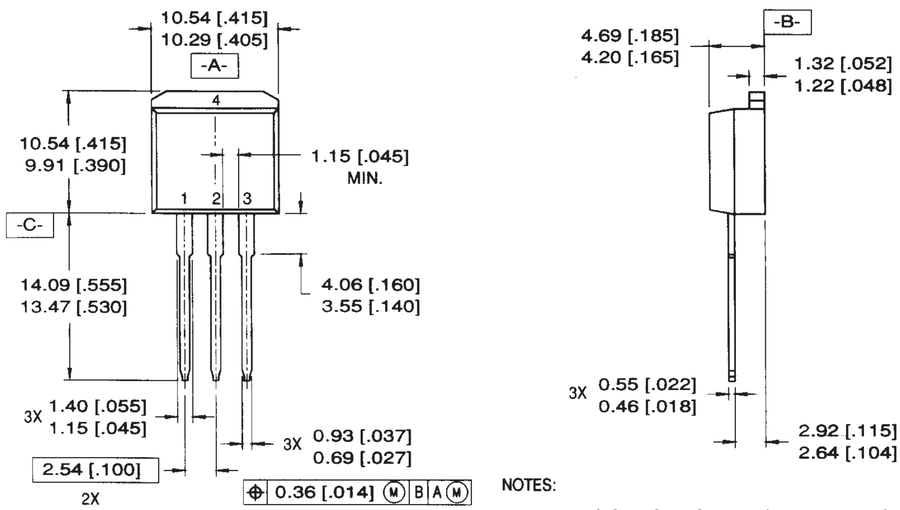
NOTES:
1 DIMENSIONS AFTER SOLDER DIP.
2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
3 CONTROLLING DIMENSION : INCH.
4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE

D²Pak Part Marking Information



TO-262 Package Outline



LEAD ASSIGNMENTS

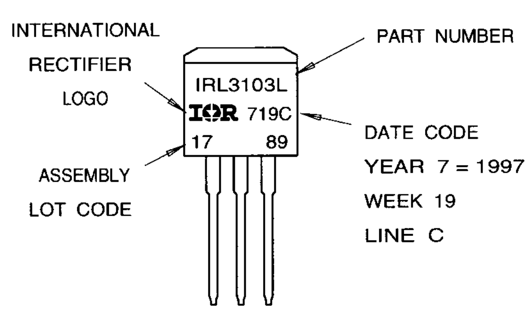
1 = GATE
2 = DRAIN
3 = SOURCE
4 = DRAIN

NOTES:

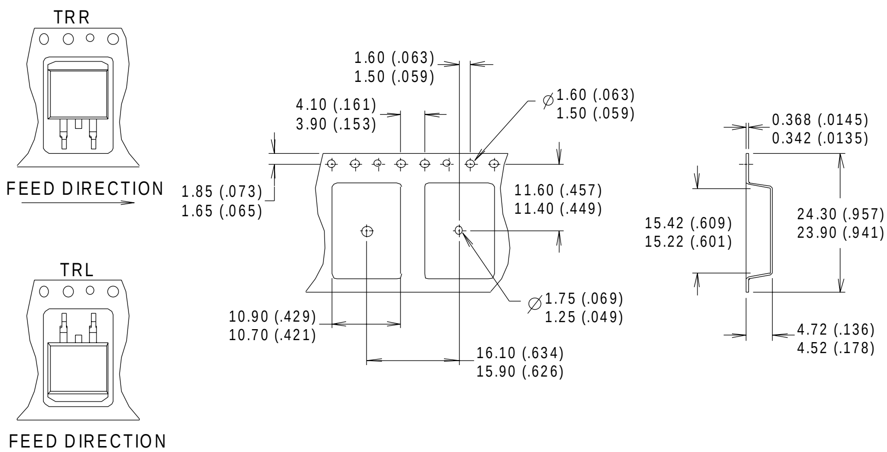
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

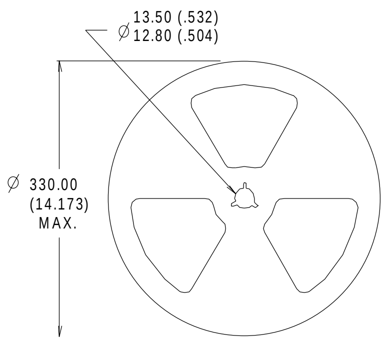
TO-262 Part Marking Information

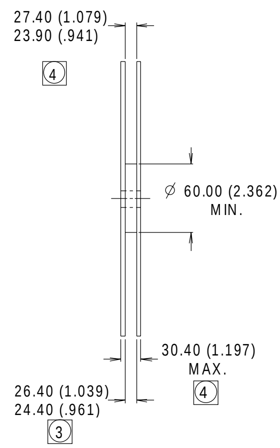
EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"



D^{2}Pak Tape & Reel Information







NOTES :
1. COMFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION MEASURED @ HUB.
4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.

International
IOR Rectifier

WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, Tel: (310) 252 7105
IR GREAT BRITAIN: Hurst Green, Oxted, Surrey RH8 9BB, UK Tel: ++ 44 1883 732020
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo Japan 171 Tel: 81 3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673, Taiwan Tel: 886-2-2377-9936

Data and specifications subject to change without notice. 12/99

Note: For the most current drawings please refer to the IR website at:
http://www.irf.com/package/