

Power-line communication dual line driver



Features

- Dual line driver suitable for differential or single-ended configuration
- Up to 18 V p-p single-ended, 36 V p-p differential output range
- · Very high linearity for EMC compliance
- Externally configurable power amplifier topology
- Up to 1.5 A_{RMS} max. current
- Embedded overtemperature protection
- Suitable for any narrow-band power-line communication (PLC) applications
- Available in QFN24 (4x4x1 mm) package
- -40 °C to +105 °C temperature range

Applications

- · Smart metering, smart grid and Internet of Things applications
- Suitable for application designs compliant with CENELEC, FCC and ARIB regulations

Description

The STLD1 line driver is a low-distortion, high-current dual power amplifier specifically designed for power-line communication applications, where high output current drives the AC power-line loads.

Operating on a single 8-18 V supply, the STLD1 can deliver high output current up to 1.5 A_{RMS} and an output voltage swing-up to 18 V peak-to-peak single-ended / 36 V peak-to-peak differential.

The STLD1 features a very low output impedance (down to 0.1 Ω in the typical configuration) to ensure efficient transfer of power to very low impedance loads, typically between 5 Ω and 100 Ω .

The device has very low in-band and out-of-band two-tone intermodulation distortion (IM3) as well as very high spurious-free dynamic range (SFDR) to guarantee and meet CENELEC, ARIB and FCC emission requirements.

It also features thermal shutdown as well as current sense output.

Product status link					
STLD1					
Order code Package Packing					
STLD1	QFN24 (4x4	Tray			
STLD1TR	x1 mm)	Tape and reel			

1 Block diagram

THERM IBIAS_IN AGND | Thermal sense IBIAS AVDD_5V 5V REG. Vbg vcc 🕆 PVCC 📋 PA2_INN PA2_OUT PA2 PA2_INP PGND 🗀 PVCC 📋 PA1_INP PA1_OUT PA1 PA1_INN PGND | CSF_OUT TX_ON_1

Figure 2. STLD1 basic block diagram

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2 Pin configuration

PGND RSV2 RSV1 PA2_OUT PA2_OUT PA2_INN **EXPOSED PAD** (BOTTOM) PA1_OUT PA2_INP PA1_OUT PA1_INP **PGND** PA1_INN AVDD_5V 3 RSV0

Figure 3. Pin connections

Table 1. Pin descriptions

Pin	Name	Description
1	PGND	Power amplifier ground
2	PA2_OUT	Power amplifier 2 output
3	FA2_001	rower ampliner 2 output
4	PA1 OUT	Power amplifier 1 output
5	FA1_001	rower ampliner i output
6	PGND	Power amplifier ground
7	PVCC	8-18 V power amplifier supply input
8	VCC	8-18 V analog supply input for 5 V internal regulator and analog circuitry.
0	VCC	It has to be externally shorted to PVCC
9	AGND	Analog ground.
	AGNE	It has to be externally shorted to PGND
10	CSF_OUT	Power amplifier current feedback output
11	AVDD 5V	5 V internal regulator output
''	AVDD_3V	Use ≥ 10 µF bypass capacitor to AGND
12	RSV0	Reserved - connect to AGND
13	PA1_INN	Power amplifier 1 negative input
14	PA1_INP	Power amplifier 1 positive input

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Pin	Name	Description
15	PA2_INP	Power amplifier 2 positive input
16	PA2_INN	Power amplifier 2 negative input
17	RSV1	Reserved - leave floating
18	RSV2	Reserved - connect to AGND
19	RSV3	Reserved - connect to AGND
20	THERM	Thermal feedback current output
21	IBIAS_IN	Reference current input
22	TX_ON_2	Enable for power amplifier 2 (active high) Force low to set PA2_OUT to Hi-Z (approx. 30 k Ω)
23	TX_ON_1	Enable for power amplifier 1 (active high) Force low to set PA1_OUT to Hi-Z (approx. 30 k Ω)
24	PVCC	Power amplifier supply input
25	Exposed pad	It has to be connected to an AGND ground plane on PCB

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3 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
PVCC, VCC	Line driver supply voltage range	PGND -0.3	20	V
AVDD_5V	5 V internal regulator voltage range	AGND -0.3	Min. (5.5, PVCC +0.3)	V
AGND - PGND	Variations between different ground pins	-0.3	+0.3	V
PA_OUT	PA output pin voltage range	PGND -0.3	Min. (20, PVCC +0.3)	V
PA_IN	PA input pin voltage range	AGND -0.3	Min. (20, VCC +0.3)	V
PA_INP - PA_INN	PA input differential voltage on the same amplifier	-11	11	V
All other pins		AGND -0.3	Min. (5.5, AVDD_5V + 0.3)	V
V(ESD)	Maximum withstanding voltage range, ANSI-ESDA- JEDEC_JS-001 human body model acceptance criteria: "normal performance"	-2	+2	kV
I(PA_OUT)	PA repetitive RMS current		1.5	Arms

Table 3. Thermal characteristics

Symbol	Parameter	Min.	Max.	Unit
Ten	Operating junction temperature		150	
$T_{(J)}$	Peak junction temperature		170	
T _{AMB}	Operating ambient temperature	-40	105	°C
T _{STG}	Storage temperature	-50	150	

Table 4. Thermal data

Symbol	Parameter	Conditions		Unit
R _{thJA}	Maximum thermal resistance junction-ambient steady-state	Mounted on a 2s2p PCB, with a dissipating surface, connected through vias, on the bottom side of the PCB	35	°C/W
Pd	Continuous power dissipation	Ta = 70 °C	2.3	W

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4 Electrical characteristics

 $T_{(AMB)}$ = -40 to +105 °C, $T_{(J)}$ < 125 °C unless otherwise specified. Typical values are at $T_{(AMB)}$ = 25 °C.

Table 5. Power supply characteristics

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V(PVCC)	Line driver supply voltage		8	15	18	V
I(PVCC)_RX	Line driver gunnly gurrent. By made	No-load on AVDD 5V		350	400	
I(VCC)_RX	Line driver supply current. Rx mode	No-load on AVDD_5V		560	850	μA
I(PVCC) TX	Line driver supply current. Tx mode, no- load	No-load on AVDD_5V. Dual power amplifier configuration		40	54	mA
I(FVCC)_1X	Line unvei supply current. 1x mode, no- load	No-load on AVDD_5V. Single power amplifier configuration		20		mA
V(PVCC)_TH	Line driver supply voltage turn-on threshold			7	7.4	V
V(PVCC)_TL	Line driver supply voltage turn-off threshold		6.1	6.5		V
V(PVCC)_HYST	Line driver supply voltage hysteresis			0.5		V
V(AVDD_5V)	5 V regulator output voltage, no-load		4.5	5.2	5.5	V

Table 6. Line driver characteristics

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V(PAx_OUT) BIAS	Power amplifier output. Bias voltage	Rx mode		PVCC/2		V
Z(PA_OUT) RX	Power amplifier output impedance in RX mode	TX_EN low		30		kΩ
V(PA_IN) BIAS	Power amplifier input. Bias voltage	Set through external resistor divider		PVCC/2		V
GBWP	Power amplifier. Gain- bandwidth product			149		MHz
t _{ON}	Power amplifier startup time	TX_EN toggled low to high (1)		1		μs
I(PA_OUT)	Power amplifier output current	Repetitive peak			1.5	A rms
V(PA_OUT) HD2	Power amplifier output. 2 nd harmonic distortion			-73		dBc
V(PAx_OUT) HD3	Power amplifier output. 3 rd harmonic distortion	VCC = 18 V, V(PA_OUT) = 13 Vpp (single-ended), R_{load} = 50 Ω , f = 100 kHz V(PA_OUT) DC = PVCC/2		-76		dBc
V(PAx_OUT) THD	Power amplifier output. Total harmonic distortion			-70		dB
V(PAx_OUT) HD2	Power amplifier output. 2 nd harmonic distortion			-57		dBc
V(PAx_OUT) HD3	Power amplifier output. 3 rd harmonic distortion	VCC = 18 V, V(PA_OUT) = 13 Vpp (single-ended), R_{load} = 50 Ω , f = 500 kHz, V(PA_OUT) DC = PVCC/2		-76		dBc
V(PAx_OUT)THD	Power amplifier output. Total harmonic distortion	, <u>-</u> ,		-54		dB

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Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C(PAx_INP),	Power amplifier input	PA_IN+ vs. AGND, see (1)		10		pF
C(PAx_INN)	capacitance	PA_IN- vs. AGND, see (1)		10		pF
PSRR	Power supply rejection	50 Hz		-100		dB
1 Sixix	ratio	1 kHz		-88		dB
CSF_RATIO	Ratio between PA_OUT and CSF output current			106		A/A
IBIAS_IN	Reference current input	Typical conditions		16 or 32		μA
		VCC = 15 V, Vout = 24 V p-p (differential), Z_{load} = 50 Ω , f1 = 50 kHz, f2 = 80 kHz (2)		-72		dB
		VCC = 15 V, Vout = 24 V p-p (differential), Z_{load} = 50 Ω , f1 = 200 kHz, f2 = 300 kHz, see $^{(2)}$		-71		dB
IM2 in hand	In band 3 rd order intermodulation distortion	VCC = 15 V, Vout = 24 V p-p (differential), Z_{load} = 50 Ω , f1 = 450 kHz, f2 = 500 kHz, see $^{(2)}$		-67		dB
IM3 in-band		VCC = 15 V, Vout = 12 V p-p (single-ended), Z_{load} = 50 Ω , f1 = 50 kHz, f2 = 80 kHz, see $^{(2)}$		-74		dB
		VCC = 15 V, Vout = 12 V p-p (single- ended), Z_{load} = 50 Ω, f1 = 200 kHz, f2 = 300 kHz, see (2)		-72		dB
		VCC = 15 V, Vout = 12 V p-p (single-ended), Z_{load} = 50 Ω , f1 = 450 kHz, f2 = 500 kHz, see $^{(2)}$		-68		dB
		VCC = 15 V, Vout = 24 V p-p (differential), Z_{load} = 50 Ω , f1 = 50 kHz, f2 = 80 kHz (2)		-71		dB
	Out-of-band third-order intermodulation distortion	VCC = 15 V, Vout = 24 V p-p (differential), Z_{load} = 50 Ω , f1 = 200 kHz, f2 = 300 kHz, see $^{(2)}$		-68		dB
IMO and of hand		VCC = 15 V, Vout = 24 V p-p (differential), Z_{load} = 50 Ω , f1 = 450 kHz, f2 = 500 kHz, see ⁽²⁾		-65		dB
IM3 out-of-band		VCC = 15 V, Vout = 12 V p-p (single-ended), Z_{load} = 50 Ω , f1 = 50 kHz, f2 = 80 kHz, see (2)		-75		dB
		VCC = 15 V, Vout = 12 V p-p (single- ended), Z_{load} = 50 Ω, f1 = 200 kHz, f2 = 300 kHz, see (2)		-73		dB
		VCC = 15 V, Vout = 12 V p-p (single-ended), Z_{load} = 50 Ω , f1 = 450 kHz, f2 = 500 kHz, see $^{(2)}$		-68		dB

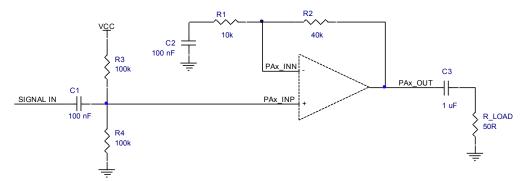
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Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
		VCC = 15 V, Vout = 24 V p-p (differential), Z_{load} = 50 Ω , f1 = 50 kHz, f2 = 80 kHz, see $^{(2)}$		71		dBc
		VCC = 15 V, Vout = 24 V p-p (differential), Zload = 50 Ω , f1 = 200 kHz, f2 = 300 kHz, see $^{(2)}$		68		dBc
SFDR	Spurious-free dynamic	VCC = 15 V, Vout = 24 V p-p (differential), Z_{load} = 50 Ω , f1 = 450 kHz, f2 = 500 kHz, see $^{(2)}$		65		dBc
SFDR	range	VCC = 15 V, Vout = 12 V p-p (single-ended), Z_{load} = 50 Ω , f1 = 50 kHz, f2 = 80 kHz, see $^{(2)}$		69		dBc
		VCC = 15 V, Vout = 12 V p-p (single-ended), Z_{load} = 50 Ω , f1 = 200 kHz, f2 = 300 kHz, see $^{(2)}$		68		dBc
		VCC = 15 V, Vout = 12 V p-p (single- ended), Z_{load} = 50 Ω , f1 = 450 kHz, f2 = 500 kHz, see $^{(2)}$		67		dBc
V(TX_ON_x) IL	TX_ON_x pin input low level voltage		AGND		0.95	V
V(TX_ON_x) IH	TX_ON_x pin input high level voltage		1.85		AVDD_5V	V
V(TX_ON_x) HYST	TX_ON_x pin input voltage hysteresis			500		mV
T1	Thermal sensor threshold see (2)			70		°C
T2	Thermal sensor threshold see (2)			100		°C
Т3	Thermal sensor threshold see (2)			125		°C
T4	Thermal sensor threshold see (2)			170		°C
T_HYST	Thermal sensor hysteresis see (2)			10		°C

- 1. Not tested in production, guaranteed by design.
- 2. Characterization data, not tested in production.

Figure 4. Line driver test circuit (single-ended configuration)



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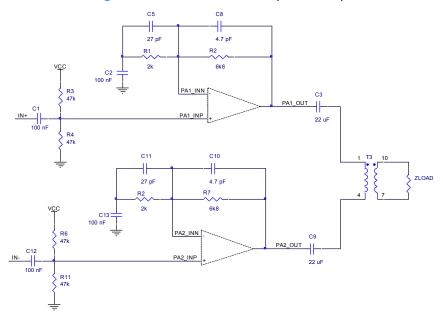


Figure 5. Line driver test circuit (differential)

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5 Device characteristics

5.1 Thermal protection

Any overtemperature event forces the line driver to self-disable the power amplifiers, thus preventing the STLD1 from damage. The thermal feedback is provided on THERM pin by a current that is N times the IBIAS_IN input current, according to the relationship described in the following table.

I(THERMAL)	Junction temperature level
0 x I(IBIAS_IN)	Tj < T1
1 x I(IBIAS_IN)	T1 < Tj < T2
2 x I(IBIAS_IN)	T2 < Tj < T3
3 x I(IBIAS_IN)	T3 < Tj < T4
4 x I(IBIAS_IN)	Tj > T4

Table 7. Thermal current level vs. junction temperature

5.2 Current feedback

Current sense feedback is provided by CSF_OUT current output, proportional to the LD output current. The CSF_OUT current is converted into voltage by a resistor and compared with the current limit threshold set at system level.

5.3 Power management

The STLD1 operates from a single 8-18 V external supply. It directly supplies the power amplifiers and the internal 5 V linear regulator for the analog and control circuitry. The block diagram for the power management is shown in the figure below.

PVCC VCC Power 8 V to amplifiers 5 V 18 V PA1_OUT AVDD 5V Linear PA2_OUT Reg. Internal circuitry AGND PĠND

Figure 6. Power supply scheme

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6.1 QFN24L (4x4x1 mm) package information

Figure 7. QFN24L (4x4 mm) package outline

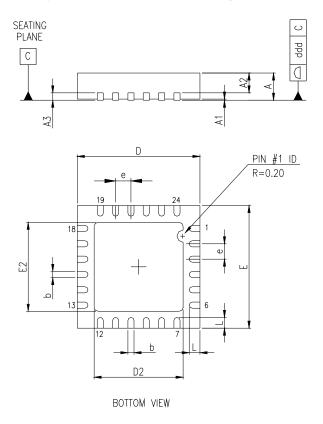


Table 8. QFN24L (4x4 mm) package mechanical data

Dim.	mm					
Dilli.	Min.	Тур.	Max.			
Α	0.80	0.90	1.00			
A1		0.02	0.05			
A2		0.65	1.00			
A3		0.20				
b	0.18	0.25	0.30			
D	3.85	4.00	4.15			
D2	2.50	2.60	2.70			
Е	3.85	4.00	4.15			
E2	2.50	2.60	2.70			
е		0.50				
L	0.35	0.40	0.45			
ddd			0.08			

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Revision history

Table 9. Document revision history

Date	Revision	Changes
25-Oct-2017	1	Initial release.
19-Jun-2018	2	Updated Section ● Device summary

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