

## 1 Introduction

This application note is intended for engineers to understand the power management system of OSD335x-SM. It is also intended to aid in power budgeting for systems using the OSD335x-SM. It provides an overview of the power management system inside the OSD335x-SM and runs through an example application power budgeting procedure.

The OSD335x-SM contains the TPS65217C Power Management Integrated Circuit(PMIC) and the TL5209 Low Drop-Out(LDO) regulator as well as all associated passives for power management. The PMIC is responsible for powering the AM335x processor and the DDR3 as well as provide output power for other system needs. It provides configurable power-up and power-down sequencing required by the processor and monitors the processor input voltage levels. The PMIC contains 3 DC-DC power converters, 2 LDOs and 2 load switches that can be configured as LDOs that can be used as power supplies. It can be powered by any combination of a 5V AC adapter, USB port, or Single Cell Li-Ion battery. Figure 1 shows the power system of OSD335x-SM including connections between the PMIC and various power domains of the processor.





The OSD335x-SM allows the I/O voltage domains (VDDSHVx) of the AM335x to be set to either 1.8V or 3.3V. The VDDSHVx pins of the OSD335x-SM (ie VDDSHV1 thru VDDSHV6), which can be found in Table 5.5, must be connected to either a 1.8V or 3.3V power source in order to provide power to the I/Os. Recommendations on how to connect the I/O voltage domain pins is in the OSD335x-SM Layout Guide in the Reference Documents section. See the AM335x datasheet in the Reference Documents section for more information on the pins associated with each I/O voltage domain.



<u>Table 1</u> shows the voltage output levels of each of the voltage sources. Each of the output voltages can be changed dynamically using I2C commands when the PMIC is in active mode.

Table 1 PMIC voltage outputs					
TPS65217C Voltage Source	OSD335x Voltage rail	Voltage (V)			
DCDC1	VDDS_DDR	1.5			
DCDC2	VDD_MPU	1.1			
DCDC3	VDD_CORE	1.1			
LDO1	SYS_RTC_1P8V	1.8			
LDO2	SYS_VDD2_3P3V	3.3			
LDO3	SYS_VDD_1P8V	1.8			
LDO4	SYS_VDD3_3P3V	3.3			





## Table of Contents

1	l	ntroduo	ction	1
2	R	Revision	1 History	4
3	Ρ	ower L	Jp Sequence	5
3.	1 A	ddition	al functions of the PMIC	6
4	Ρ	Power B	Budgeting: How to Approach it?	6
	4.1	1 Step	ס 1: Creating a Power Diagram	6
	4.2	2 Step	o 2: Creating a Power Budget	8
		4.2.1	Maximum Power	8
		4.2.2	Refining the Power Budget	14
	4.3	3 Step	o 3: Tally Up	16
5	C	Conclusi	ion	17
6	R	Referen	ce Documents	17



## 2 Revision History

Revision Number Revision Date		Changes	Author
1	10/24/2017	Initial Release	Neeraj Dantu

<u>Notice</u>: The information provided within this document is for informational use only. Octavo Systems provides no guarantees or warranty to the information contained.



### 3 Power Up Sequence

The power-up sequence of the processor is shown below in <u>Figure 2</u>, with the numbers in red representing the order in which they come up, and the main power up events are described below:



Figure 2: AM335x + PMIC power up sequence for OSD335x-SM

- 1. SYS\_RTC\_1P8V is activated.
- PMIC\_OUT\_LDO\_PGOOD rail which is connected externally to the processor's RTC\_PWRONRSTN (Power on reset of RTC domain) is pulled high to indicate presence of right voltages for the RTC domain of the processor to power-up.
- RTC circuitry in the processor comes up and pulls the PMIC\_IN\_PWR\_EN signal high instructing the PMIC to start power-up sequence. The output of DCDC1 (VDDS\_DDR) which powers the DDR memory is also activated.
- 4. Output of LDO3 (SYS\_VDD\_1P8V) is activated
- 5. Output of LDO2 (SYS\_VDD2\_3P3V) is activated
- 6. Output of LDO4 (SYS\_VDD3\_3P3V) is activated
- 7. Outputs of DCDC2 (VDD\_MPU) and DCDC3 (VDD\_CORE) are activated
- 8. PMIC\_OUT\_PGOOD which is connected externally to the processor's PWRONRSTN (Power on reset of AM335x) of the processor is pulled high releasing the processor from reset.

5

Octavo Systems LLC Copyright 2018



This power up sequence and delays between each step of the sequence are already programmed into the PMIC inside the OSD335x so you don't need to worry about it. The power-down sequence follows the reverse order of the power-up sequence.

## 3.1 Additional functions of the PMIC

The PMIC also performs some tertiary functions. A few of the key functions are listed below. For a complete explanation of all the functions provided by the TPS65217C PMIC refer to the datasheet.

- 1. The PMIC retrieves the processor from OFF or SLEEP mode upon detecting a falling edge on PMIC\_IN\_PB\_IN. It also power cycles the processor if PMIC\_IN\_PB\_IN is held low for more than 8 seconds.
- 2. It provides an active low wake up signal (PMIC OUT NWAKEUP) which is de-asserted when a wakeup event is detected.
- 3. The PMIC has an interrupt pin (PMIC\_OUT\_NINT) to signal an event or fault condition to the processor. The pin is released when the processor reads the INT register.
- PMIC provides a linear charger for Single Cell Li-Ion batteries and allows charging of the battery and powering of the system at the same More information can be obtained from the datasheet.
- 5. The TPS65217C provides protection to the AM335x and itself in the event of catastrophic situations like an unexpected short or excessive current leakage.
- 6. It monitors the functioning of a battery if one is connected and charges the battery when possible.

Now that the function and of the PMIC and its relationship with the processor is clear, the process of power budgeting discussed below can be better understood.

#### Power Budgeting: How to Approach it? 4

It is a good practice to make a power budget for your product/design at the beginning of the project. Good power budgeting contributes to circuit robustness, increased product life and reduced cost of the product. A power budget should include the availability of power, operating temperature, amount of data collected, communication, and operation modes of the processor.

## 4.1 Step 1: Creating a Power Diagram

The first step in making a power budget is to have a power diagram that shows all the power paths of the system. Start with all the available power sources for the system. For OSD335x, this would include power rails that are described in the datasheet as output power supplies. There are six output power rails on the OSD335x including a 2.75V – 5.5 output (SYS VOUT), three 3.3V outputs (SYS VDD1 3P3V, SYS\_VDD2\_3P3V and SYS\_VDD3\_3P3V) and three 1.8V outputs (SYS\_RTC\_1P8V, SYS\_VDD\_1P8V and SYS ADC 1P8V).

### Perk:

Range of SYS\_VOUT is determined by input power supply voltage. For example, if the SiP is being powered through a battery (VIN BAT), SYS VOUT can be 2.75 V - 5.5 V depending on the battery voltage. Due to the dropout behavior of the LDO TL5209, its output voltage rail SYS VDD1 3P3V should not be used when the OSD335x is being powered through VIN BAT. Please refer to the TL5209 datasheet for details.





Next, put in the power consuming components and connect them to the appropriate power rail. The connection should be based on the voltage input level for the component. Current supply capacities of the power rails and ease of use can also be factors for choosing the best power rail for the component. In order to understand this process, let us use the OSD3358-SM-RED Platform. The board provides access to many peripherals of OSD335x-SM and has a number of external components powered by the OSD335x-SM. Figure 3 shows the completed power system diagram for the design. It shows most of the components that draw at least a nominal amount of power.

The diagram not only shows the power rail for a particular component but also lists all the components that are being powered by a power rail. In addition to helping with the power budgeting, this allows you to identify power issues early in the design process and make necessary adjustments.



Figure 3: OSD3358-SM-RED power system diagram



### 4.2 Step 2: Creating a Power Budget

The next step involves making a power budget to estimate power consumption of each component and thus the total power consumption of the board.

### 4.2.1 Maximum Power

There are several challenges involved in accurately estimating the power consumption of each component. For example, it is difficult to estimate how much current, the AM3358 processor and the DDR Memory draw since that is highly application specific. Power consumption will also depend on the presence of a USB device or a Micro SD card. To account for all situations, we can start out by assuming maximum power consumption for all the components. <u>Table 2</u> shows the power budget table for OSD3358-SM-RED assuming maximum power consumption for each component.

Part Name Part Number Max Current (mA) Supply vo		Supply voltage	rail Voltage (V)	Max Power (mW)	
AM3358	U1	307.8	Internal	5	1539
TPS65217C	U1	< 1	Internal	5	<5
TL5209	U1	25	Internal	5	125
DDR RAM	U1	339	Internal	1.5	508.5
TPS2051	U15	< 1	SYS_VOUT	5	< 5
USB Connectors	X4, X5	< 500	SYS_VOUT	5	< 2500
24LC32AT	U1	3	Internal	3.3	15
APX811	U4	20	SYS_VDD1_3P3V	3.3	66
USB2534-1080AEN	U8	80	SYS_VDD1_3P3V	3.3	264
ASDMB-12.000MHZ	Y3	15	SYS_VDD1_3P3V	3.3	49.5
ASDMB-24.576MHz	Y5	15	SYS_VDD1_3P3V	3.3	75
DM3BT-DSF-PEJS	Х3	200	SYS_VDD1_3P3V	3.3	1000
SDIN8DE2-16G	U7	80	SYS_VDD1_3P3V	3.3	400
SN74LVC1G07DCK	U3	24	SYS_VDD1_3P3V	3.3	120
SN74LVC2G241DCUR	U6	24	SYS_VDD1_3P3V	3.3	120
AR8035-AL1A	U9	128	SYS_VDD1_3P3V	3.3	422.4
TDA19988BHN	U10	77	SYS_VDD_1P8V	1.8	385
MPU-9250	U23	3.7	SYS_VDD1_3P3V	3.3	12.21
TMP468	U17	10	SYS_VDD1_3P3V	3.3	33
BMP280	U22	1	SYS_VDD1_3P3V	3.3	3.3
S25FL127S	U21	50	SYS_VDD1_3P3V	3.3	165
AT97SC3205T	U16	25	SYS_VDD1_3p3V	3.3	82.5
				Total	~7895

Table 2: Power budget table with maximum power consumption

\*\*SDIN8DE2-16G datasheet is not available on the internet. So, an equivalent <u>datasheet</u> was used to determine current consumption

\*\*AT97SC3205T datasheet does not specify current consumption. So, an equivalent datasheet was used

Maximum current consumption values can be found from the component datasheets for most devices. However, there is no deterministic way of calculating the current consumed by the AM335x and the DDR3 as they are highly application specific. The next two sections will explore how to use tools provided by TI and Micron to estimate the max power used by the AM335x and DDR.



### 4.2.1.1 Using Power Estimation Tool for estimating AM3358 power consumption

Texas Instruments provides access to a power estimation tool that can calculate the internal power consumption of AM3358 including individual power domains of the processor. The process involves filling out a spreadsheet and submitting it to a webpage. The detailed procedure is described in the wiki page "<u>AM335x Power Estimation Tool</u>". A short overview of the process with notes on usage with the OSD335x is given below. The inputs shown in the screenshots were put in to calculate the maximum power consumption of AM335x.

- 1. Download either the simplified or the advanced spreadsheet for AM335x from http://www.ti.com/tool/powerest
- 2. In section A, among other inputs, set the device revision to PG2.1, DDR type to , DDR loading to 1, and all the VDDSHVx voltages to 3.3. The power modes of AM335x are discussed later in this document.

Device Revision	PG2.1
DDR Type	DDR3L
DDR Loading	1
Junction Temperature (°C)	40
Power Estimation Mode	Max
Smart Reflex	off
VDDSHV1 Voltage [V]	3.3
VDDSHV2 Voltage [V]	3.3
VDDSHV3 Voltage [V]	3.3
VDDSHV4 Voltage [V]	3.3
VDDSHV5 Voltage [V]	3.3
VDDSHV6 Voltage [V]	3.3

## A) High-Level System Configuration

Figure 4: System configuration in power estimation spreadsheet



3. Set the Operational Performance Point (OPP), MPU frequency and Utilization percentages in Section B.

**B) Processors** 

OPP	Slot 0
CORE OPP	OPP100
MPU OPP	NITRO
MPU Frequency (Mhz)	1000

ARM Sub-system	Slot 0	
ARM Sub-system	Utilization %	
Cortex-A8	100	
Cortex-A8 NEON	100	

SGX Sub-system (For SGX-	Slot 0
enabled devices only)	Utilization %
SGX	100

Figure 5: Processor options and utilization in power estimation spreadsheet

4. Input Utilization percentages for peripheral usage of AM335x in section C.



## C) Peripherals

Module Name	Slot 0		
Module Name	Utilization %		
EDMA	100		
EMIF	100		
GPMC	100		
OCMC-RAM	100		
LCDC	100		
USB	100		
Ethernet MAC	100		
PRUSS	100		
McASP1	100		
McASP2	100		
MMC1	100		
MMC2	100		
MMC3	100		
Misc. Peripherals (UART, SPI, I2C, CAN, GPIO, eHRPWM, eQEP, RTC etc)	100		

Figure 6: Peripheral utilization in power estimation spreadsheet

5. Enable/Disable analog modules in Section D

## D) Analog Modules

Module Name	Slot 0
ADC	On

Figure 7: ADC module usage in power estimation spreadsheet

- 6. Click on the submit button in the spreadsheet. This will open a webpage to which the edited spreadsheet can be uploaded to. This requires logging in to TI's website.
- 7. A power analysis report will be emailed to the email address attached to the user account logged into.



# OSD335x-SM Power Application Note

Rev.1 10/24/2017

AM335x Power Estimation Report						
Input File Name:	am335x_pet_in	out_adv.xls				
Junction Temperature (°C):	40					
Device Process:	strong					
ARM Clock Freq [MHz]	NITRO(1000)					
	Volta			0		Downer 040
		ge(V)	Laskass	Current(A)	A	Power (W
VOD MOU	min	max	Leakage	Active	Average	Total
VDD_MPU	1.33	1.33	0.020	0.678	0.698	0.92802
VDD_CORE	1.10	1.10	0.019	0.471	0.490	0.53893
VDDS_DPLL	1.80	1.80	0.000	0.013	0.013	0.02342
VDDS_SRAM	1.80	1.80	0.006	0.000	0.006	0.00997
VDDS_DDR	1.35	1.35	0.000	0.003	0.003	0.00576
VDDS_1P8	1.80	1.80	0.000	0.008	0.008	0.01390
VDDS_3P3	3.30	3.30	0.000	0.005	0.005	0.01776
VDDA1P8V_USB0/1, VDDA_ADC	1.80	1.80	0.000	0.000	0.000	0.00090
VDDA3P3V_USB0/1	3.30	3.30	0.000	0.000	0.000	0.00000
Total						1.53867
Notes :						
VDDS_DPLL includes VDDS_PLL_MPU, VDDS_PL	L_CORE_LC	D and VDD	S_PLL_DDR	power sup	plies	
VDDS_SRAM includes VDDS_SRAM_CORE_BG a	nd VDDS_SR	AM_MPU_	BB powre s	upplies		
VDDS_1P8 includes VDDS, VDDS_RTC, VDDS_OS	C and 1.8 V	VDDSHVx	power suppl	ies		
VDDS_3P3 includes 3.3 V VDDSHVx power suppl	ies					

Figure 8: Power estimation result

The worst-case current consumption can be obtained by maximizing the inputs to the spreadsheet. Other relevant resources that help estimation of AM335x power usage are given below:

- 1. <u>Processor SDK Linux kernel performance guide</u>
- 2. AM335x power consumption summary

#### 4.2.1.2 Estimating Power for the DDR3

Like the AM335x spreadsheet, Micron provides a spreadsheet to estimate DDR3L power consumption. Though the exact power consumption depends on the part number of the memory, the spreadsheet serves as a ball park estimation tool. A brief use case of the spreadsheet is shown below.

1. Download the spreadsheet available for the DDR3L memory on Micron's website.



2. Input SDRAM configuration inputs in the *"DDR3 Config"* The screenshot shows inputs specific to DDR3 memory used in OSD335x.

DRAM Density	4Gb	•
Number of DQs per DRAM	x8	-
Speed Grade	-125	-
Mode Register bit 12: Precharge PD Exit Mode	0:Slow	-

*Figure 9: DDR3 configuration in power estimation spreadsheet* 

3. Input DRAM usage conditions in *"System Config"* These inputs may vary based on use case. The inputs shown below are for estimating worst case power consumption of the RAM.

	System VDD	1.435	V
	System CK frequency	400	MHz
	Burst length	8	
PdqRD	DDR3 SDRAM output power per individual DQ on this DRAM during READs from this DRAM	5.0	mW
PdqWR	DDR3 SDRAM termination power per individual DQ during WRITEs to this DRAM	18.9	mW
PdqRDoth	DDR3 SDRAM termination power per individual DQ during READs from other DRAM	27.2	mW
PdqWRoth	DDR3 SDRAM termination power per individual DQ during WRITEs to other DRAM	27.4	mW
BNK_PRE%	The percentage of time that all banks on the DRAM are in a precharged state	0%	
CKE_LO_PRE%	The percentage of the all bank precharge time for which CKE is held LOW	0%	
CKE_LO_ACT%	The percentage of the at least one bank active time for which CKE is held LOW	0%	
PH%	Page hit rate	0%	
RDsch%	The percentage of clock cycles which are outputting read data from the DRAM	0%	
WRsch%	The percentage of clock cycles which are inputting write data to the DRAM	100%	
811		0%	
termRDsch%	The percentage of clock cycles which are terminating read data to another DRAM	0%	
termWRsch%	The percentage of clock cycles which are terminating write data to another DRAM	0%	
<sup>t</sup> RRDsch	The average time between ACT commands to this DRAM (includes ACT to same or different banks in the same DRAM device)	8.0	ns

Figure 10: DDR3 system configuration in power estimation spreadsheet



4. The "Summary" page will show the power consumption summary for previously entered inputs.

Psys Power Consumption Summary			
ACT	182.1	mW	
Total Activate Power	182.1	mW	
RD	0.0	mW	
WR	70.3	mW	
READ I/O	0.0	mW	
Write ODT	207.6	mW	
Total RD/WR/Term Power	277.9	mW	
ACT_STBY	40.9	mW	
PRE_STBY	0.0	mW	
ACT_PDN	0.0	mW	
PRE_PDN	0.0	mW	
REF	7.6	mW	
Total Background Power	48.5	mW	
Total DDR3 SDRAM Power	508.5	mW	
TERM 2nd rank	0.0	mW	

## Dava Dawar Consumption Summa

*Figure 11: DDR3 power consumption summary* 

From the results, the worst case current consumption was calculated to be 339 mA with 1.5 V input

#### 4.2.2 Refining the Power Budget

Some of the current consumption numbers are highly unrealistic. No system uses all the processor cores and peripherals at a 100% utilization. The DDR current consumption is calculated assuming 100% of the time is spent writing to the memory with lowest ACT command interval. So, while it is safe to use these figures to assume worst case load, the system would be vastly over-designed. It is better to build a second power budget table with typical current consumptions and a more application specific scenario while keeping the previous version in mind.



Part Name	Part Number	Max Current (mA)	Supply voltage	rail Voltage (V)	Max Power (mW)
AM3358	U1	186.4	Internal	5	932
TPS65217C	U1	< 1	Internal	5	<5
TL5209	U1	8	Internal	5	125
DDR RAM	U1	206	Internal	1.5	309
TPS2051	U8	< 1	SYS_VOUT	5	< 5
USB2534-1080AEN	U8	45	SYS_VDD1_3P3V	3.3	148.5
USB Connector	X4, X5	< 500	SYS_VOUT	5	< 2500
24LC32AT	U1	1	Intenal	3.3	5
DM3BT-DSF-PEJS	Х3	100	SYS_VDD1_3P3V	3.3	500
SDIN8DE2-16G	U7	80	SYS_VDD1_3P3V	3.3	400
SN74LVC1G07DCK	U3	16	SYS_VDD1_3P3V	3.3	80
SN74LVC2G241DCUR	U6	16	SYS_VDD1_3P3V	3.3	80
AR8035-AL1A	U9	33.9	SYS_VDD1_3P3V	3.3	111.8
MPU-9250	U23	3.2	SYS_VDD1_3P3V	3.3	10.6
S25FL127S	U21	24	SYS_VDD1_3P3V	3.3	79.2
Total					5291

Table 3 Application specific power budget table

<u>Table 3</u> shows an application specific power budget table in which the processor is operated in conditions described in <u>Table 4</u>. All the other peripherals and features are assumed to be disabled in this scenario and 'typical' current consumption values from component datasheets are used rather than 'maximum' current consumption values.

Table 4 AM335x application specific operating conditions			
Feature/peripheral	Utilization (%)		
Cortex A8	70		
Cortex A8 NEON	70		
CORE OPP	OPP100		
MPU OPP	NITRO		
MPU Frequency	1 GHz		
EMIF	70		
OCMC RAM	70		
USB	70		
Ethernet MAC	70		
MMC1	70		
Miscellaneous Peripherals	50		
ADC	OFF		

Note that the utilization percentages of each feature/peripheral of the AM335x processor are still high. This is done to leave ourselves some head room if the board runs into an unexpected scenario. Similarly, the RAM usage is also safely assumed to have a 20% page hit rate, a 10ns interval between ACT commands, 30% of the time spent reading from RAM and 30% of the time writing to the RAM. Also, observe that several components of the board are not in use and so are left out of <u>Table 3</u>.

## OSD335x-SM Power Application Note



Rev.1 10/24/2017

## 4.3 Step 3: Tally Up

Thus, we have an extreme scenario and an application specific application scenario for our power budget. The usage scenarios should now be stacked up to the supply capacities of output power rails of OSD335x that we outlined in step 1 to make sure everything checks out. Given below are the conditions that need to be verified and corresponding usage on the OSD3358 SBC reference design from the datasheet:

Table 5 Current limitations from OSD335x datasheet

Condition	Limitation	Extreme	Application		
VIN_AC input current	2.0 A	1.58 A	1.05 A		
VIN_USB input current* (See below)	1.3 A	1.58 A	1.05 A		
VIN_BAT input current (5V battery)	2.0 A	1.58 A	1.05 A		
SYS_VOUT output current	500 mA	500mA	500mA		
SYS_VDD1_3P3V (VDD_3V3B) output current	500 mA	752.7mA	318.1mA		
SYS_VDD2_3P3V (VDD_3V3AUX) output current	150 mA	_	-		
SYS_RTC_1P8V (VDD_RTC) output current	100 mA	_	_		
SYS_VDD_1P8V (VDD_1V8) output current	250 mA	77mA	_		
SYS_ADC_1P8V (VDD_ADC) output current	25 mA	_	_		

#### Perk:

By default, VIN\_USB is limited to 500mA. A current limiting register in the PMIC needs to be modified to allow current greater than 500mA. Another important thing to keep in mind is the type of components used for power supply. While the MPU domain, CORE domain and the DDR memory are powered by efficient DC to DC converters, all the other power rails come from LDOs. So, current consumption of the components powered by LDOs is a direct addition to the overall current consumption irrespective of the level of the voltage rail.

From Table 5, although SYS\_VOUT current consumption looks like it touches the maximum recommended output current, it is highly unlikely to have a USB device that would draw 500mA in the application. The extreme condition input current exceeds the USB input current limit. But, there are alternative input power paths(AC and BAT) that can mitigate this issue even though the scenario will never occur. The load current for the SYS\_VDD1\_3P3V voltage rail also exceeds the output current limit in the extreme scenario. So, that voltage rail may fail if components begin to draw maximum specified currents. But, the application specific current draws taken into account while designing the board are significantly lower than the limits. More weight was placed on the application scenario vs theoretical maximum current consumptions during the design. As can be seen from Table 5, there is enough room for the board to be able to deal with most unexpected situations of high current consumption in an application scenario.

While this board presents no problems in power analysis for an application, there might be situations where the current draws are close or exceed the power rail limits in a design. In this case, alternative approaches to design can solve the problem. The OSD335x has multiple rails of 1.8V and 3.3V. So, spreading out the total current consumption of all the parts among the available power rails can be a

16



first approach. If that does not resolve the issue, alternative power paths need to be designed. This might involve using more regulators and/or using AC/BAT input instead of the current limiting USB input.

## 5 Conclusion

This document discussed the power management system of OSD335x-SM and presented a power budgeting procedure that helps in efficient product design. Most of the above discussion centers around hardware. However, software also plays an important role in power management. Some aspects of software power management and a case study on its advantages are presented in the application note: <u>Software Power Management with the OSD335x Family</u>.

## 6 Reference Documents

- 1. TPS65217C datasheet
- 2. TL5209 LDO datasheet
- 3. AM335x datasheet
- 4. Powering the AM335x with TPS65217C
- 5. Using Power Estimation Tool to estimate power consumption of AM335x
- 6. <u>Processor SDK Linux kernel performance guide</u>
- 7. AM335x power consumption summary
- 8. Spreadsheet for DDR3 power consumption estimation
- 9. AM335x Power Management User Guide
- 10. Linux Core Power Management User's guide
- 11. AM335x Power Management User Guide
- 12. AM335x Power Management Standby User's Guide