		PRODUCTS	· · · · ·		TYPE				PAGE	(
	CHM	Semiconductor IC			BDec)69GU	т		1/4	
		00					0900	l	<u> </u>	1/4
	Structure	Sili	Silicon Monolithic Integrated Circuit							
	Product Name	Sy	Synchronous rectification step-up DC/DC converter for mobile phone							
	Туре	В	BD6069GUT							
	Features Synchronous rectification step-up DC/DC converter No external schottky diode required									
	OAbsolute Maximum F	Ratinos (Ta=	25°C)							
	Parameter		iymbol		Rating		Unit	Conditio		
	Maximum applied volta		MAX1		7(*1)		V	VIN, EN, VFB, T		
	Maximum applied volta		MAX2		20(*1)		V	SW, VOUT		
	Power dissipation		Pd		800(*2)		mW			
	Operating temperature		Topr	-	-30 to +85		°C			
	Storage temperature ra (*1) These values are		Tstg		55 to +150)	°C			
	(*2) This value is the r (50mm×58mm× Temperature dele	1.75mm gla ting: 6.4mW	ss epoxy / °C from	Board) Ta>25°C		the PCB by	/ ROHM			
	Parameter		umbol		Rating		l la it	Q a ra di ti a		
	Parameter	3	ymbol	Min.	Тур.	Max.	Unit	Conditio	n	
	Supply voltage	Vin 2.7 3.6 5.5 V								
	This product isn't designed to protect itself against radioactive rays. Status of this document The English version of this document is the formal specification. A customer may use this translation version only for a reference to help reading the formal version. If there are any differences in translation version of this document,formal version takes priority.									
 ROHM The prooffice- Should would control ROHM 	ion example I cannot provide adequate cr roduct described in this spe automation equipment, com d you intend to use this pro- directly endanger human li ollers and other safety device I assumes no responsibility sentations that the circuits a	ecification is de munications d oduct with equi fe (such as me es), please be s / for use of ar re free from pa	esigned to evices, ele- pment or o dical instru- sure to con ny circuits	ctrical applian devices which uments, trans sult with our described he	nces, and el h require an portation ec sales repres	ectronic toys) extremely hi juipment, aer entative in ac). igh level (ospace m dvance.	of reliability and the ma achinery, nuclear-react	Ifunction of or controlle	f which rs, fuel
	IGN СНЕСК aki Којі i <i>Taniuch</i> í r. 2006 27. Nar. 2006	APPROVAL	DATE	: 27/Mar/2	2006 SP	ECIFICATIO	NNO.:	TSZ02201-BD6	069GUT	-1-2
	.r. 2006 27. Mar. 2006 111.04	27 Mar 20	REV.	В			ROH	M CO., LTD.		

		 _
R	h	

TYPE

OElectrical Characteristics

ſ

(Unless otherwise noted, Ta = -30 to +85 $^{\circ}$ C, Vin=3.6V)

Parameter	Symbol	Spec			Unit	Condition
Parameter	Symbol	Min.	Тур.	Max.	Unit	Condition
EN Terminal		F	1			T
EN Low threshold voltage	VthL	-	_	0.4	v	
EN High threshold voltage	VthH	1.4	-	-	V	
EN Input current	lin	-	18.3	30.0	μA	EN=5.5V
EN Output current	lout	-2.0	-0.1	-	μA	EN=0
Switching Regulator				·····		
Input voltage range	Vin	3.1	-	5.5	V	
Quiescent Current	lq	-	0.1	2.0	μA	EN=0V
Current Consumption	ldd	-	1.1	1.5	mA	EN=2.6V,VFB=1.0V,VIN=3.6V
Feedback voltage	Vfb	0.47	0.50	0.53	v	
Inductor current limit	Icoil	270	350	430	mA	Vin=3.6V (*1)
SW saturation voltage	Vsat	-	0.14	0.28	v	Isw=200mA,Vin=3.6V
SW on resistance P	Ronp	-	2.1	3.2	Ω	lpch=200mA,Vout=13V
Switching frequency	fSW	0.8	1.0	1.2	MHz	
Duty cycle limit	Duty	82.7	85.0	-	%	VFB=0V
Output voltage range	Vo	-	-	18.0	v	
Over voltage limit	Ovl	18.0	18.5	19.0	v	VFB=0V
Start up time	Ts	-	0.5	1.0	ms	

*1. This parameter is tested with dc measurement.

REV. :

PRODUCTS	ТҮРЕ	PAGE
Semiconductor IC	BD6069GUT	3/4

OExternal dimensions



OTerminals

BALL Name
GNDA
EN
TEST
VIN
VFB
VOUT
SW
GND

VCSP60N1(8Pin) (Unit:mm)



O Cautions on use

RDHM

(1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Power supply and GND line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. Pav attention to the interference by common impedance of layout pattern when there are plural power supplies and GND lines. Especially, when there are GND pattern for small signal and GND pattern for large current included the external circuits, please separate each GND pattern. Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use a capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(3) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(4) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(5) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(6) Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(7) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

(8) Thermal shutdown circuit (TSD)

When junction temperatures become 175°C (typ) or higher, the thermal shutdown circuit operates and turns a switch OFF. The thermal shutdown circuit, which is aimed at isolating the LSI from thermal runaway as much as possible, is not aimed at the protection or guarantee of the LSI. Therefore, do not continuously use the LSI with this circuit operating or use the LSI assuming its operation.

(9) Thermal design

Perform thermal design in which there are adequate margins by taking into account the permissible dissipation (Pd) in actual states of use.

(10) DC/DC converter

Please select the low DCR inductors to decrease power loss for DC/DC converter.

ROHM CO., LTD.

REV. :

RDHM PRODUCTS Semi	conductor	Jisso Information for BD6069GUT	PAGE 1∕4
— Jisso Info	rmation —		
<u> Package : V</u>	CSP60N1		
 A table of contents > 1. Structure and materials 2. Tape and Reel information 3. Storage conditions 4. Marking lot number 5. Recommended soldering 6. Footprint dimensions 7. Regarding the underfill m 8. External dimensions 	ons conditions	3/4 page 3/4 page 3/4 page 3/4 page 4/4 page 4/4 page	

1. Structure and materials



No.	İtem	Materials
1	Die	Silicon
2	Cu Layer	Cu
3	Cu Post	Cu
4	Encapsulation	Epoxy Resin
5	Ext. terminal	Sn-3Ag-0.5Cu Solder
6	Encapsulation	Polyamide-imide Resin
\bigcirc	Marking	Laser Marking

Dehydrated weight : 0.003g



Таре	Embossed carrier tape
Quantity	3,000pcs/Reel
Direction of feed	E2 (See Fig. 2)

- 2. 2. Tape and Reel specification
- 2. 2. 1. Tape and reel dimensions (See the table on page 2/4)





Fig. 2 Typical Tape and Reel configuration

PRODUCTS	TYPE Jisso Information for PAGE					
Semiconductor	BD6069GUT 2	2/4				
(Tape dimensions) (Reel dimensions)						
A1 B1 D0 D1 E F K' P0 P1 P2	T W A B C D E W1	W2				
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		13.4 ± 1.0				
$\left[\begin{array}{c} \pm 0.1 \\ \pm 0.1 \\ -0 \end{array} \right] \begin{array}{c} \pm 0.1 \\		i				
2. 3. Leader and Trailer						
2. 3. 1. Leader						
No component pockets are 40 pockets or more.						
 2. 3. 2. Trailer No component pockets are 10 pockets or more. 						
Tape is free from reel.						
2. 4. Label for Reel and Box						
Product No. BD6069GUT-E2						
	Out going inspection stamp (Only unit box)					
Quantity — 3, 000 pcs. 0124 A5110						
Lot numberMNo. 1						
MNo. 1						
Fig. 5 Label ex.	ample					
2. 5. Packing style						
4 reels or less per inner box.	Lab	bel				
Label Reel Fig. 6 Packing style	Inner box					
	2. 7. Decking meterials					
 6. Shipping style 4 unit boxes or less per shipping box. 	2. 7. Packing materials					
7	Item Material Embossed carrier tape PS					
255	Cover tape PET +	PE				
190	Reel PS					
	Unit box Cardboar					
	Shipping box Cardboar	rd				
193 193						
Fig. 7 Shipping box dimensions and shipping style						
(Unit:mm)						
ROHM CO.,LTD. REV. B	SPECIFICATION No. : TSZ02201-BD6069GUT-1-2					



PRODUCTS Semiconductor		Information for 6069GUT	PAGE 4/4		
6. Footprint dimensions (Optimize footprint dimensions to the board design and soldering condition)					
$\phi \phi O$	[Reference			
	Symbol	Value			
	e	0.50			
$ \qquad	b3	0.25			
		(Unit:mm)			

7. Regarding the underfill material

There are some cases that the underfill material is applied as purpose to reinforce the soldered junction of the package. Since the mount reliability depends on the resin material or coating condition, it may deteriorate on the contrary. Therefore, it is necessary to evaluate it sufficiently for its application.

In term of the coating condition, it is preferable that there is an enough material beyond the each four sides of a packeage.





8. External dimentions

