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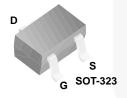


December 2015

BSS123W N-Channel Logic Level Enhancement Mode Field Effect Transistor

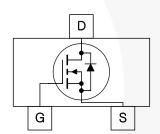
Features

- 0.17 A, 100 V, $R_{DS(ON)}$ = 6 Ω at V_{GS} = 10 V $R_{DS(ON)}$ = 10 Ω at V_{GS} = 4.5 V
- High Density Cell Design for Low R_{DS(ON)}
- · Rugged and Reliable
- · Ultra Small Surface Mount Package
- · Very Low Capacitance
- · Fast Switching Speed
- · Lead Free / RoHS Compliant



Description

This N-channel enhancement mode field effect transistor is produced using high cell density, trench MOSFET technology. This product minimizes on-state resistance while providing rugged, reliable and fast switching performance. This product is particularly suited for low-voltage, low-current applications such as small servo motor control, power MOSFET gate drivers, logic level transistor, high speed line drivers, power management/power supply and switching applications.



Ordering Information

Part Number Marking		Package	Packing Method	
BSS123W	BSS123W SA		Tape and Reel	

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at $T_A = 25$ °C unless otherwise noted.

Symbol	Parameter		Value	Unit		
V _{DSS}	Drain-Source Voltage		100	V		
V _{DGR}	Drain-Gate Voltage R _{GS} ≤ 20 kΩ		100	V		
V _{GSS}	Gate-Source Voltage		±20	V		
I _D	Drain Current	Continuous		0.17	A	
		Pulsed		0.68		
T _J , T _{STG}	Operating and Storage Temperature Range		-55 to +150	°C		

Thermal Characteristics

Values are at $T_A = 25$ °C unless otherwise noted.

Symbol	Parameter	Value	Unit
В	Total Power Dissipation	200	mW
P _D	Derate Above 25°C	1.6	mW/°C
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient ⁽¹⁾	625	°C/W

Note:

1. Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch. Minimum land pad size.

Electrical Characteristics

Values are at $T_A = 25$ °C unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
Off Charac	Off Characteristics					•
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	100			V
I _{DSS} 2	Zero Gate Voltage Drain Current	V _{DS} = 100 V, V _{GS} = 0 V			1	μΑ
		V _{DS} = 20 V, V _{GS} = 0 V			10	nA
I _{GSSF}	Gate-Body Leakage, Forward	V _{GS} = 20 V, V _{DS} = 0 V			50	nA
I _{GSSR}	Gate-Body Leakage, Reverse	$V_{GS} = -20 \text{ V}, V_{DS} = 0 \text{ V}$			-50	nA
On Charac	teristics ⁽²⁾					
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 1 \text{ mA}$	0.8	1.7	2.0	V
В	Static Drain-Source On-Resistance	$V_{GS} = 10 \text{ V}, I_D = 0.17 \text{ A}$		1.39	6	Ω
R _{DS(ON)}		$V_{GS} = 4.5 \text{ V}, I_D = 0.17 \text{ A}$		1.48	10	
9 _{FS}	Forward Transconductance	V _{DS} = 10 V, I _D = 0.17 A	80			mS
V _{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = 0.34 \text{ A}$		0.81	1.30	٧
Dynamic C	haracteristics					
C _{iss}	Input Capacitance			71		pF
C _{oss}	Output Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1.0 MHz		6.6		pF
C _{rss}	Reverse Transfer Capacitance	1 - 1.0 WII 12		2.74		pF
Switching	Characteristics ⁽²⁾					
t _r	Turn-On Rise Time			1.24	8	ns
t _f	Turn-Off Fall Time	V_{DD} = 30 V, I_{D} = 0.28 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		5.73	16	ns
t _{d(on)}	Turn-On Delay			2.94	8	ns
t _{d(off)}	Turn-Off Delay			8.4	13	ns

Note:

2. Pulse test: pulse width \leq 300 μ s, duty cycle \leq 2.0%.

Typical Performance Characteristics

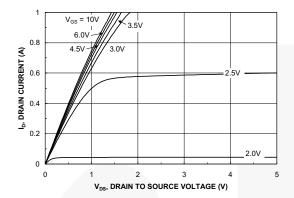


Figure 1. On-Region Characteristics

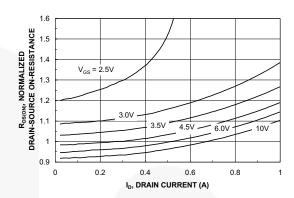


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

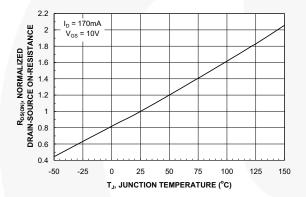


Figure 3. On-Resistance Variation with Temperature

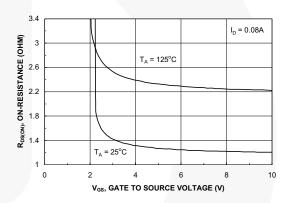


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

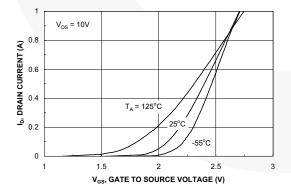


Figure 5. Transfer Characteristics

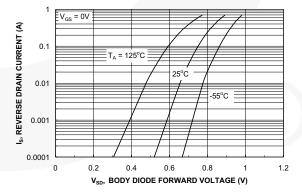


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

Typical Performance Characteristics (Continued)

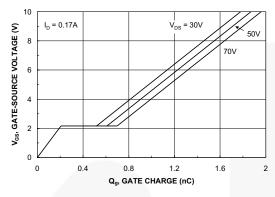


Figure 7. Gate Charge Characteristics

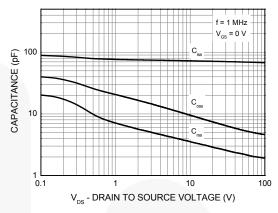
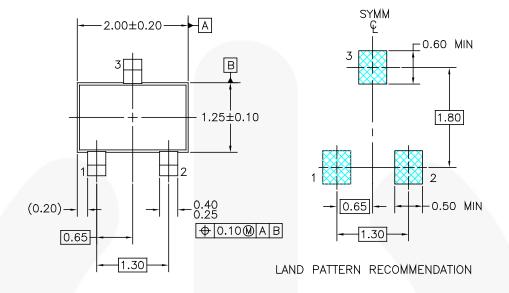
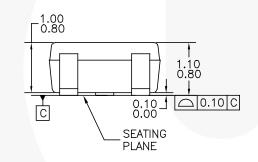
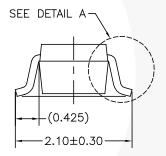


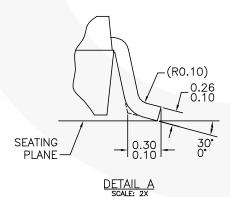
Figure 8. Capacitance

Physical Dimensions









NOTES: UNLESS OTHERWISE SPECIFIED

- THIS PACKAGE CONFORMS TO EIAJ
- B)
- THIS PACKAGE CONFORMS TO EIAJ SC-70. ALL DIMENSIONS ARE IN MILLIMETERS. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH.

MAA03AREVA

Figure 9. 3-LEAD, SC70, EIAJ SC-70, 1.25MM WIDE





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Definition of Terms				
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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.		
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