Cyclone V GX, GT, and E Device Errata

2018.03.05

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This document lists the errata for the Cyclone® V GX, GT, and E devices.

JTAG Programming of 28-nm Devices

JTAG configuration of 28-nm devices does not operate correctly when you initiate a PAUSE_DR instruction during configuration. In this scenario, JTAG configuration fails when pausing configuration in the middle of the bit stream by entering into the PAUSE-DR state and continuing to clock the TCK input. The failure is indicated by CONF_DONE staying low after all of the data has been clocked into the FPGA while nSTATUS remains high.

The PAUSE-DR feature works correctly with normal IEEE 1149.1 JTAG test operations.

Workaround

If you require pausing in the middle of the bit stream during JTAG configuration, halt the TCK and do not enter the PAUSE-DR state. Restart the TCK when you resume the configuration.

Status

Affects: Cyclone V GX, GT, and E devices

There is no planned fix for this issue.

Signal Detect Issue in PCIe Configuration

The Signal Detect (SD) circuit required in PCIe Configuration (Hard IP and PIPE mode) may switch OFF under the following conditions:

- Low temperature
- Upper limit of V_{CCER_GXB} (receiver buffer power supply voltage)

PCIe link training may not be fully completed in the case where the SD circuit remains de-asserted or remains OFF with an incoming signal.

This issue is a time-zero condition. If shipped devices have been tested not to show this issue initially, it will not show in the future.

Workaround

Update the Intel® Quartus® Prime settings for receiver common mode voltage (RX Vcm) and receiver signal detect circuit threshold (RX Vth) settings as shown in the following table.

Device	V_{CCER_GXB}	RX Vcm Voltage	RX Vth Settings
Cyclone V GT/ST	1.2 V	0.75 V	4

To update RX Vcm and RX Vth settings, refer to the KDB solution.

If you are unable to make changes to resolve the issue, contact **Intel Premier Support** for additional information.

Status

Affects: Cyclone V GT/ST devices

There is no planned fix for this issue.

Related Information

RX Vcm and RX Vth KDB solution.

External Memory Interface (EMIF) Maximum Frequency Specification Update

Description

To achieve timing closure, the EMIF maximum frequency specification has been updated in the table below.

Table 1: Cyclone V EMIF Maximum Frequency Specification Update

Note: In this table, the stated performances apply to component topology only. The DIMM topology is not supported on the hard controller.

Note: For changes to other variants and slower speed grades, refer to the **External Memory Interface Spec Estimator**.

Device	Speed Grade	Memory Type	Memory Topology	Depth Expansion	Interface Type	Original Maximum Spec (MHz)	Updated Maximum Spec (MHz)
Cyclone V GX/E	-C6	DDR2	Component	2 Chip Selects	Hard Controller	400	333
Cyclone V GX/GT/E	-A7	DDR2	Component	1 Chip Select	Hard Controller	400	333

Device	Speed Grade	Memory Type	Memory Topology	Depth Expansion	Interface Type	Original Maximum Spec (MHz)	Updated Maximum Spec (MHz)
Cyclone V GX/GT/E	-A7	DDR2	Component	2 Chip Selects	Hard Controller	333	300

Status

Affects: Cyclone V GX, GT, and E devices

Status: No planned fix

Fractional PLL Phase Alignment Error

Description

The fPLL has a silicon sensitivity that causes the static phase error to operate beyond the Quartus II software expectation. The frequency range and jitter performance of the fPLL meet the *Cyclone V Device Datasheet* specifications. This sensitivity is a time zero failure, which means a design affected by this issue will show failure immediately upon a given device operation over expected operating conditions or will never show the issue.

The following usage modes may be affected:

- When the fPLL is used for phase compensation. For example, applications that may use phase compensation include LVDS, board trace matching, or FPGA skew compensation, such as zero delay buffering.
- Specific IP cores that require fPLL usage.
- Inter-clock domain transfers involving fPLL usage.

Workaround

You can implement design techniques to mitigate inter-clock domain transfers and use the Intel tool to evaluate fPLL usage and determine if designs may be affected by this issue.

Note: To determine if your design may be affected, use the **Altera fPLL Usage Evaluation Tool**.

If you believe your design is affected by this issue, please contact **Intel Premier Support** for further assistance.

Status

Affects: Cyclone V GX, GT, and E devices

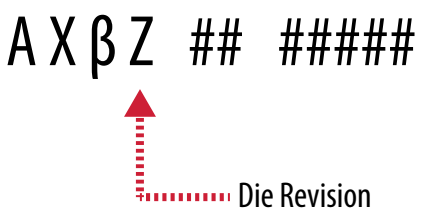
This issue is fixed in the silicon die revision shown below.

Table 2: Fixed Silicon by Die Revision

Family	Device	Fixed Die Revision
Cyclone V GT	5CGTD9	B
	5CGTD7	C
	5CGTD5	B
Cyclone V GX	5CGXC9	B
	5CGXC7	C
	5CGXC5	B
	5CGXC4	B
	5CGXC3	B
Cyclone V E	5CEA9	B
	5CEA7	C
	5CEA5	B
	5CEA4	B
	5CEA2	B

Figure 1: Altera Date Code Marking Format

This figure explains the date code and revision marking format.



Related Information

Cyclone V Device Datasheet

Configuration via Protocol (CvP)

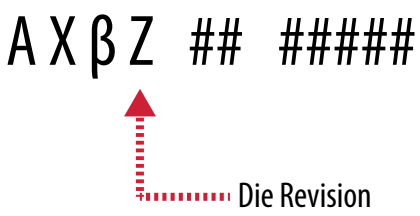
Description

The fix for this issue requires a new die revision. Use the die revision character in the Date Code (printed on the top side of the device) to determine if the device supports CvP. The CvP update can only be used at Gen1 data rates.

CvP is supported if the fourth alphanumeric character from the left ("Z" in Figure below) is equal to, or later in the alphabet than the letter in the "Revision with Fix" column of the table shown in the "Status" section below.

Figure 2: Altera Date Code Marking Format

This figure explains the date code and revision marking format.



Status

Affects: Cyclone V GX and GT devices, except for 5CGXC3

Status: Devices that are CvP capable will be available in Q2 2013

The table below shows which revisions will have the fix.

Table 3: Device and Die Revisions

Note: Future revisions beyond the one listed in the "Revision with Fix" column will be CvP capable.

Member Code	Revisions without Fix	Revision with Fix
5CGXC3	None	A
5CGXC4	A	B
5CGXC5	A	B
5CGXC7	A and B	C
5CGXC9	A	B
5CGTD5	A	B
5CGTD7	A and B	C
5CGTD9	A	B

Note: For Gen2 CvP updates or further inquiries, please contact **Intel Premier Support**.

Usermode High Icc

Description

When the affected device transitions into User mode, high Icc is observed, due to internal dataline contention.

Workaround

Use the following software workaround to prevent the Usermode high Icc issue:

- For the Error Detection Cyclic Redundancy Check (EDCRC) user, no workaround is needed because the EDCRC feature eliminates the high Icc issue.
- For the non-EDCRC user, a software workaround is needed and is available in the Quartus II software version 12.1 sp1, or later.

Action Needed for Existing Designs (pre-Quartus II version 12.1 sp1)

Specific action is needed when the existing design uses the EDCRC and certain versions of the Quartus II software. The table below lists the actions needed for different settings.

Table 4: Device and Die Revisions

Design	Quartus II Version	Action
EDCRC enabled	Any	None needed.
EDCRC disabled	12.1 only	Full recompilation is required using the Quartus II software version 12.1 sp1, or later release.
	Pre-12.1	Full recompilation is NOT needed, but requires the use of Quartus II software version 12.1 sp1, or later for programming file conversion.(1)

Status

Affects: Cyclone V GX, GT, and E devices

Status: No planned fix

False Configuration Failure in Active Serial Multi-Device Configuration x1 Mode

Description

In Active Serial (AS) multi-device configuration x1 mode, the error checking for `CONF_DONE` release may not operate correctly. Because of this, false configuration errors may result. The failure is indicated by `CONF_DONE` going high followed by `nSTATUS` going low and reconfiguration repeatedly initiated.

Workaround

To overcome this issue, perform the following steps:

1. Disable the `CONF_DONE` error checking in AS multi-device configuration mode:

(1) Convert the existing SOF file to RBF, POF, JIC, or another format using **Convert Programming File**, under the **File** menu of the Quartus II software.

a. If you are using Quartus II version 12.0 software or older, check the "Disable AS mode CONF_DONE error check" option. This option can be found in the "Advanced" button under the Convert Programming File window.

b. If you are using Quartus II version 12.0 SP1 or later, the error checking is disabled automatically for AS multi-device configuration POF file generation.

2. Enable the `INIT_DONE` pin option:

a. To ensure successful configuration, Altera recommends that you enable the `INIT_DONE` optional pin for devices in the configuration chain. On the board, do not tie `INIT_DONE` pins together between master and slave devices. Monitor the `INIT_DONE` status for each device to ensure a successful transition into user-mode.

Note: Other configuration modes (JTAG, Fast Passive Parallel (FPP), Passive Serial (PS) single and multi device configuration, and AS single device configuration) are not affected.

Status

Affects: Cyclone VES GX, GT, and E devices

Status: No planned fix

Revision History for Cyclone V GX, GT, and E Device Errata

Date	Version	Changes
March 2018	2018.03.05	Made the following changes: • Updated the related information link in the "Signal Detect Issue in PCIe Configuration" section.
April 2017	2017.04.19	Made the following changes: • Corrected the URL to the fPLL evaluation tool in the "Fractional PLL Phase Alignment Error" section.
March 2017	2017.03.27	Made the following changes: • Changed the status to show correct list of affected devices.
March 2017	2017.03.15	Made the following changes: • Added the "Signal Detect Issue in PCIe Configuration" section.
September 2015	2015.09.18	Made the following changes: • Added the "JTAG Programming of 28-nm Devices" section.
April 2015	2015.04.03	Made the following changes: • Restructured and reformatted the document. • Removed the "SEU Internal Scrubbing" section. • Removed all SoC-related errata. This content is provided in the *Cyclone V SX, ST and E SoC Device Errata* document.