

April 1988 Revised September 2000

74F174

Hex D-Type Flip-Flop with Master Reset

General Description

The 74F174 is a high-speed hex D-type flip-flop. The device is used primarily as a 6-bit edge-triggered storage register. The information on the D inputs is transferred to storage during the LOW-to-HIGH clock transition. The device has a Master Reset to simultaneously clear all flip-flops.

Features

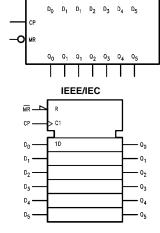
- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- Asynchronous common reset
- Guaranteed 4000V minimum ESD protection

Ordering Code:

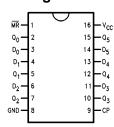
Order Number	Package Number	Package Description
74F174SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
74F174SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F174PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



Unit Loading/Fan Out

Pin Names	Decemention	U.L.	Input I _{IH} /I _{IL}	
Pin Names	Description	HIGH/LOW	Output I _{OH} /I _{OL}	
D ₀ -D ₅	Data Inputs	1.0/1.0	20 μA/-0.6 mA	
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μA/-0.6 mA	
MR	Master Reset Input (Active LOW)	1.0/1.0	20 μA/-0.6 mA	
Q ₀ -Q ₅	Outputs	50/33.3	-1 mA/20 mA	

Functional Description

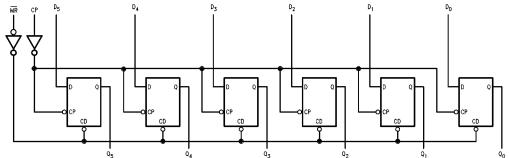
The 74F174 consists of six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The Clock (CP) and Master Reset (MR) are common to all flip-flops. Each D input's state is transferred to the corresponding flip-flop's output following the LOW-to-HIGH Clock (CP) transition. A LOW input to the Master Reset (MR) will force all outputs LOW independent of Clock or Data inputs. The 74F174 is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

Truth Table

	Outputs		
MR	СР	D _n	Q _n
L	Х	Х	L
Н	~	Н	Н
Н	~	L	L

- H = HIGH Voltage Level
- L = LOW Voltage Level
- X = Immaterial
- = LOW-to-HIGH Clock Transition

Logic Diagram



 $\dot{q_5}$ $\dot{q_4}$ $\dot{q_3}$ $\dot{q_2}$ $\dot{q_1}$ Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

Recommended Operating Conditions

 $\begin{array}{ll} \mbox{Storage Temperature} & -65^{\circ}\mbox{C to } +150^{\circ}\mbox{C} \\ \mbox{Ambient Temperature under Bias} & -55^{\circ}\mbox{C to } +125^{\circ}\mbox{C} \\ \end{array}$

Ambient Temperature under Bias -55°C to +125°C

Junction Temperature under Bias -55°C to +150°C

-55°C to +150°C

 V_{CC} Pin Potential to Ground Pin -0.5V to +7.0V Input Voltage (Note 2) -0.5V to +7.0V Input Current (Note 2) -30 mA to +5.0 mA

Voltage Applied to Output in HIGH State (with $V_{CC} = 0V$)

 $\begin{array}{lll} \text{Standard Output} & & -0.5 \text{V to V}_{\text{CC}} \\ \text{3-STATE Output} & & -0.5 \text{V to } +5.5 \text{V} \end{array}$

Current Applied to Output

 $\label{eq:lower_state} \begin{array}{ll} \text{in LOW State (Max)} & \text{twice the rated I}_{\text{OL}} \text{ (mA)} \\ \text{ESD Last Passing Voltage (Min)} & 4000 \text{V} \end{array}$

Free Air Ambient Temperature 0° C to +70°C Supply Voltage +4.5V to +5.5V

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

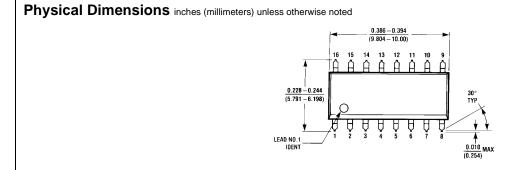
Symbol	Parameter		Min	Тур	Max	Units	v _{cc}	Conditions
V _{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage				8.0	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage				-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH	10% V _{CC}	2.5			V	Min	I _{OH} = -1 mA
	Voltage	$5\% V_{CC}$	2.7			V	IVIIII	$I_{OH} = -1 \text{ mA}$
V _{OL}	Output LOW	10% V _{CC}			0.5	V	Min	I _{OL} = 20 mA
	Voltage	10% V _{CC}			0.5	V	IVIIII	I _{OL} = 20 mA
I _{IH}	Input HIGH				5.0	μА	Max	V _{IN} = 2.7V
	Current				5.0	μΛ	IVIAX	V N - 2.1 V
I _{BVI}	Input HIGH Current				7.0	μА	Max	V _{IN} = 7.0V
	Breakdown Test							VIN - 1.0V
I _{CEX}	Output HIGH				50	μА	Max	V _{OUT} = V _{CC}
	Leakage Current				30	μΛ	IVIAX	VOUT - VCC
V _{ID}	Input Leakage		4.75			V	0.0	I _{ID} = 1.9 μA
	Test		4.73			V	0.0	All Other Pins Grounded
I _{OD}	Output Leakage				3.75		0.0	V _{IOD} = 150 mV
	Circuit Current				3.73	μΑ	0.0	All Other Pins Grounded
I _{IL}	Input LOW Current				-0.6	mA	Max	V _{IN} = 0.5V
los	Output Short-Circuit Current		-60		-150	mA	Max	$V_{OUT} = 0V$
I _{CCH}	Power Supply Current			30	45	mA	Max	CP = _
								$D_n = \overline{MR} = HIGH$
I _{CCL}	Power Supply Current			30	45	mA	Max	$V_O = LOW$

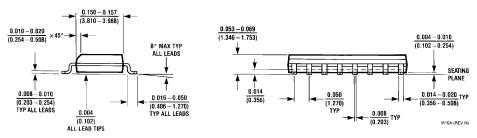
AC Electrical Characteristics

Symbol	Parameter	$T_{A} = +25^{\circ}C$ $V_{CC} = +5.0V$ $C_{L} = 50 \text{ pF}$			$T_{A} = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = +5.0V$ $C_{L} = 50 \text{ pF}$		$T_A = 0$ °C to +70°C $V_{CC} = +5.0V$ $C_L = 50$ pF		Units
		Min	Тур	Max	Min	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency	80			70		80		MHz
t _{PLH}	Propagation Delay	3.5	5.5	8.0	3.0	10.0	3.5	9.0	
t _{PHL}	CP to Q _n	4.0	7.0	10.0	4.0	12.0	4.0	11.0	ns
t _{PHL}	Propagation Delay MR to Q _n	5.0	10.0	14.0	5.0	16.0	5.0	15.0	ns

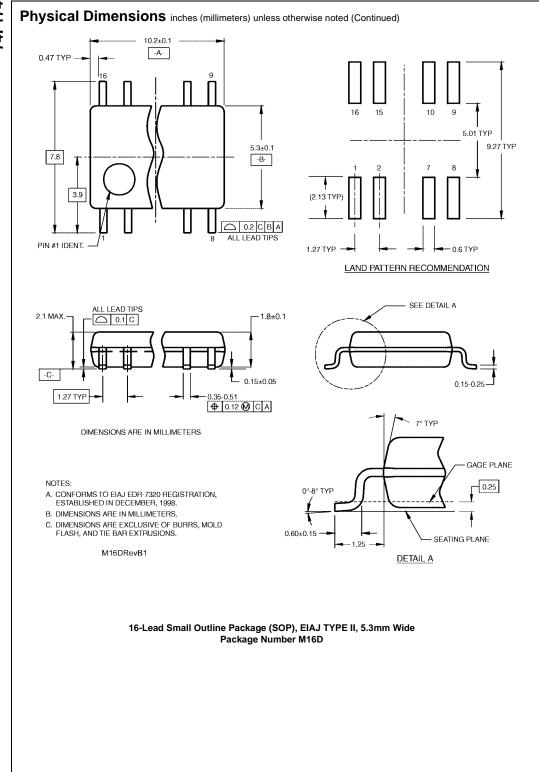
AC Operating Requirements

-		$T_A = +25^{\circ}C$ $V_{CC} = +5.0V$		$T_A = -55^{\circ}C \text{ to } +125^{\circ}$ $V_{CC} = +5.0V$		$T_A = 0$ °C to $+70$ °C $V_{CC} = +5.0V$		Units	
Symbol	Parameter								
		Min	Max	Min	Max	Min	Max		
t _S (H)	Setup Time, HIGH or LOW	4.8		5.0		4.8			
t _S (L)	D _n to CP	4.0		5.0		4.0		ns	
t _H (H)	Hold Time, HIGH or LOW	0		2.0		0		lio	
t _H (L)	D _n to CP	0		2.0		0			
t _W (H)	CP Pulse Width	4.0		5.0		4.0		ns	
$t_W(L)$	HIGH or LOW	6.0		7.5		6.0		115	
t _W (L)	MR Pulse Width, LOW	5.0		6.5		5.0		ns	
t _{REC}	Recovery Time, MR to CP	5.0		6.0		5.0			





16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow Package Number M16A



N16E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued) $\frac{0.740 - 0.780}{(18.80 - 19.81)}$ 0.090 (2.286) 15 14 13 12 11 16 T5 F INDEX AREA 0.250 ± 0.010 $\frac{6.350 \pm 0.310}{(6.350 \pm 0.254)}$ PIN NO. 1 PIN NO. 1 1 2 3 4 5 6 7 8 1 2 IDENT IDENT OPTION 01 OPTION 02 0.065 0.130 ± 0.005 (1.651 0.060 4º TYP 0.300 - 0.320 (1.524) TYP (3.302 ± 0.127) OPTIONAL (7.620 - 8.128) $\frac{0.145 - 0.200}{(3.683 - 5.080)}$ 95°±5° 0.00 - 800.0 90° ± 4° TYP 0.020 0.203 - 0.40.280 (0.508)0.125 **-** 0.150 (3.175 **-** 3.810) (7.112) 0.030 ± 0.015 (0.762 ± 0.381) MIN 0.014 - 0.023 0.100 ± 0.010 (0.325 +0.040 -0.015

(B OFF +1.016) 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N16E

 (2.540 ± 0.254)

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LIFE SUPPORT POLICY

 $\overline{(0.356 - 0.584)}$

TYP

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