

Devices Connected/Referenced

AD9958/ AD9959	500 MSPS, 2-Channel/4-Channel, Direct Digital Synthesizer (DDS)
AD9520	Clock Generator and Distribution IC

Phase Coherent FSK Modulator

CIRCUIT FUNCTION AND BENEFITS

The standard single channel direct digital synthesizer (DDS) does not switch between frequencies in a phase coherent manner. By design, DDS frequency transitions are *phase continuous* (see Figure 2, for example). However, the circuit shown in Figure 1 demonstrates how to configure the AD9958/AD9959 multichannel DDS for a robust *phase coherent* FSK (frequency shift keying) modulator by summing the outputs of the multichannel DDS together.

A multichannel DDS virtually eliminates temperature and timing issues between channels compared to synchronizing multiple single channel devices for the same application. For instance, multichannel DDS outputs, though independent, share the same system clock edges in the chip. Consequently, the system clock edges across multiple chips would not track as well over temperature and power supply deviations compared to an integrated multichannel DDS. As a result, a multichannel DDS is better suited for producing a closer to ideal phase coherent frequency transition at the summed output.

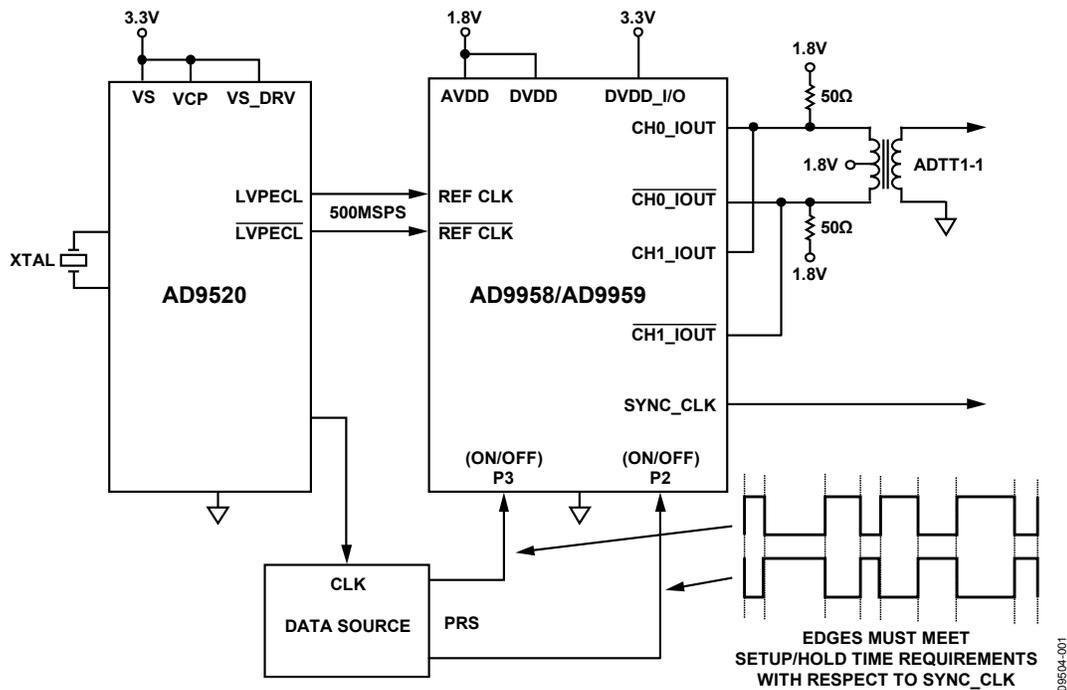


Figure 1. Setup for Phase Coherent FSK Modulator (Simplified Schematic: All Connections and Decoupling Not Shown)

Rev. 0

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CIRCUIT DESCRIPTION

The AD9520-x clock generator and distribution IC drives the AD9958/AD9959 with a high performance reference clock, at the same time providing the clock to the data source for the FSK data stream, which is a pseudo random sequence (PRS). The AD9520 provides multiple output logic choices, as well as delay adjustment verniers to meet the setup and hold time requirements between the FSK data stream and SYNC_CLK of the multichannel AD9958/AD9959 DDS.

The AD9958 consists of two independent DDS channels with differential current output. In the circuit, those current outputs are wired together (summed) with pre-programmed frequencies (F1 and F2). To select the desired frequency, the channel outputs are equipped with an ON/OFF feature driven by the profile pins. In this case, the profile pins are configured to drive the multiplier at each DAC input to control the output amplitude.

To accomplish this, each multiplier is pre-programmed with two profile-selectable settings: zero-scale and full-scale. A logic low on the profile pins shuts off the sine wave at the DAC output, and a logic high passes the sine wave. The operation requires two complementary input data streams to alternate between the two frequencies.

The two DDS channels run continuously generating frequencies F1 and F2. The OFF feature mutes the appropriate DDS output, thereby producing an FSK signal that is phase coherent.

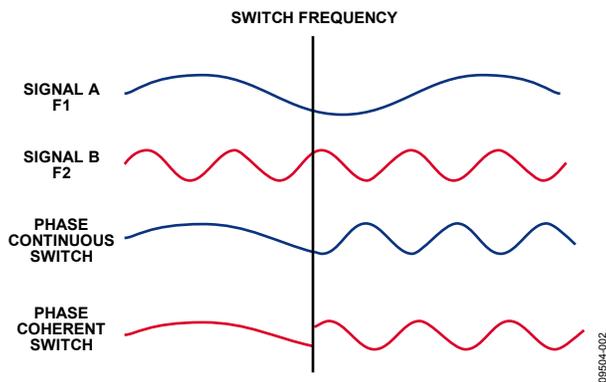


Figure 2. Phase Continuous vs. Phase Coherent Frequency Switching

The 4-channel AD9959 DDS was used to generate the unfiltered waveforms shown in Figure 3 and Figure 4. The AD9959 better demonstrates phase coherent switching because the two unused channels can serve as a phase reference for the two switched frequencies at the summed output. The upper trace is the summed output showing phase coherent switching. The next two traces are the reference signals for F1 and F2. The bottom trace is the PRS (pseudorandom sequence) data stream that selects between the two frequencies. Note the edges of the PRS data stream do not align with the frequency transitions of the summed outputs due to the pipeline delay within the device.

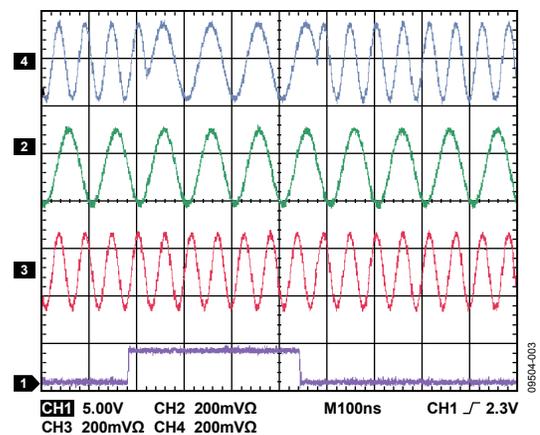


Figure 3. Measured Phase Coherent FSK Transition

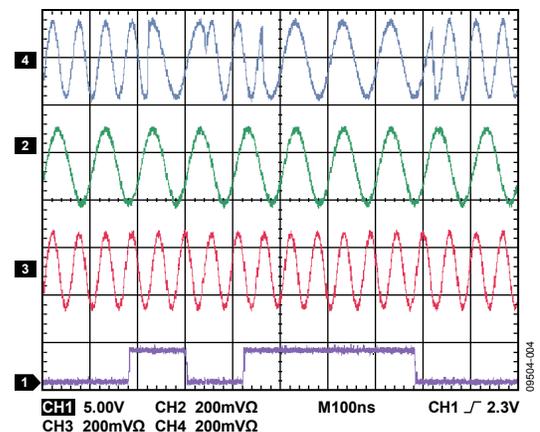


Figure 4. Measured Phase Coherent FSK Transition

COMMON VARIATIONS

Analog Devices offers a variety of direct digital synthesizers, clock distribution chips, and clock buffers to design DDS-based clock generators. Refer to www.analog.com/dds and www.analog.com/clock for more information.

LEARN MORE

AN-837 Application Note, *DDS-Based Clock Jitter Performance vs. DAC Reconstruction Filter Performance*. Analog Devices.

Kester, Walt. 2005. *The Data Conversion Handbook*. Analog Devices. Chapters 6 and 7.

Kester, Walt. 2006. *High Speed System Applications*. Analog Devices. Chapter 2, "Optimizing Data Converter Interfaces."

Kester, Walt. 2006. *High Speed System Applications*. Analog Devices. Chapter 3, "DACs, DDSs, PLLs, and Clock Distribution."

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of AGND and DGND*. Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*. Analog Devices.

Data Sheets and Evaluation Boards

[AD9958 Data Sheet](#)

[AD9958 Evaluation Board](#)

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[AD9520-0 Data Sheet](#)

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REVISION HISTORY

1/11—Revision 0: Initial Version

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