RoHS

COMPLIANT

HALOGEN

FREE



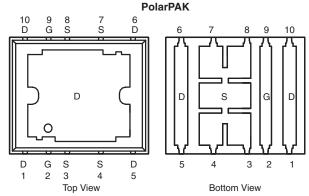


N-Channel 100-V (D-S) MOSFET

PRODUCT SUMMARY					
		I _D (A)			
V _{DS} (V)	$R_{DS(on)}\left(\Omega\right)$	Silicon Limit	Package Limit	Q _g (Typ.)	
100	0.0142 at V _{GS} = 10 V	64	60 ^a	50 nC	

Package Drawing

www.vishay.com/doc?72945



Top surface is connected to pins 1, 5, 6, and 10

Ordering Information: SiE854DF-T1-E3 (Lead (Pb)-free)

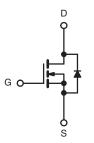
SiE854DF-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFET
- Ultra Low Thermal Resistance Using Top-Exposed PolarPAK[®] Package for Double-Sided Cooling
- Leadframe-Based New Encapsulated Package
 - Die Not Exposed
 - Same Layout Regardless of Die Size
- Low Q_{qd}/Q_{qs} Ratio Helps Prevent Shoot-Through
- 100 % R_q and UIS Tested
- Compliant to RoHS directive 2002/95/EC

APPLICATIONS

- Primary Side Switch
- · Half-Bridge



N-Channel MOSFET For Related Documents www.vishay.com/ppg?69824

Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V_{DS}	100	V	
Gate-Source Voltage		V_{GS}	± 20	V	
Continuous Drain Current (T _{.I} = 150 °C)	$T_C = 25 ^{\circ}C$ $T_C = 70 ^{\circ}C$	I _D	64 (Silicon Limit) 60 ^a (Package Limit) 52		
	T _A = 25 °C T _A = 70 °C		13.2 ^{b, c} 10.5 ^{b, c}	A	
Pulsed Drain Current		I _{DM}	60		
Continuous Source-Drain Diode Current	$T_C = 25 ^{\circ}C$ $T_A = 25 ^{\circ}C$	I _S	60 ^a 4.3 ^{b, c}		
Single Pulse Avalanche Current	I _ 0.1 m∐	I _{AS}	40		
Single Pulse Avalanche Energy L = 0.1 mH		E _{AS}	80		
Maximum Power Dissipation		P _D	125 80 5.2 ^{b, c} 3.3 ^{b, c}	w	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150	°C	
Soldering Recommendations (Peak Tempera	ature) ^{d, e}		260		

Notes:

- a. Package limited.
- b. Surface Mounted on 1" x 1" FR4 board.
- c. t = 10 s.
- d. See Solder Profile (www.vishay.com/doc?73257). The PolarPAK is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

SiE854DF

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THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^{a, b} $t \le 10 \text{ s}$		R_{thJA}	20	24		
Maximum Junction-to-Case (Drain Top)	Steady State	R _{thJC} (Drain)	0.8	1	°C/W	
Maximum Junction-to-Case (Source)a, c	ase (Source) ^{a, c}		2.2	2.7		

Notes:

- a. Surface Mounted on 1" x 1" FR4 board.
- b. Maximum under Steady State conditions is 68 °C/W.
- c. Measured at source pin (on the side of the package).

Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	100			V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I _D = 250 μA		120		mV/°C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I _D = 250 μA		- 10			
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_{D} = 250 \mu A$	2.5		4.4	V	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 100 V, V _{GS} = 0 V			1		
		V _{DS} = 100 V, V _{GS} = 0 V, T _J = 55 °C			10	μΑ	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	25			Α	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 13.2 A		0.0117	0.0142	Ω	
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 13.2 A		30		S	
Dynamic ^b							
Input Capacitance	C _{iss}			3100		pF	
Output Capacitance	C _{oss}	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		250			
Reverse Transfer Capacitance	C _{rss}			95			
Total Gate Charge	Q_q			50	75	nC	
Gate-Source Charge	Q_{gs}	$V_{DS} = 50 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 13.2 \text{ A}$		16			
Gate-Drain Charge	Q_{gd}			13			
Gate Resistance	R_{g}	f = 1 MHz		1	1.5	Ω	
Turn-On Delay Time	t _{d(on)}			15	25		
Rise Time	t _r	V_{DD} = 50 V, R_L = 5 Ω		10	15	ns	
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 10 \text{ A}, V_{GEN} = 10 \text{ V}, R_q = 1 \Omega$		30	45		
Fall Time	t _f	Č		10	15		
Drain-Source Body Diode Characteristic	s		ı				
Continuous Source-Drain Diode Current	Is	T _C = 25 °C			60	A	
Pulse Diode Forward Current ^a	I _{SM}				60		
Body Diode Voltage	V _{SD}	I _S = 10 A		0.8	1.2	٧	
Body Diode Reverse Recovery Time	t _{rr}	<u>-</u>		70	110	ns	
Body Diode Reverse Recovery Charge	Q _{rr}	1 10 A dl/dt 100 A/vo T 05 °C		195	300	nC	
Reverse Recovery Fall Time	t _a	- I _F = 10 A, dl/dt = 100 A/μs, T _J = 25 °C		56		ns	
Reverse Recovery Rise Time	t _b			14			

Notes:

- a. Pulse test; pulse width \leq 300 $\mu s,$ duty cycle \leq 2 %
- b. Guaranteed by design, not subject to production testing.

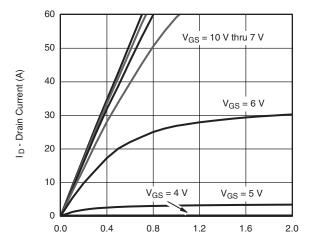
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.





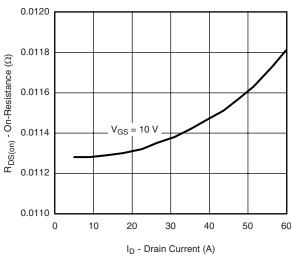


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

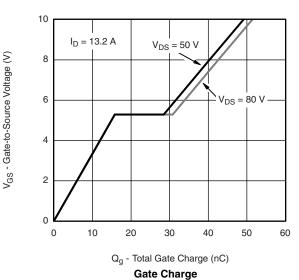


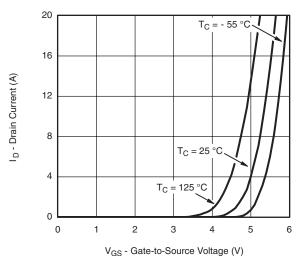
V_{DS} - Drain-to-Source Voltage (V)

Output Characteristics



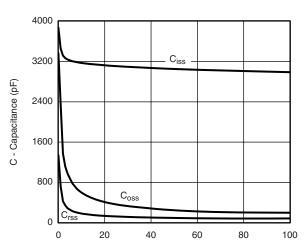
On-Resistance vs. Drain Current and Gate Voltage





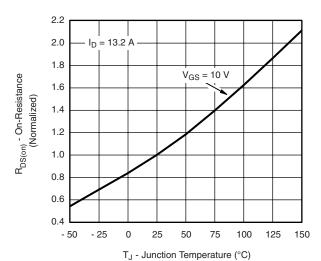
Transfer Characteristics

Transfer Characteristics



V_{DS} - Drain-to-Source Voltage (V)

Capacitance

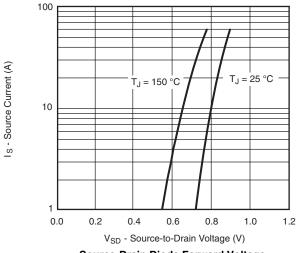


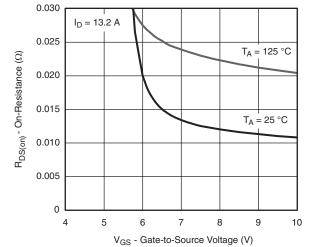
On-Resistance vs. Junction Temperature

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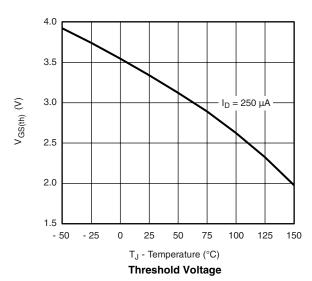
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

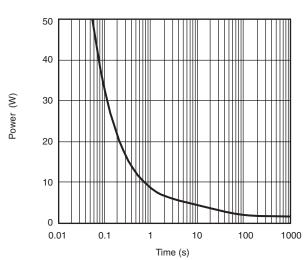




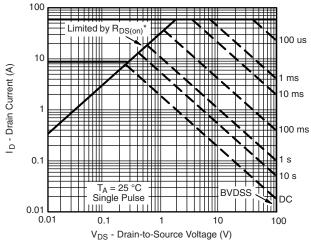
Source-Drain Diode Forward Voltage







Single Pulse Power, Junction-to-Ambient



* V_{GS} > minimum V_{GS} at which R_{DS(on)} is specified

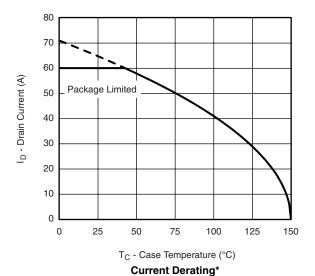
Safe Operating Area, Junction-to-Ambient

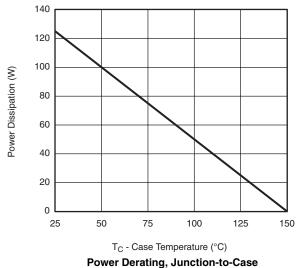




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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



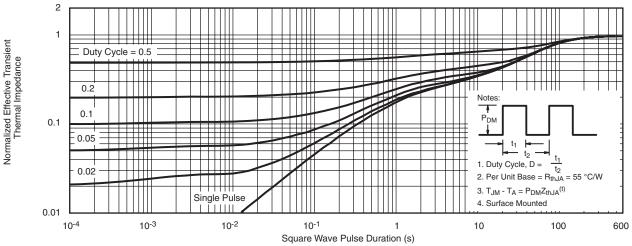


^{*} The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

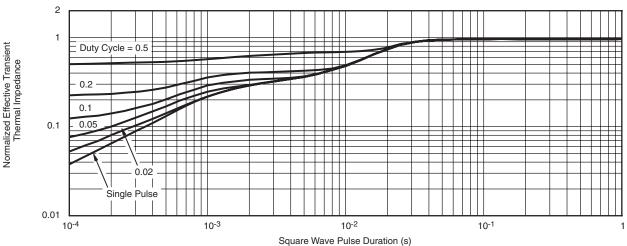
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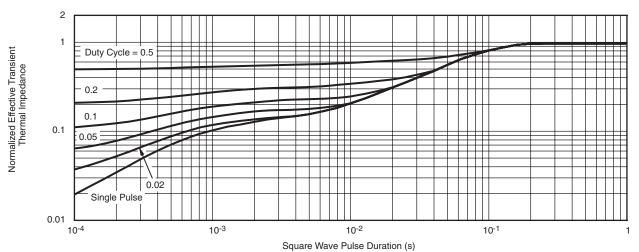
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case (Drain Top)



Normalized Thermal Transient Impedance, Junction-to-Source

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