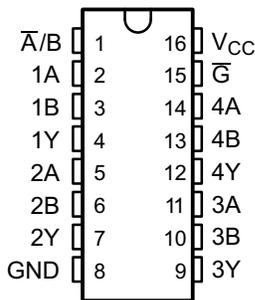
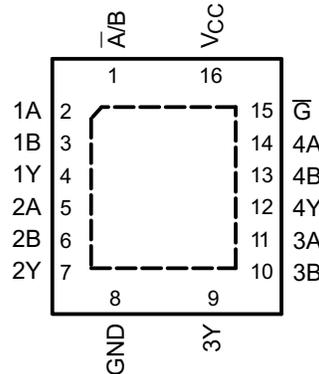
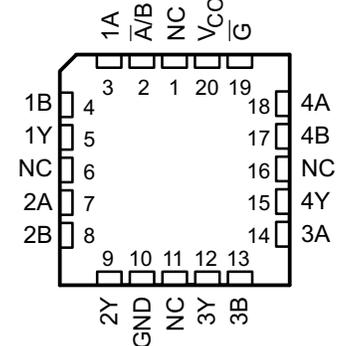


QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

Check for Samples: [SN54AHC157](#), [SN74AHC157](#)

FEATURES

- Operating Range 2-V to 5.5-V
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

**SN54AHC157 . . . J or W PACKAGE
SN74AHC157 . . . D, DB, DGV, N, NS,
OR PW PACKAGE
(TOP VIEW)**

**SN74AHC157 . . . RGY PACKAGE
(TOP VIEW)**

**SN54AHC157 . . . FK PACKAGE
(TOP VIEW)**


NC – No internal connection

DESCRIPTION

These quadruple 2-line to 1-line data selectors/multiplexers are designed for 2-V to 5.5-V V_{CC} operation.

The 'AHC157 devices feature a common strobe (\bar{G}) input. When the strobe is high, all outputs are low. When the strobe is low, a 4-bit word is selected from one of two sources and is routed to the four outputs. The devices provide true data.

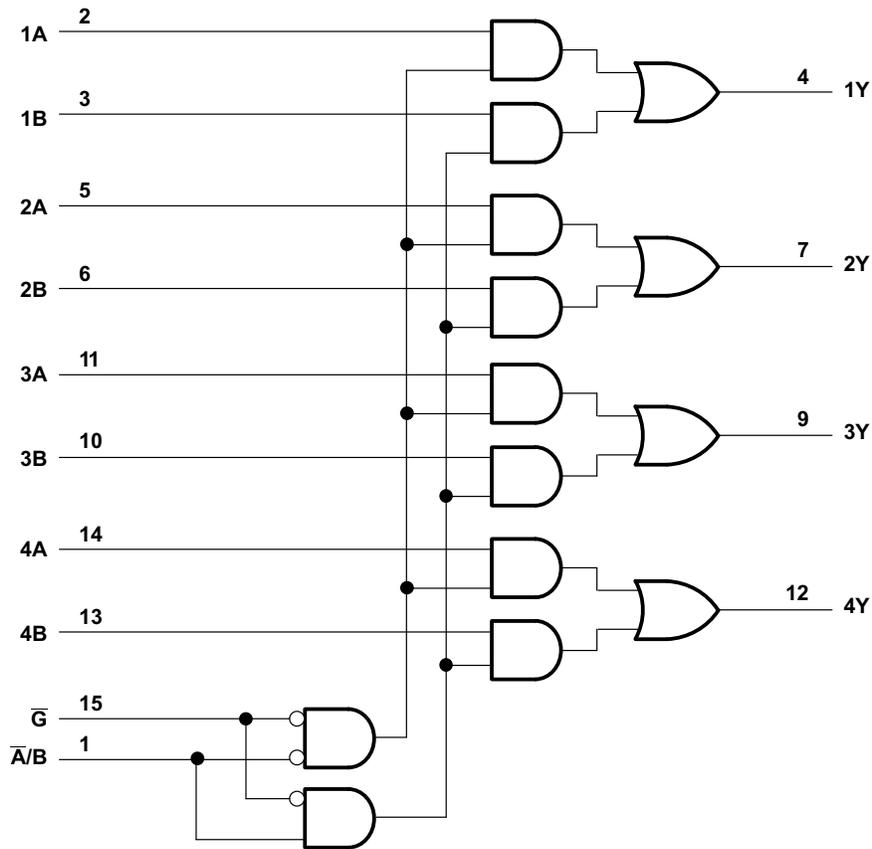
FUNCTION TABLE

INPUTS				OUTPUT
\bar{G}	\bar{A}/B	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for the D, DB, DGV, J, N, NS, PW, RGY, and W packages.

ABSOLUTE MAXIMUM RATINGS

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		VALUE	UNIT
Supply voltage range, V_{CC}		-0.5 to 7	V
Input voltage range, V_I ⁽²⁾		-0.5 to 7	V
Output voltage range, V_O ⁽²⁾		-0.5 to $V_{CC} + 0.5$	V
Input clamp current, I_{IK} ($V_I < 0$)		-20	mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)		± 20	mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})		± 25	mA
Continuous current through V_{CC} or GND		± 50	mA
Package thermal impedance, θ_{JA}	D package ⁽³⁾	73	°C/W
	DB package ⁽³⁾	82	
	DGV package ⁽³⁾	120	
	N package ⁽³⁾	67	
	NS package ⁽³⁾	64	
	PW package ⁽³⁾	108	
	RGY package ⁽⁴⁾	39	
Storage temperature range, T_{stg}		-65 to 150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The package thermal impedance is calculated in accordance with JESD 51-7.

(4) The package thermal impedance is calculated in accordance with JESD 51-5.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

		SN54AHC157		SN74AHC157		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2	5.5	2	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V	1.5	1.5		V
		$V_{CC} = 3$ V	2.1	2.1		
		$V_{CC} = 5.5$ V	3.85	3.85		
V_{IL}	Low-level Input voltage	$V_{CC} = 2$ V	0.5		0.5	V
		$V_{CC} = 3$ V	0.9		0.9	
		$V_{CC} = 5.5$ V	1.65		1.65	
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2$ V	-50		-50	mA
		$V_{CC} = 3.3$ V ± 0.3 V	-4		-4	
		$V_{CC} = 5$ V ± 0.5 V	-8		-8	
I_{OL}	Low-level output current	$V_{CC} = 2$ V	50		50	mA
		$V_{CC} = 3.3$ V ± 0.3 V	4		4	
		$V_{CC} = 5$ V ± 0.5 V	8		8	
$\Delta t/\Delta v$	Input Transition rise or fall rate	$V_{CC} = 3.3$ V ± 0.3 V	100		100	ns/V
		$V_{CC} = 5$ V ± 0.5 V	20		20	
T_A	Operating free-air temperature	-55	125	-40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			T _A = -55°C TO 125°C		T _A = -40°C TO 85°C		T _A = -40°C TO 125°C		UNIT
						Recommended		SN54AHC157		SN74AHC157		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	2 V	1.9	2		1.9		1.9		1.9	V	
		3 V	2.9	3		2.9		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		4.4		
	I _{OH} = -4 mA	3 V	2.58		2.48		2.48		2.48			
	I _{OH} = -8 mA	4.5 V	3.94		3.8		3.8		3.8			
V _{OL}	I _{OL} = 50 μA	2 V			0.1		0.1		0.1		V	
		3 V			0.1		0.1		0.1			
		4.5 V			0.1		0.1		0.1			
	I _{OH} = 4 mA	3 V			0.36		0.5		0.44			
	I _{OH} = 8 mA	4.5 V			0.36		0.5		0.44			
I _I	V _I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1 ⁽¹⁾		±1		μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			4		40		40		μA	
C _i	V _I = V _{CC} or GND	5 V		2	10				10		pF	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C		T _A = -55°C TO 125°C		T _A = -40°C TO 85°C		T _A = -40°C TO 125°C		UNIT
						Recommended		SN54AHC157		SN74AHC157		
				TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A or B	Y	C _L = 15 pF	6.2 ⁽¹⁾	9.7 ⁽¹⁾	1 ⁽¹⁾	11.5 ⁽¹⁾	1	11.5	1	11.5	ns
t _{PHL}				6.2 ⁽¹⁾	9.7 ⁽¹⁾	1 ⁽¹⁾	11.5 ⁽¹⁾	1	11.5	1	11.5	
t _{PLH}	$\overline{A/B}$	Y	C _L = 15 pF	8.4 ⁽¹⁾	13.2 ⁽¹⁾	1 ⁽¹⁾	15.5 ⁽¹⁾	1	15.5	1	15.5	ns
t _{PHL}				8.4 ⁽¹⁾	13.2 ⁽¹⁾	1 ⁽¹⁾	15.5 ⁽¹⁾	1	15.5	1	15.5	
t _{PLH}	\overline{G}	Y	C _L = 15 pF	8.7 ⁽¹⁾	13.6 ⁽¹⁾	1 ⁽¹⁾	16 ⁽¹⁾	1	16	1	16	ns
t _{PHL}				8.7 ⁽¹⁾	13.6 ⁽¹⁾	1 ⁽¹⁾	16 ⁽¹⁾	1	16	1	16	
t _{PLH}	A or B	Y	C _L = 50 pF	8.7	13.2	1	15	1	15	1	15	ns
t _{PHL}				8.7	13.2	1	15	1	15	1	15	
t _{PLH}	$\overline{A/B}$	Y	C _L = 50 pF	10.9	16.7	1	19	1	19	1	19	ns
t _{PHL}				10.9	16.7	1	19	1	19	1	19	
t _{PLH}	\overline{G}	Y	C _L = 50 pF	11.2	17.1	1	19.5	1	19.5	1	19.5	ns
t _{PHL}				11.2	17.1	1	19.5	1	19.5	1	19.5	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$		$T_A = -55^\circ\text{C TO } 125^\circ\text{C}$		$T_A = -40^\circ\text{C TO } 85^\circ\text{C}$		$T_A = -40^\circ\text{C TO } 125^\circ\text{C}$		UNIT
						Recommended						
				TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	$C_L = 15\text{ pF}$	4.1 ⁽¹⁾	6.4 ⁽¹⁾	1 ⁽¹⁾	7.5 ⁽¹⁾	1	7.5	1	7.5	ns
t_{PHL}				4.1 ⁽¹⁾	6.4 ⁽¹⁾	1 ⁽¹⁾	7.5 ⁽¹⁾	1	7.5	1	7.5	
t_{PLH}	$\overline{A/B}$	Y	$C_L = 15\text{ pF}$	5.3 ⁽¹⁾	8.1 ⁽¹⁾	1 ⁽¹⁾	9.5 ⁽¹⁾	1	9.5	1	9.5	ns
t_{PHL}				5.3 ⁽¹⁾	8.1 ⁽¹⁾	1 ⁽¹⁾	9.5 ⁽¹⁾	1	9.5	1	9.5	
t_{PLH}	\overline{G}	Y	$C_L = 15\text{ pF}$	5.6 ⁽¹⁾	8.6 ⁽¹⁾	1 ⁽¹⁾	10 ⁽¹⁾	1	10	1	10	ns
t_{PHL}				5.6 ⁽¹⁾	8.6 ⁽¹⁾	1 ⁽¹⁾	10 ⁽¹⁾	1	10	1	10	
t_{PLH}	A or B	Y	$C_L = 50\text{ pF}$	5.6 ⁽¹⁾	8.4 ⁽¹⁾	1 ⁽¹⁾	9.5 ⁽¹⁾	1	9.5	1	9.5	ns
t_{PHL}				5.6 ⁽¹⁾	8.4 ⁽¹⁾	1 ⁽¹⁾	9.5 ⁽¹⁾	1	9.5	1	9.5	
t_{PLH}	$\overline{A/B}$	Y	$C_L = 50\text{ pF}$	6.8 ⁽¹⁾	10.1 ⁽¹⁾	1 ⁽¹⁾	11.5 ⁽¹⁾	1	11.5	1	11.5	ns
t_{PHL}				6.8 ⁽¹⁾	10.1 ⁽¹⁾	1 ⁽¹⁾	11.5 ⁽¹⁾	1	11.5	1	11.5	
t_{PLH}	\overline{G}	Y	$C_L = 50\text{ pF}$	7.1 ⁽¹⁾	10.6 ⁽¹⁾	1 ⁽¹⁾	12 ⁽¹⁾	1	12	1	12	ns
t_{PHL}				7.1 ⁽¹⁾	10.6 ⁽¹⁾	1 ⁽¹⁾	12 ⁽¹⁾	1	12	1	12	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

NOISE CHARACTERISTICS

$V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ ⁽¹⁾

PARAMETER		SN74AHC157			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}			0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}			-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.8		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

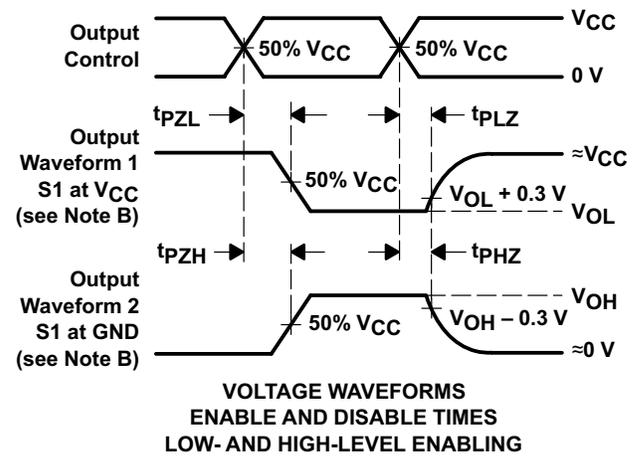
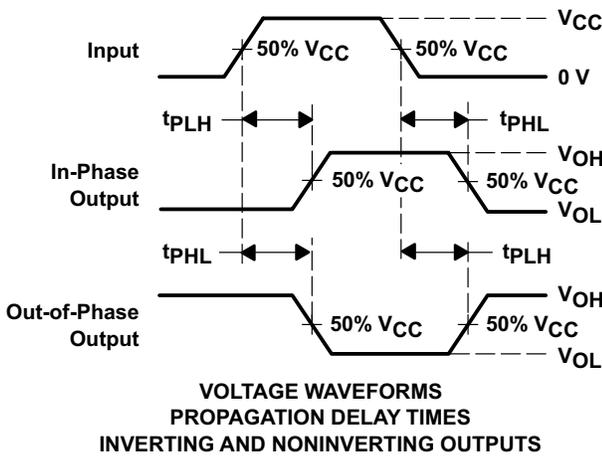
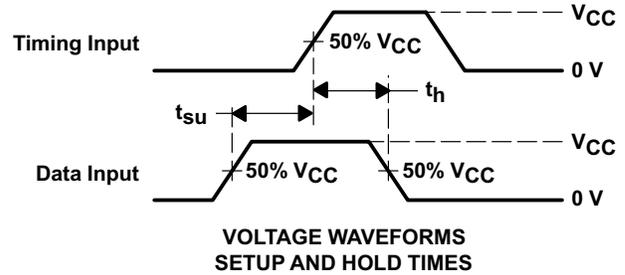
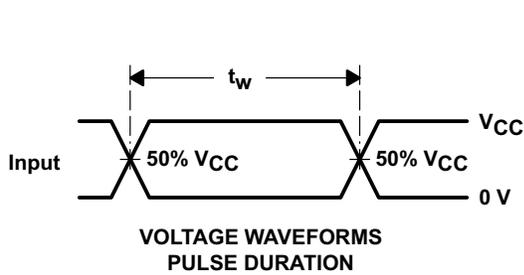
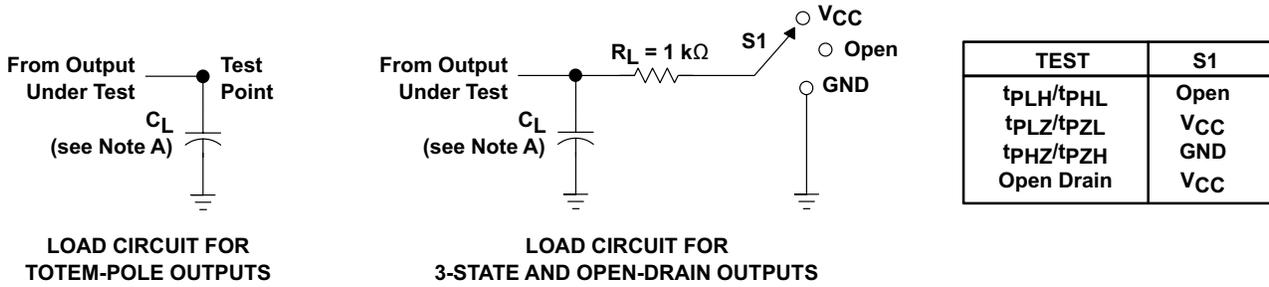
(1) Characteristics are for surface-mount packages only.

OPERATING CHARACTERISTICS

$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd}	No load, $f = 1\text{ MHz}$	11	pF

PARAMETER MEASUREMENT INFORMATION



- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

REVISION HISTORY

Changes from Revision I (May 1996) to Revision J	Page
• Changed document format from Quicksilver to DocZone.	1
• Extended operating temperature range to 125°C	3

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9764201Q2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9764201Q2A SNJ54AHC 157FK	Samples
5962-9764201QEA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9764201QE A SNJ54AHC157J	Samples
5962-9764201QFA	ACTIVE	CFP	W	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9764201QF A SNJ54AHC157W	Samples
SN74AHC157D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC157	Samples
SN74AHC157DBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA157	Samples
SN74AHC157DGVR	ACTIVE	TVSOP	DGV	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA157	Samples
SN74AHC157DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC157	Samples
SN74AHC157N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	SN74AHC157N	Samples
SN74AHC157NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC157	Samples
SN74AHC157PW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA157	Samples
SN74AHC157PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA157	Samples
SN74AHC157PWRG3	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	HA157	Samples
SN74AHC157RGYR	ACTIVE	VQFN	RGY	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HA157	Samples
SNJ54AHC157FK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9764201Q2A SNJ54AHC 157FK	Samples
SNJ54AHC157J	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9764201QE A SNJ54AHC157J	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ54AHC157W	ACTIVE	CFP	W	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9764201QF A SNJ54AHC157W	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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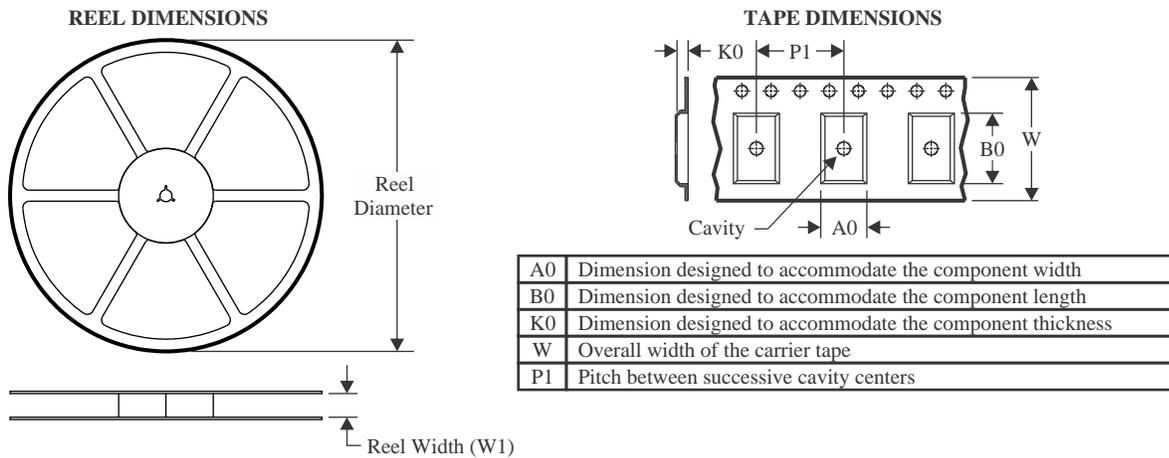
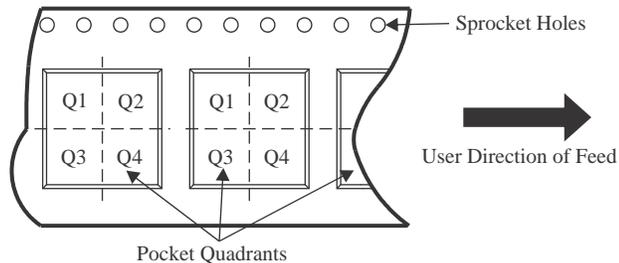
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54AHC157, SN74AHC157 :

- Catalog : [SN74AHC157](#)
- Military : [SN54AHC157](#)

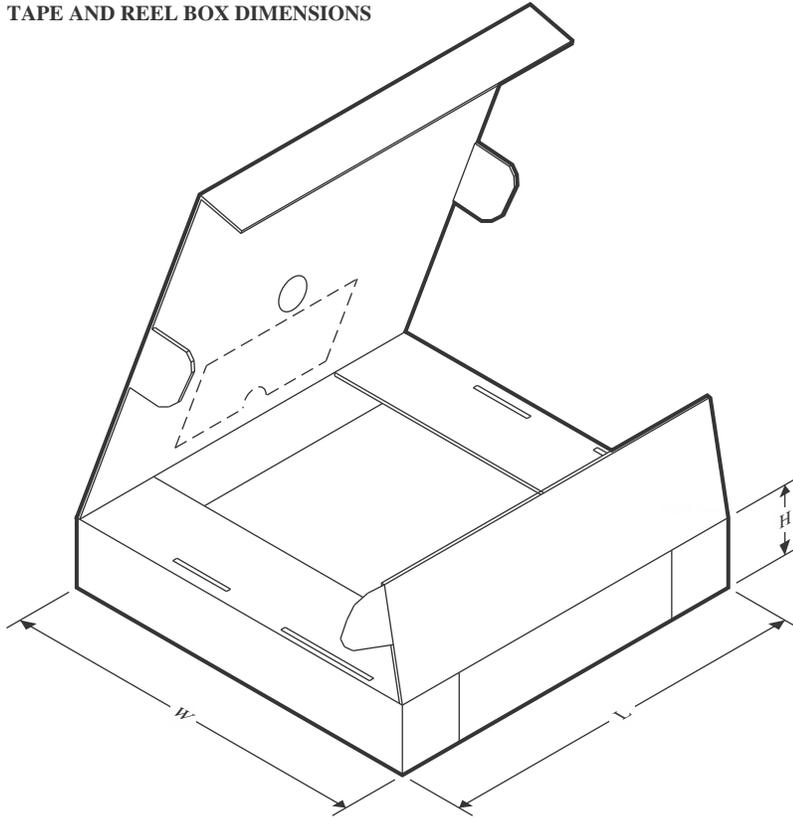
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


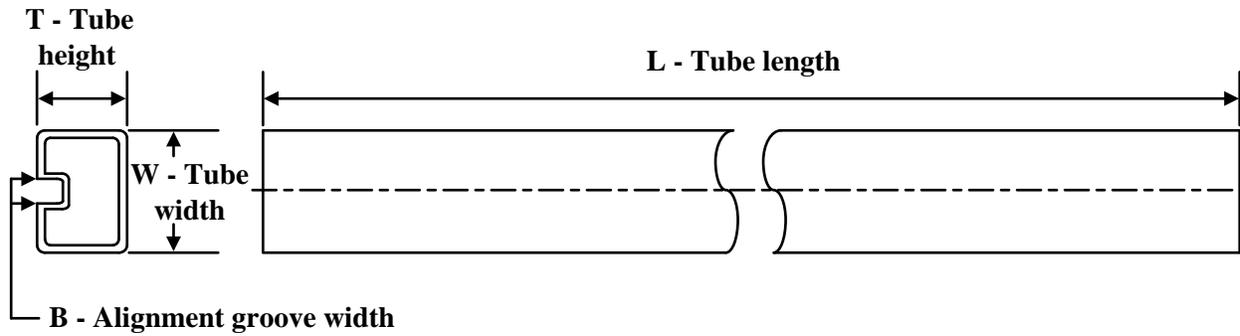
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC157DBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHC157DGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AHC157DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74AHC157NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74AHC157PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC157PWRG3	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC157RGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC157DBR	SSOP	DB	16	2000	356.0	356.0	35.0
SN74AHC157DGVR	TVSOP	DGV	16	2000	356.0	356.0	35.0
SN74AHC157DR	SOIC	D	16	2500	340.5	336.1	32.0
SN74AHC157NSR	SO	NS	16	2000	356.0	356.0	35.0
SN74AHC157PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74AHC157PWRG3	TSSOP	PW	16	2000	364.0	364.0	27.0
SN74AHC157RGYR	VQFN	RGY	16	3000	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9764201Q2A	FK	LCCC	20	1	506.98	12.06	2030	NA
5962-9764201QFA	W	CFP	16	1	506.98	26.16	6220	NA
SN74AHC157D	D	SOIC	16	40	507	8	3940	4.32
SN74AHC157N	N	PDIP	16	25	506	13.97	11230	4.32
SN74AHC157N	N	PDIP	16	25	506	13.97	11230	4.32
SN74AHC157PW	PW	TSSOP	16	90	530	10.2	3600	3.5
SNJ54AHC157FK	FK	LCCC	20	1	506.98	12.06	2030	NA
SNJ54AHC157W	W	CFP	16	1	506.98	26.16	6220	NA

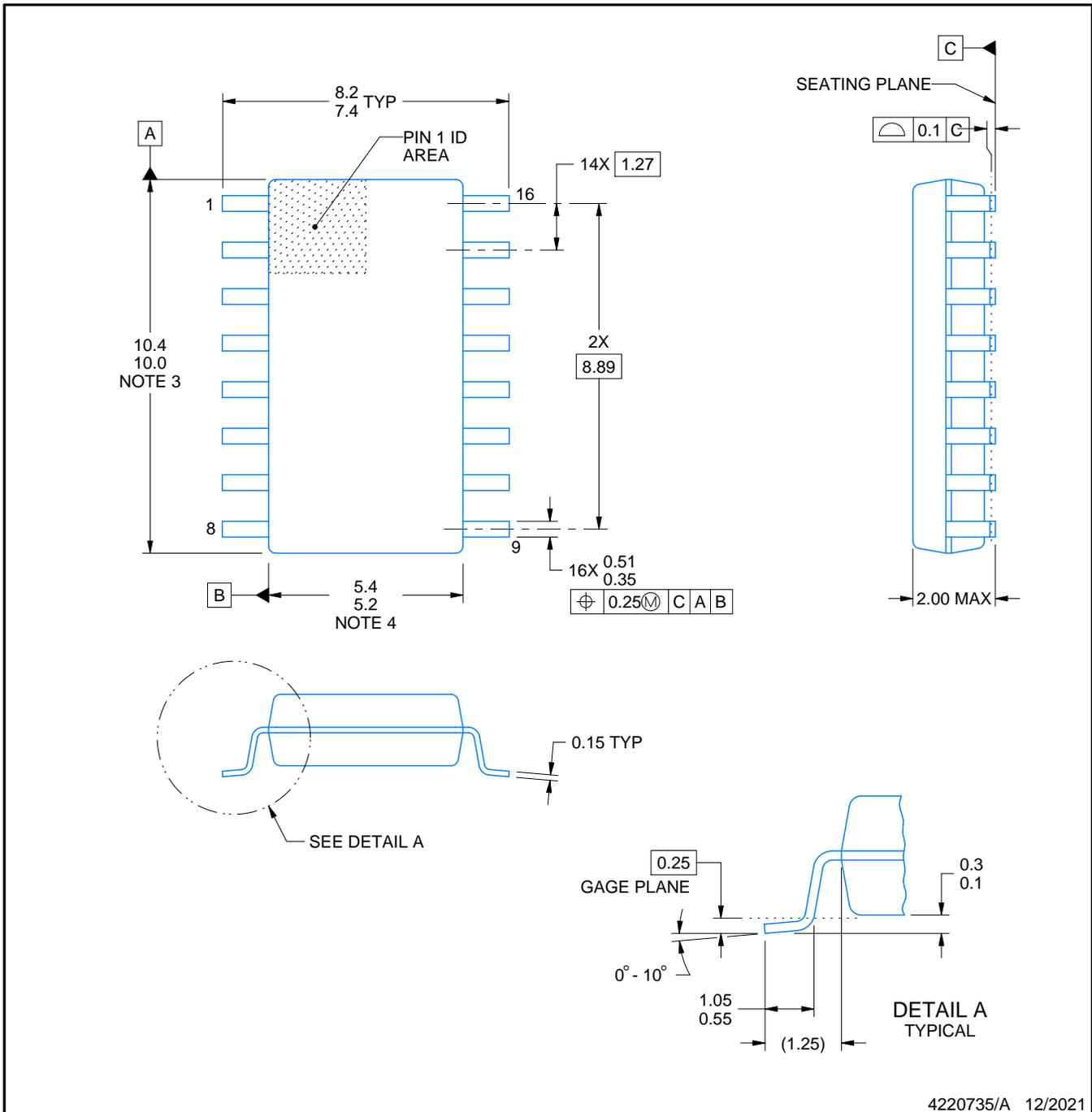


PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES:

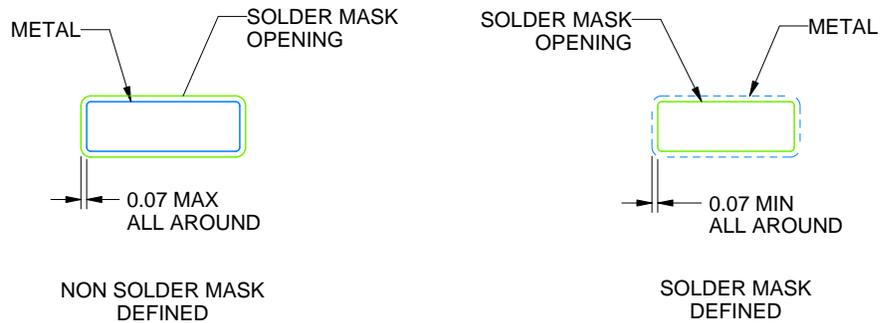
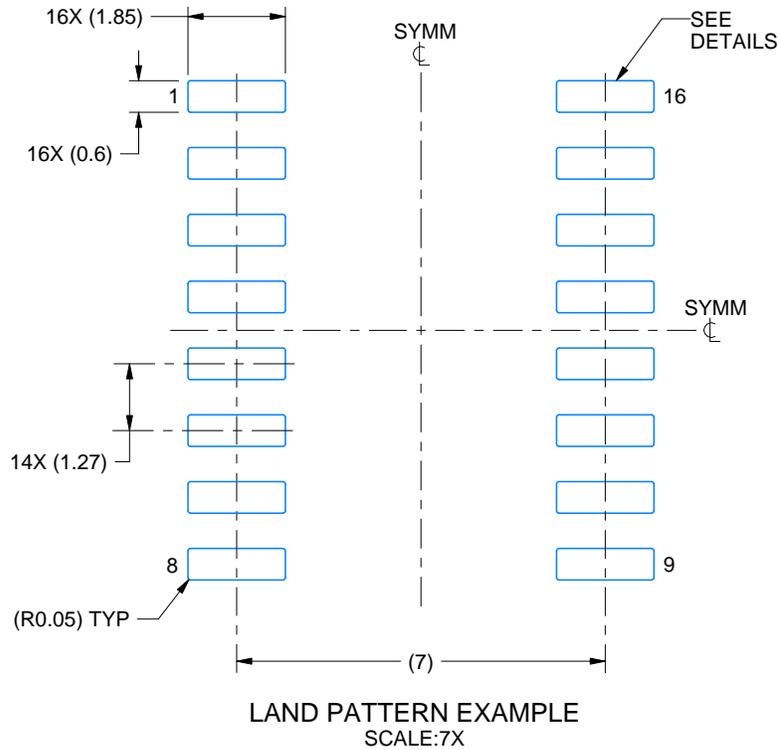
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES: (continued)

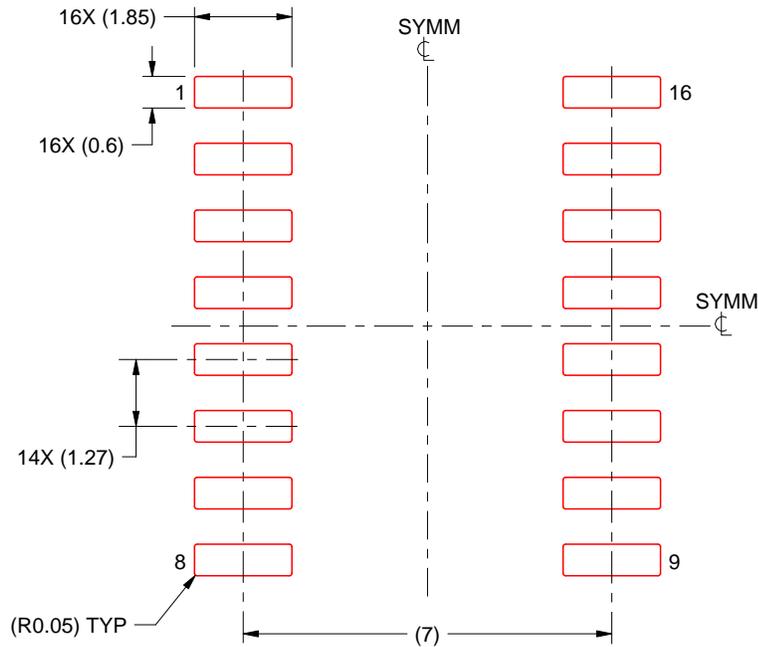
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

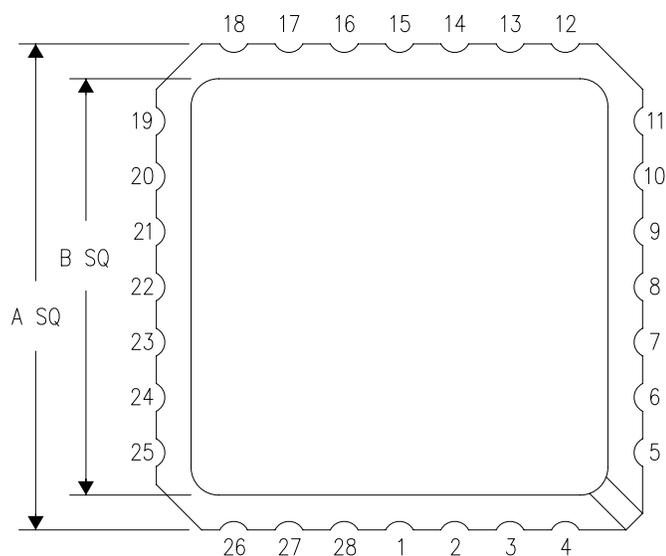
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

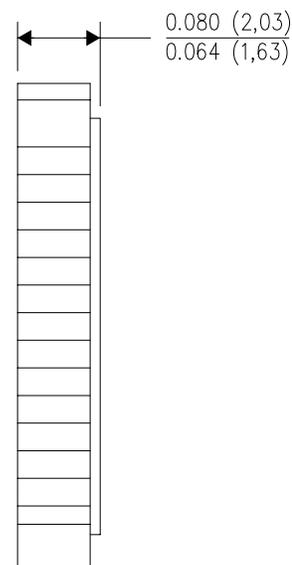
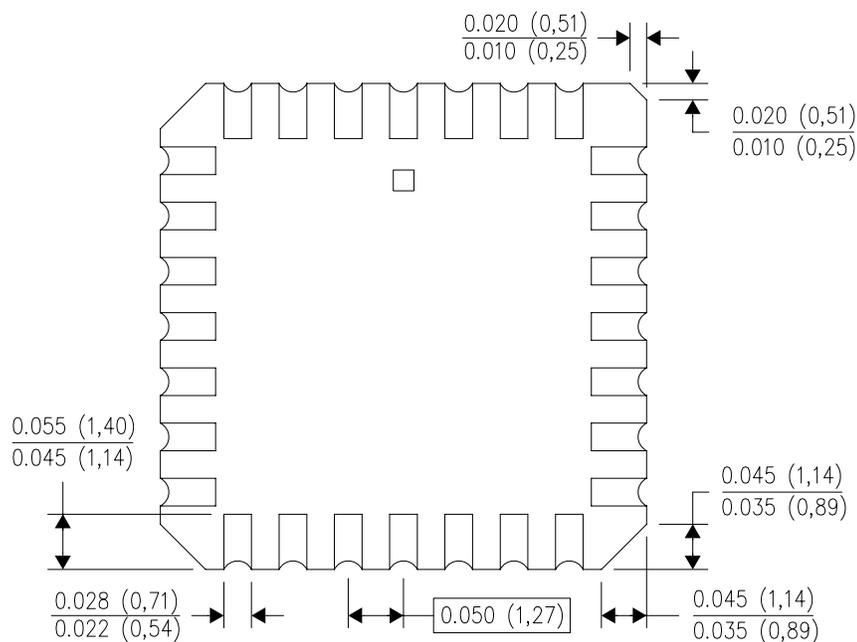
FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

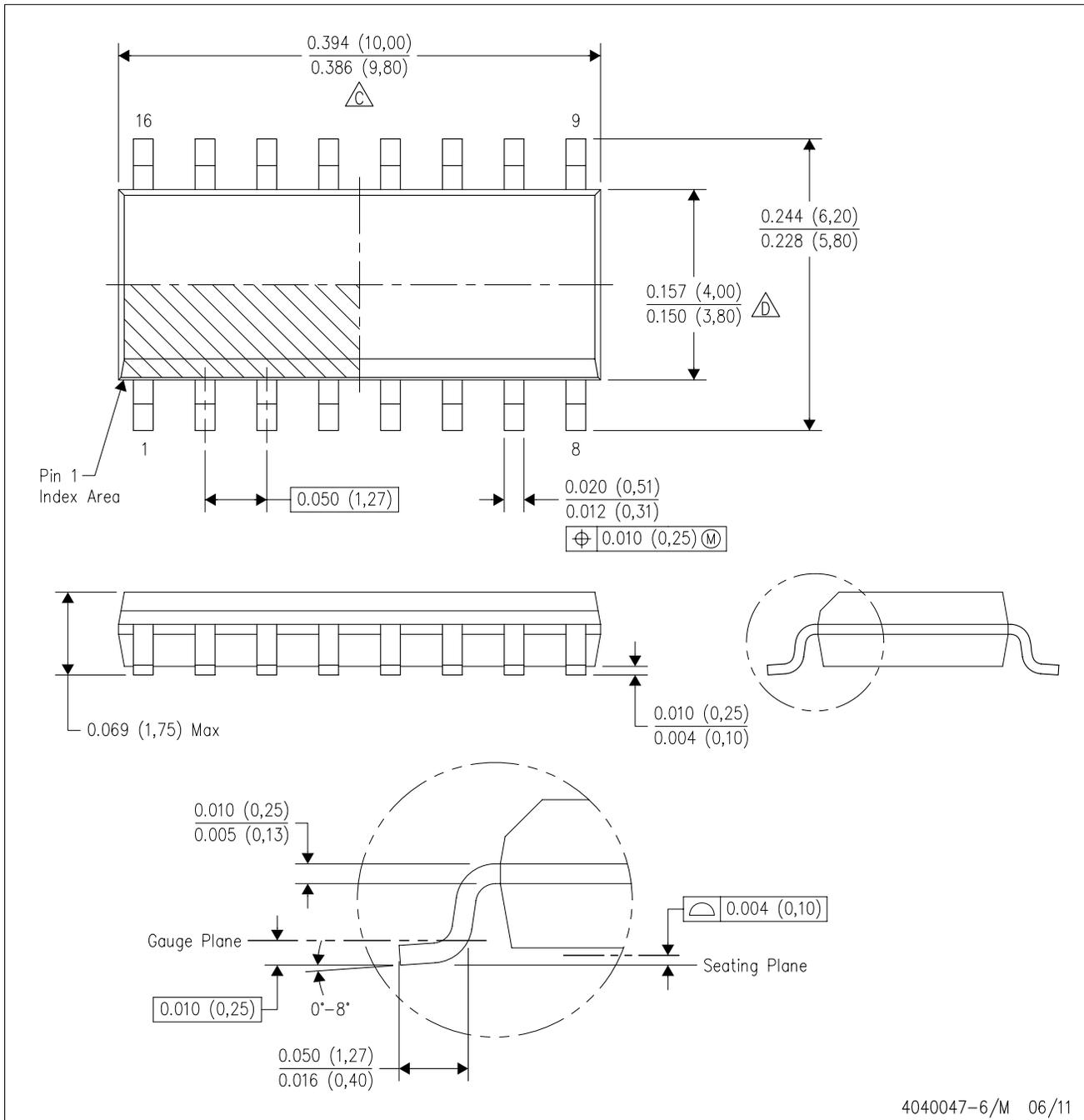


4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

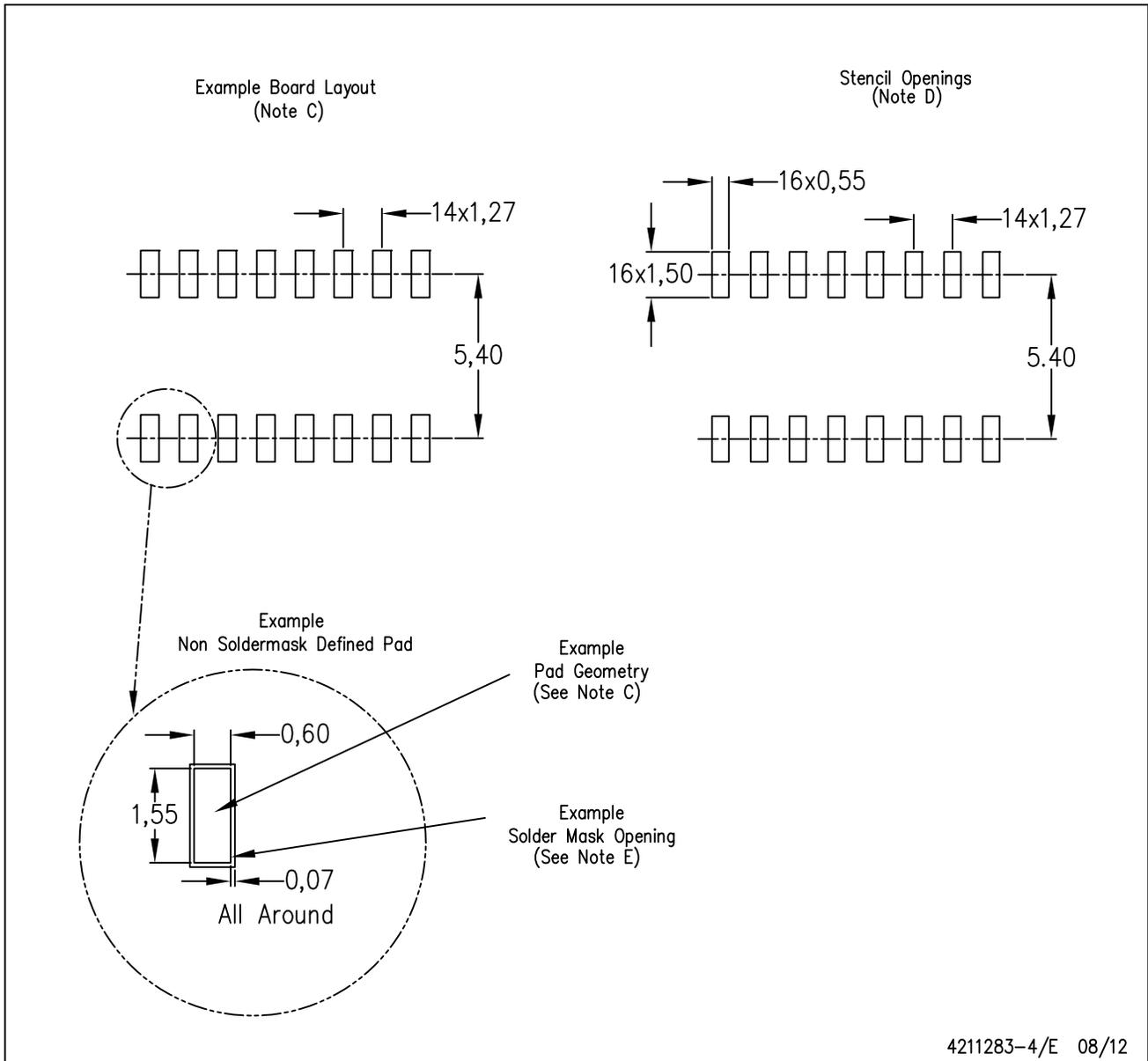


4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

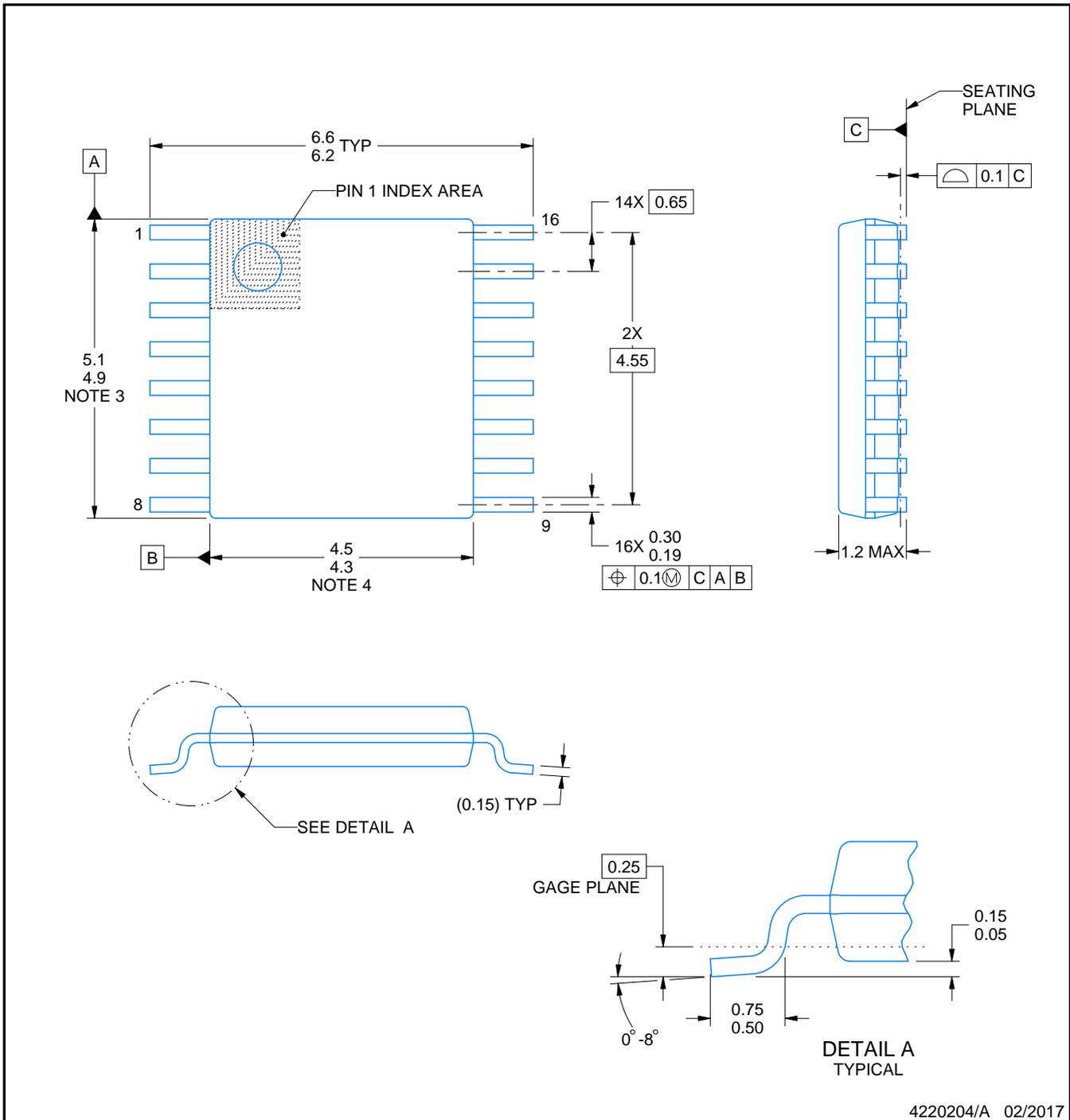
D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4211283-4/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



4220204/A 02/2017

NOTES:

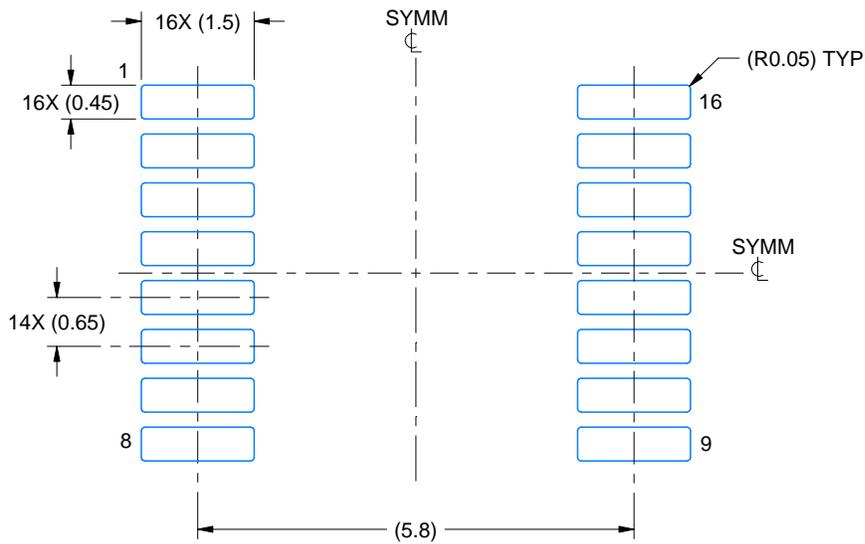
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

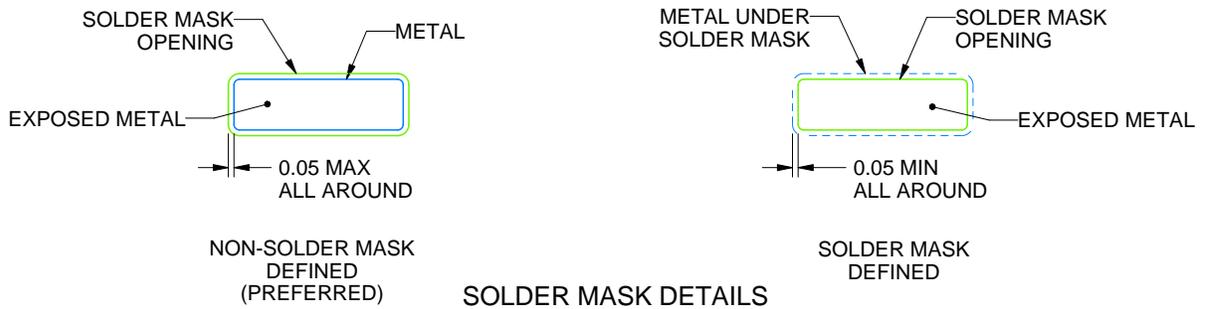
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

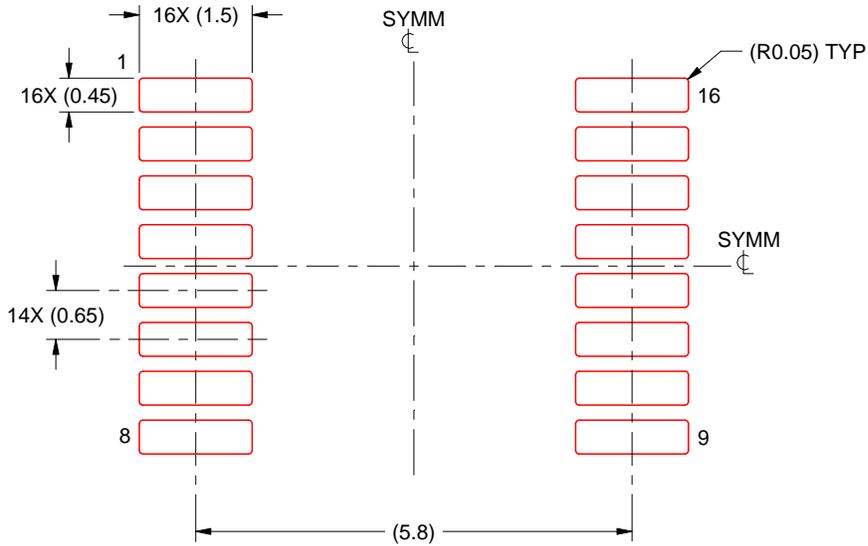
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

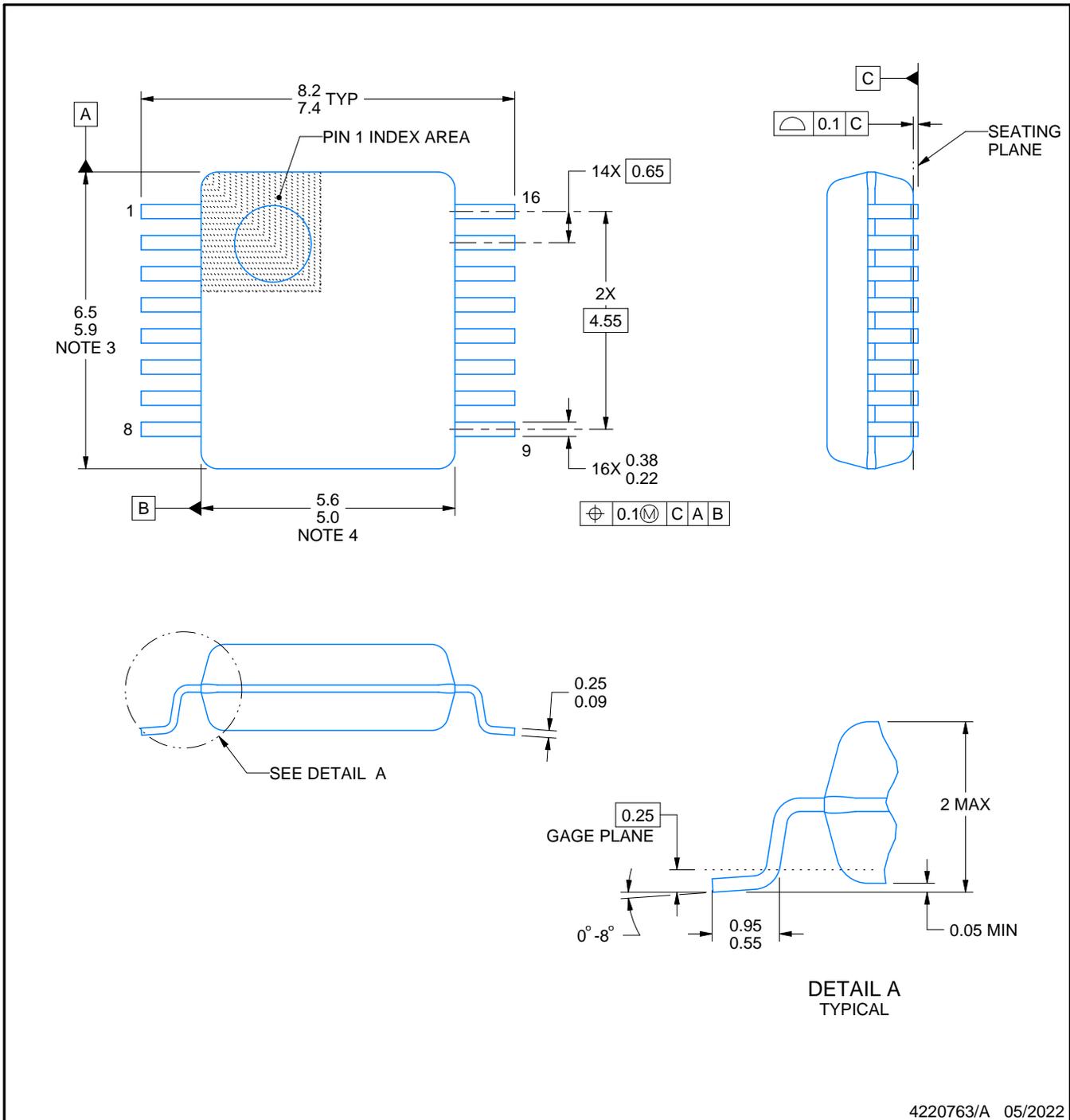
DB0016A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4220763/A 05/2022

NOTES:

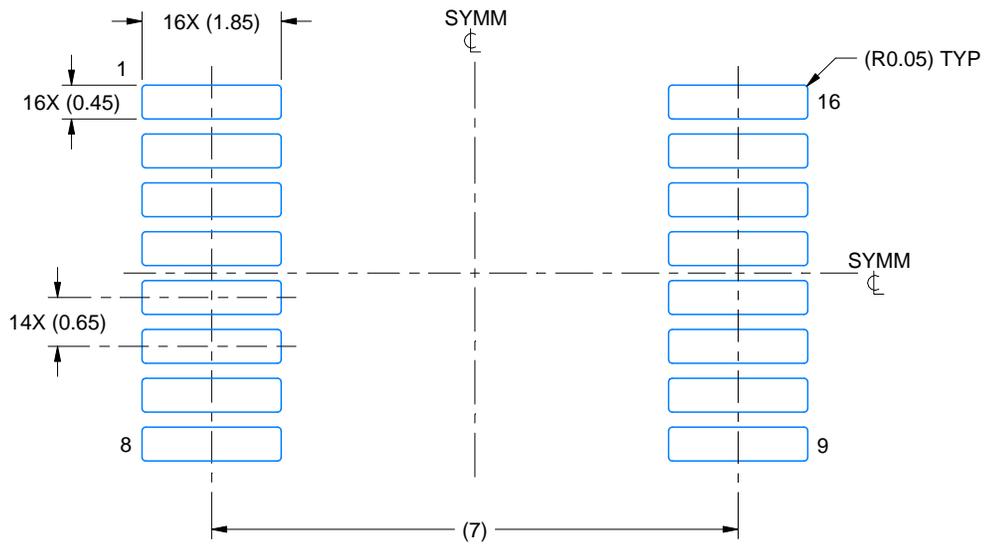
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

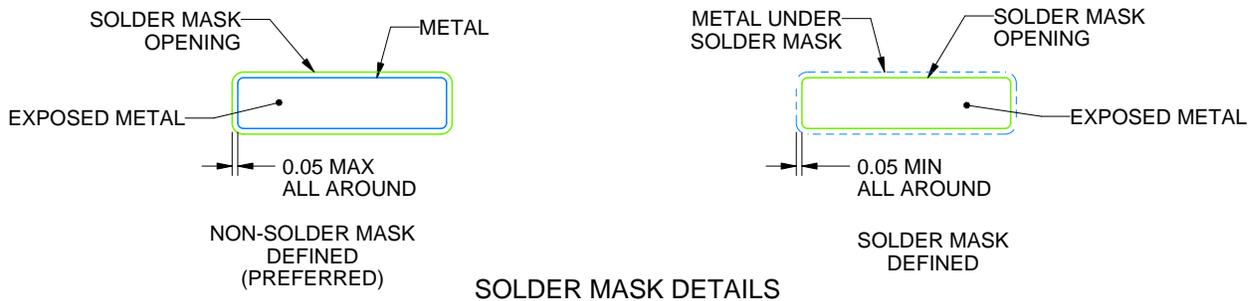
DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220763/A 05/2022

NOTES: (continued)

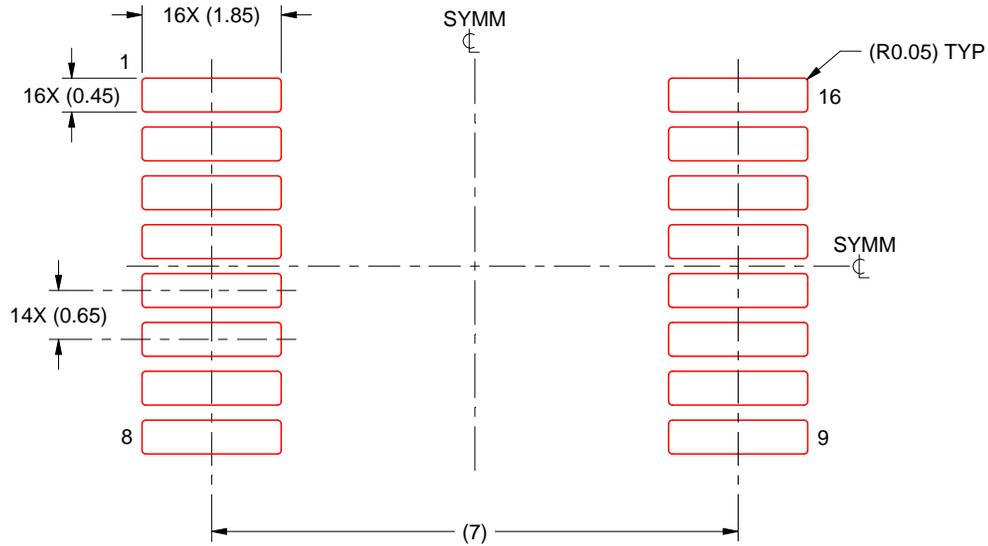
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

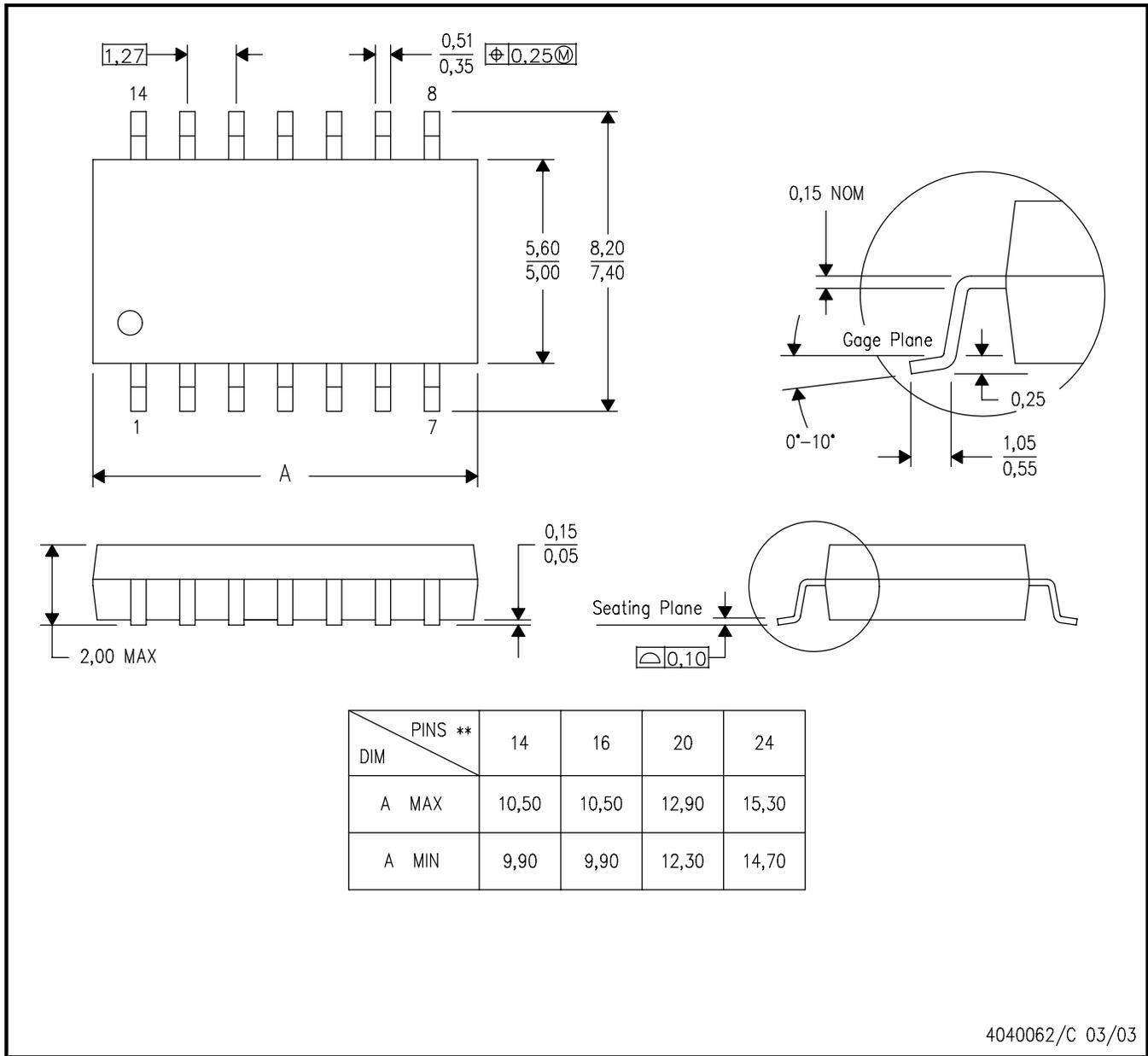
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

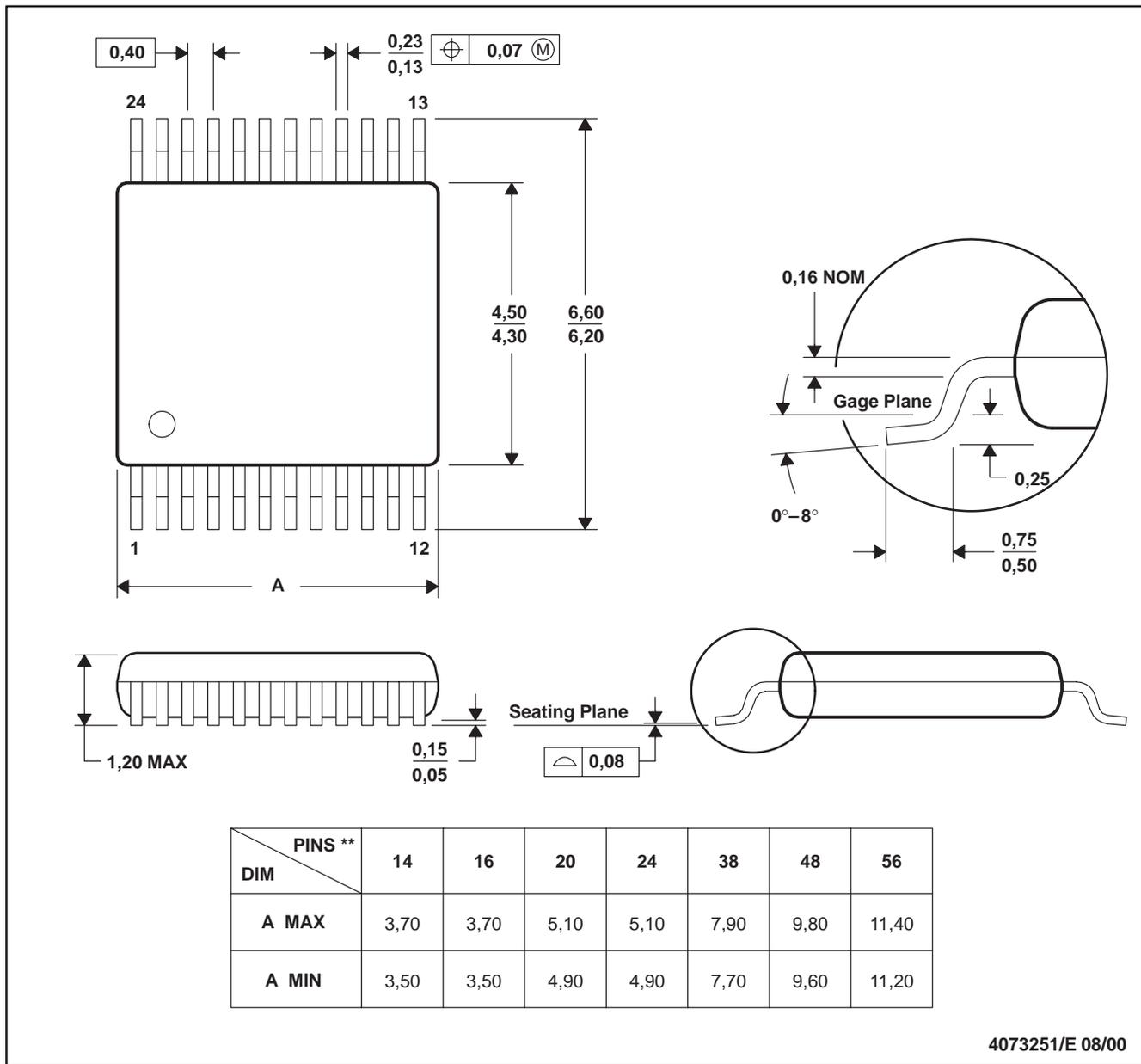


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

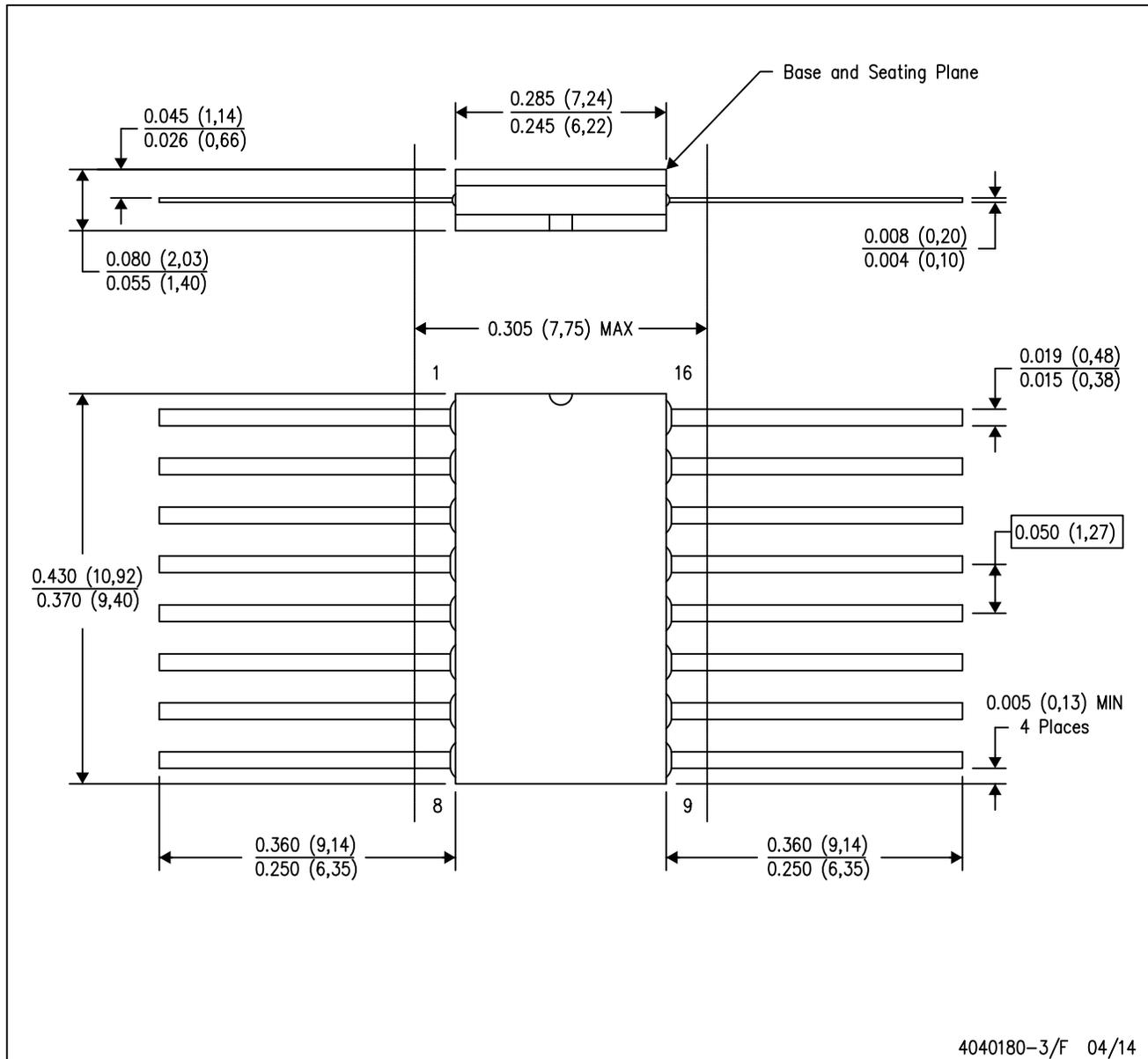
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK

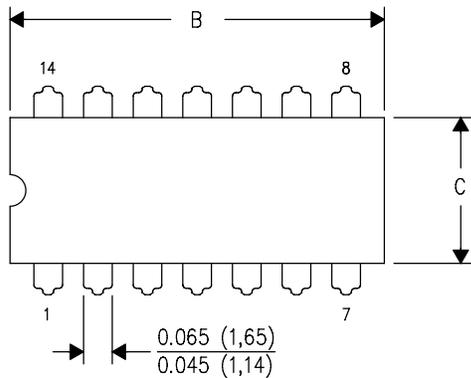


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP2-F16

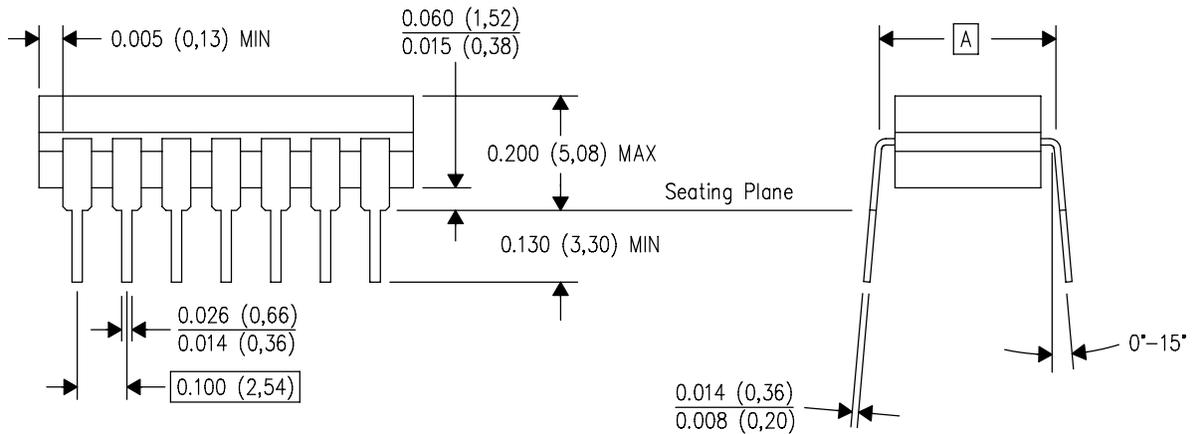
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



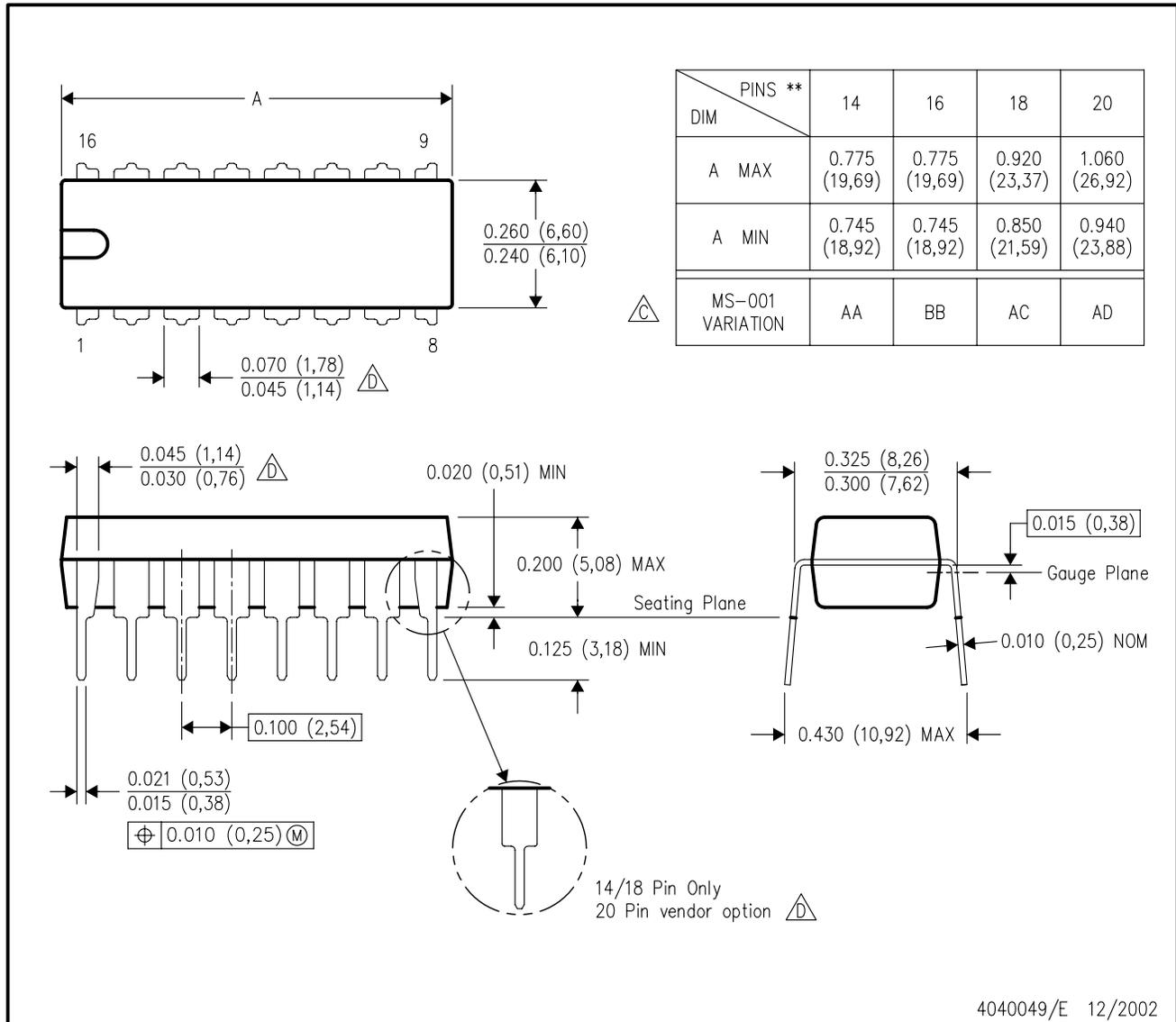
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

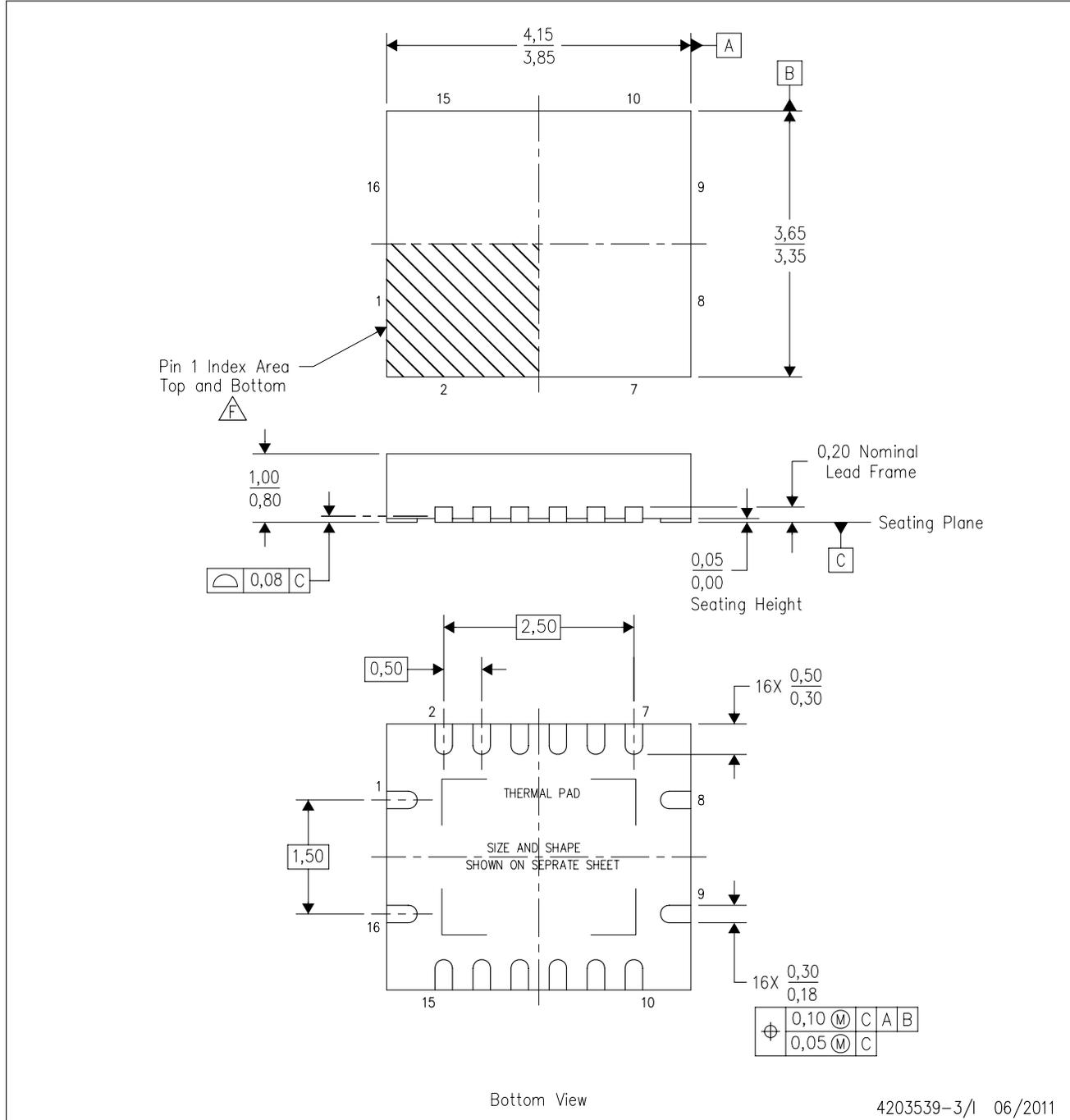


4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
 - G. Package complies to JEDEC MO-241 variation BA.

RGY (R-PVQFN-N16)

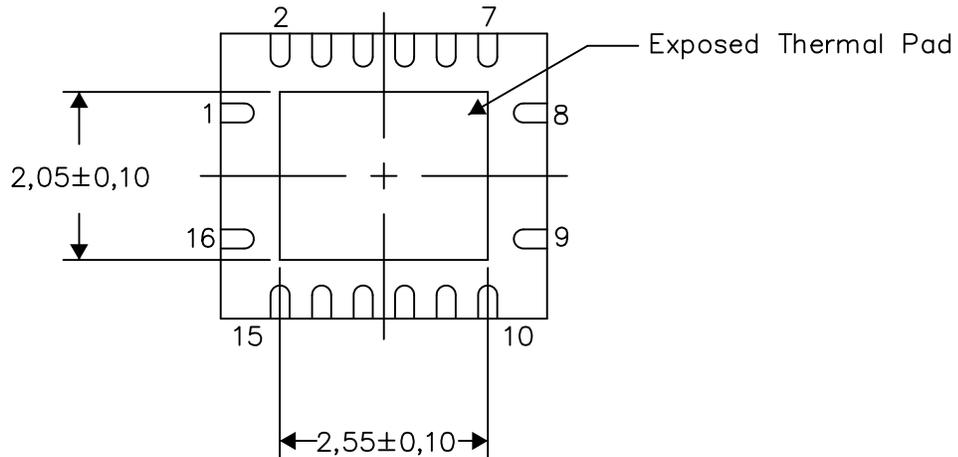
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

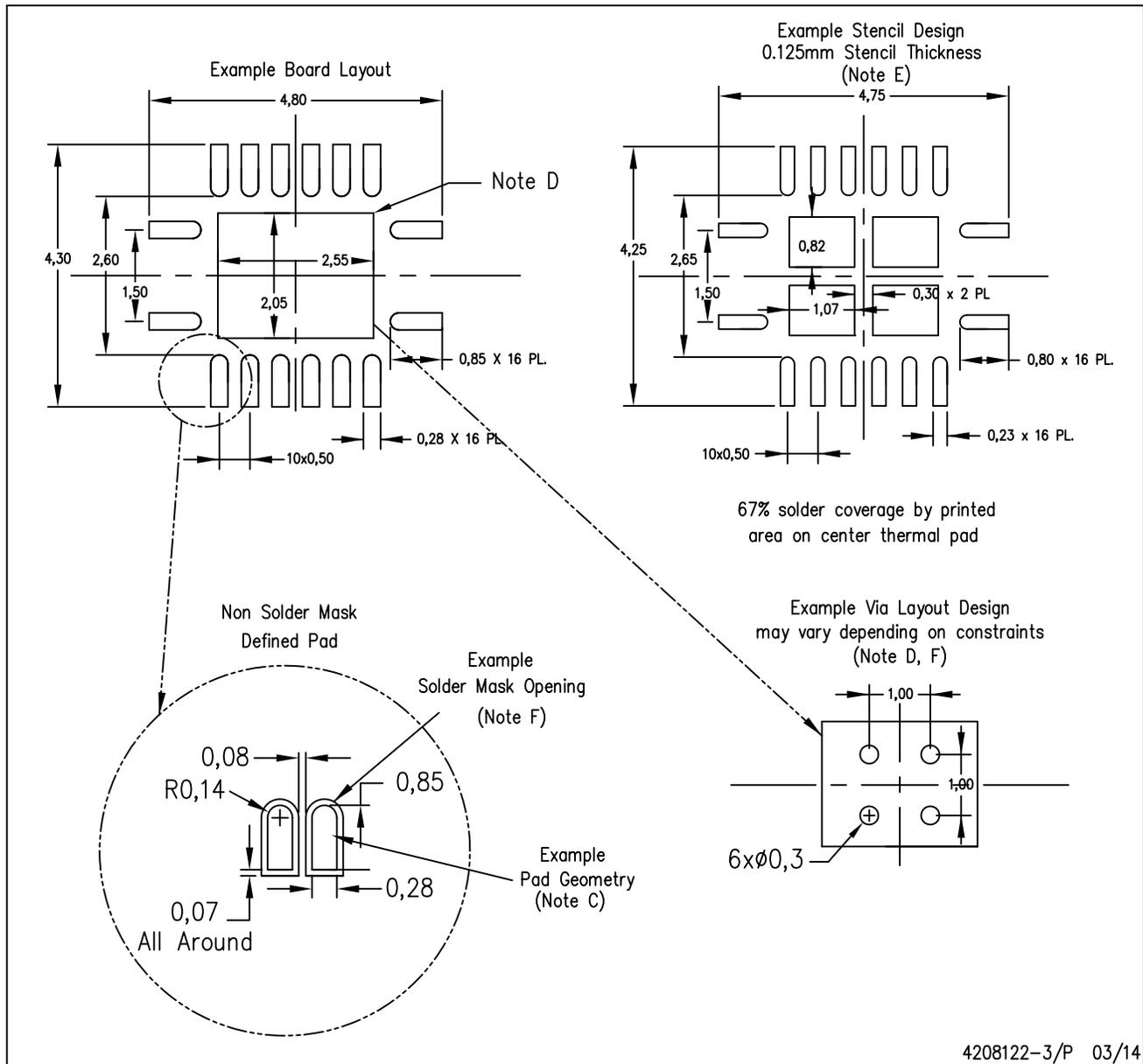
Exposed Thermal Pad Dimensions

4206353-3/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4208122-3/P 03/14

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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