ANALOG DEVICES

HMC7149

v02.0815

RoHS EARTH FRIENDLY

10 WATT GaN MMIC POWER AMPLIFIER, 6 - 18 GHz

Typical Applications

The HMC7149 is ideal for:

- Test Instrumentation
- General Communications
- Radar

Features

High Psat: +40 dBm

Power Gain at Psat: +10 dB

High Output IP3: +39.5 dBm

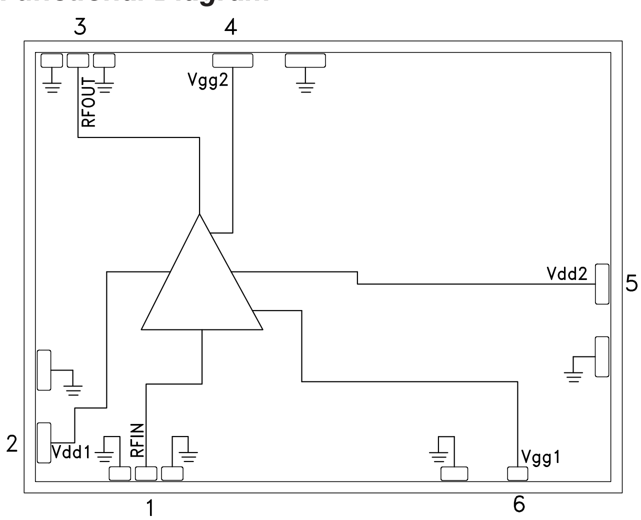
Small Signal Gain: 20 dB

Supply Voltage: +28 V @ 680 mA

50 Ohm Matched Input/Output

Die Size: 3.4 x 4.5 x 0.1 mm

Functional Diagram



General Description

The HMC7149 is an 10W Gallium Nitride (GaN) MMIC Power Amplifier which operates between 6 and 18 GHz. The amplifier typically provides 20dB of small signal gain, +40 dBm of saturated output power, and +39.5 dBm output IP3 at +28 dBm output power per tone. The HMC7149 draws 680 mA current from a +28V DC supply. The RF I/Os are matched to 50 Ohms for ease of integration into Multi-Chip-Modules (MCMs). All electrical performance data was aquired with the die eutectically attached to 1.02 mm (40 mil) thick CuMo carrier with multiple 1.0 mil diameter ball bonds connecting the die to 50 Ohm transmission lines on alumina.

Electrical Specifications, Tc = +25°C, Vdd= Vdd1 =Vdd2 = +28 V, Idd = 680 mA [1]

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency Range		6 - 10			10 - 14			14 - 16			16 - 18		GHz
Small Signal Gain	19	21		18	20		17	19		18	20		dB
Gain Flatness		±0.5			±0.6			±0.5			±0.7		dB
Gain Variation Over Temperature		0.023			0.02			0.02			0.018		dB/ °C
Input Return Loss		17			17			16			11		dB
Output Return Loss		17			17			18			12		dB
Output Power for 4 dB Compression (P4dB)		35			35			35			36		dBm
Power Gain for 4 dB compression (P4dB)		17			16			15			17		dB
Saturated Output Power (Psat)		40			40			40			40		dBm
Output Third Order Intercept (IP3) [2]		39.5			39			39.5			40.5		dBm
Power Added Efficiency		22			20			20			20		%
Supply Current (Idd @ Vdd = 28V)		680			680			680			680		mA

[1] Adjust Vgg between -3V and 0V to achieve Idd= 680 mA typical.

[2] Measurement taken at 28V @ 680 mA, Pout/tone = +28 dBm.

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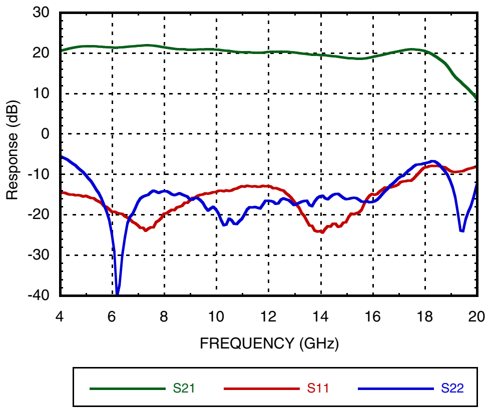
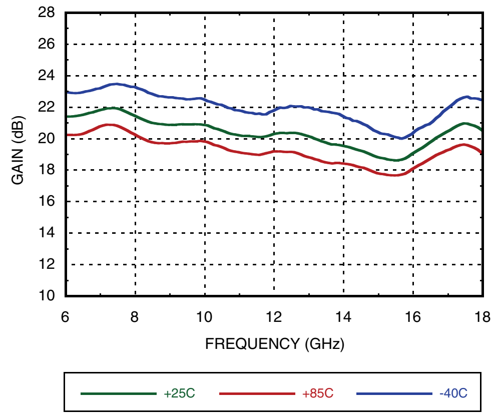
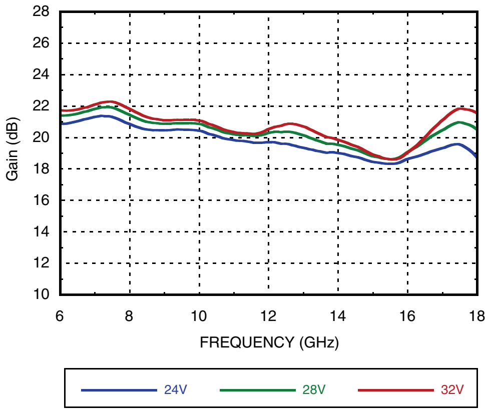
Gain and Return Loss



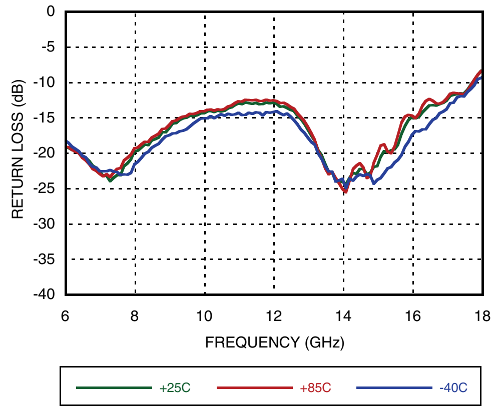
Gain vs. Temperature



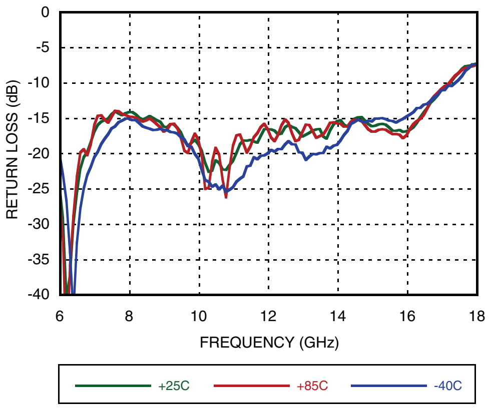
Gain vs. Vdd



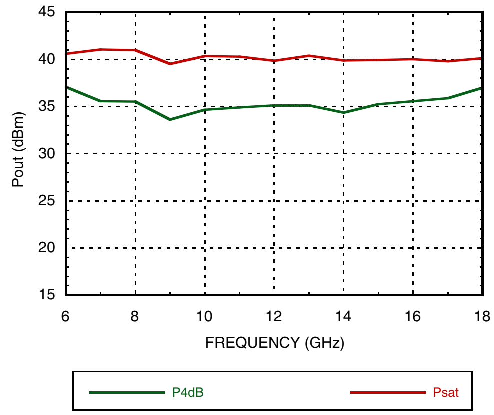
Input Return Loss vs. Temperature



Output Return Loss vs. Temperature



Pout vs. Frequency



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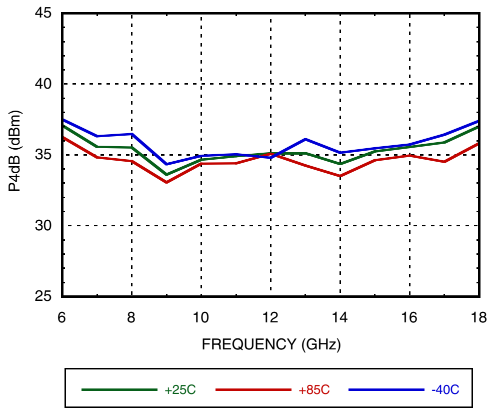
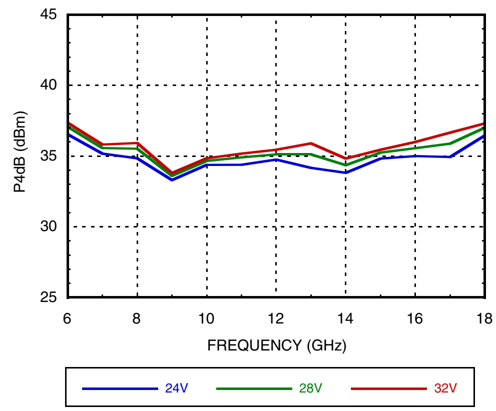
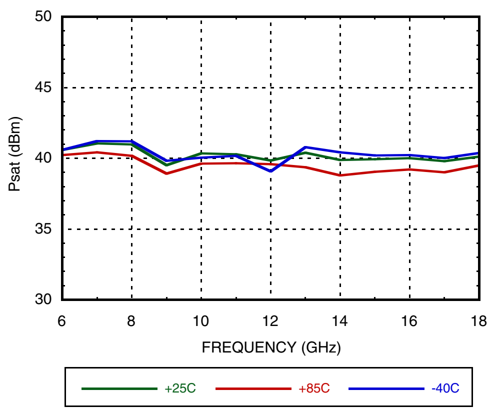
P4dB vs. Temperature



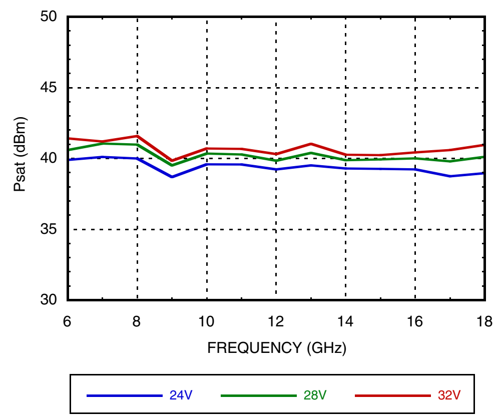
P4dB vs. Supply Voltage



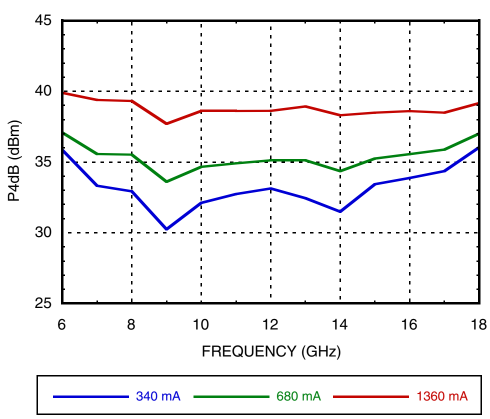
Psat vs. Temperature



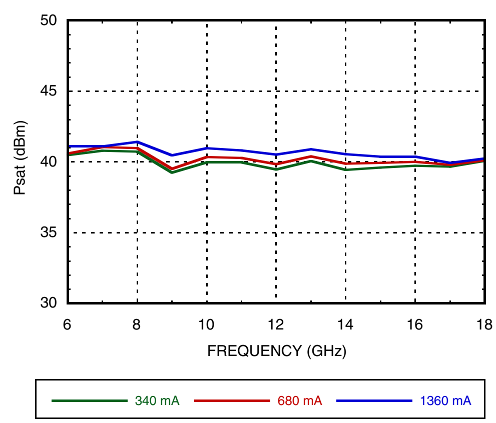
Psat vs. Supply Voltage



P4dB vs. Supply Current



Psat vs. Supply Curent



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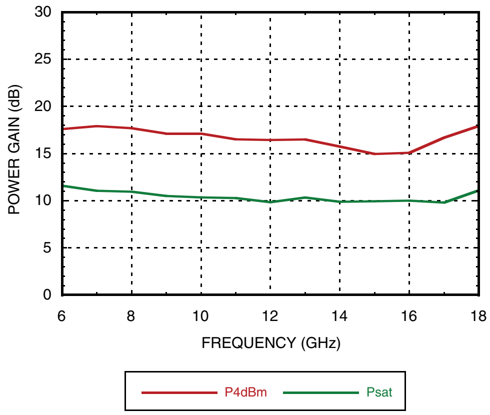
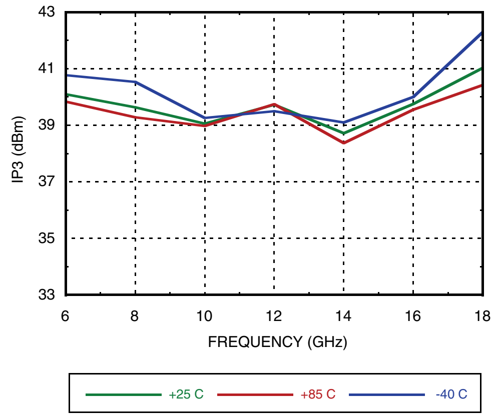
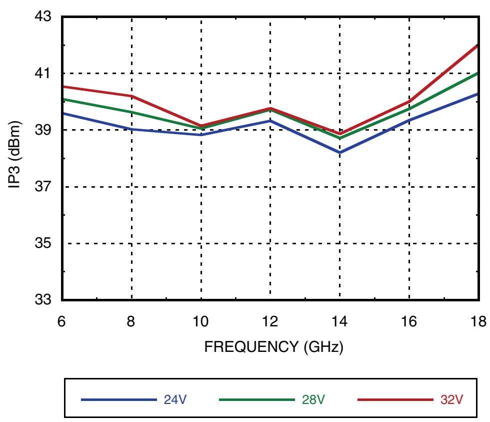
Power Gain vs. Frequency



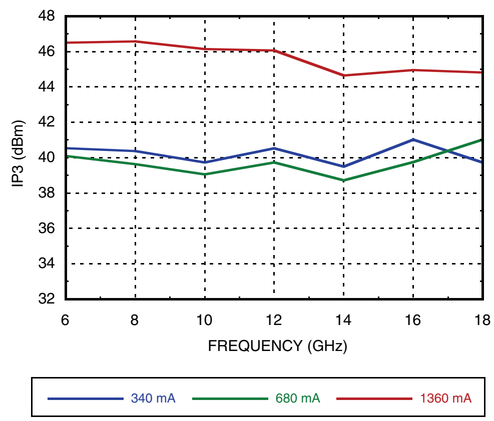
Output IP3 vs. Temperature Pout/tone = +28 dBm



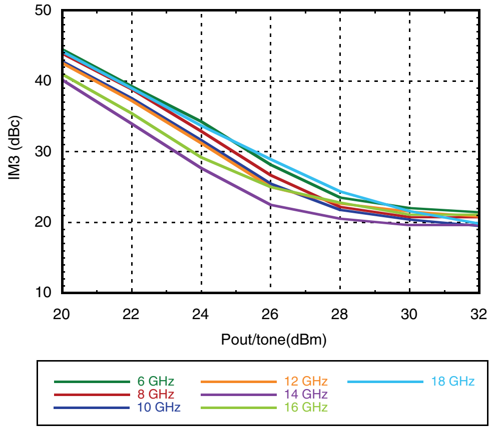
Output IP3 vs. Supply Voltage Pout/tone = +28 dBm



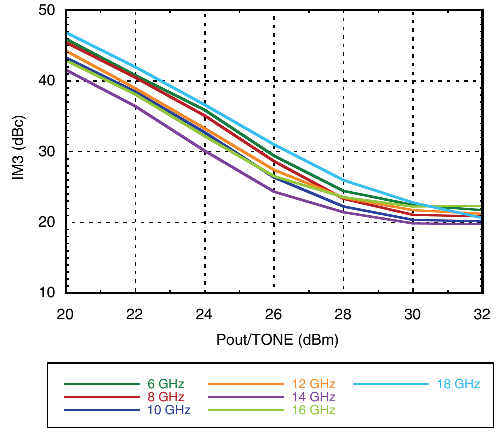
Output IP3 vs. Supply Current Pout/tone = +28 dBm



Output IM3 @ Vdd= +24V



Output IM3 @ Vdd= +28V



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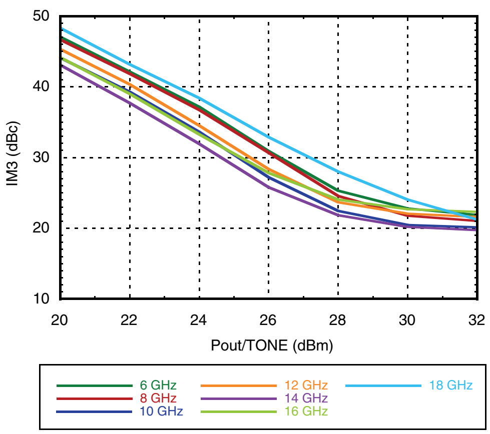
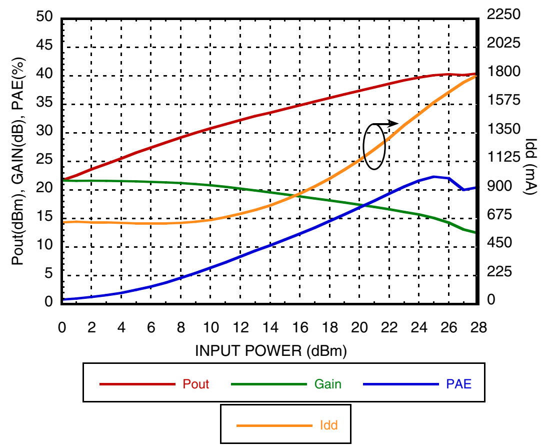
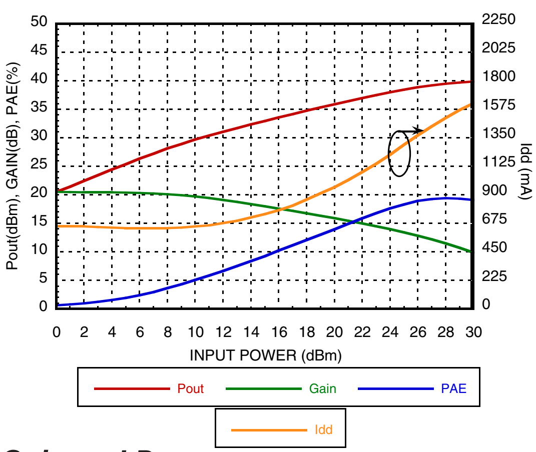
Output IM3 @ Vdd= +32V



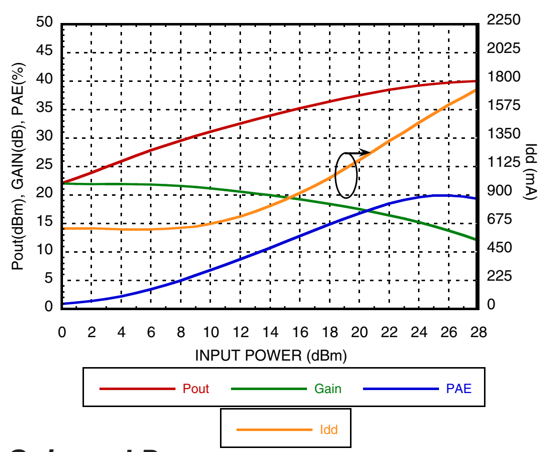
Power Compression @ 6 GHz



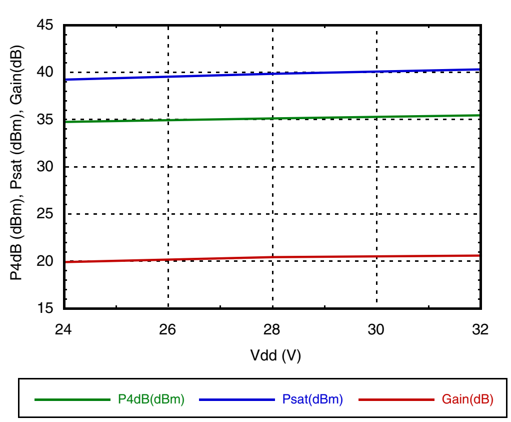
Power Compression @ 12 GHz



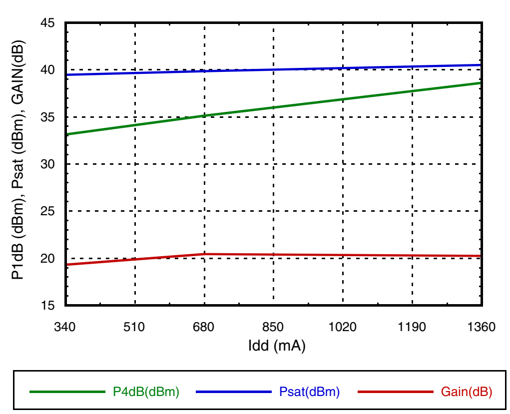
Power Compression @ 18 GHz



Gain and Power vs. Supply Voltage @ 12 GHz



Gain and Power vs. Supply Curent @ 12 GHz



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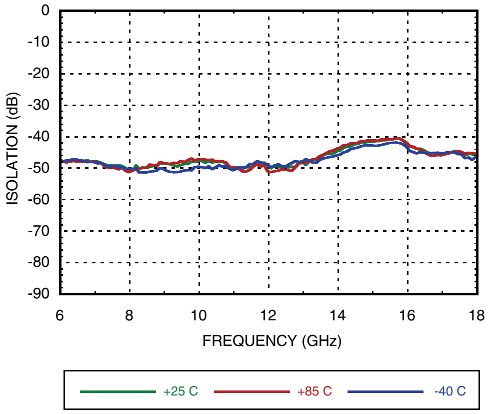
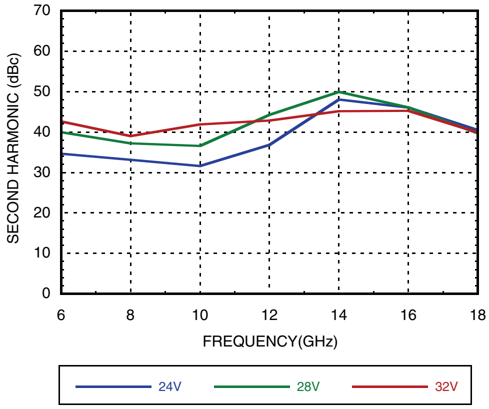
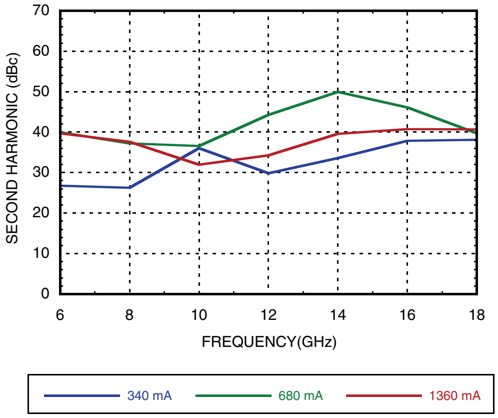
Reverse Isolation vs. Temperature



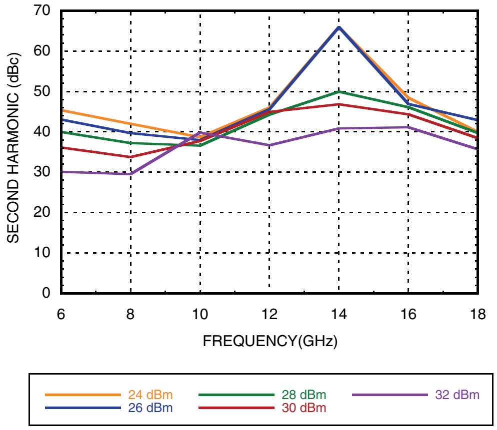
Second Harmonomics vs. Supply Voltage



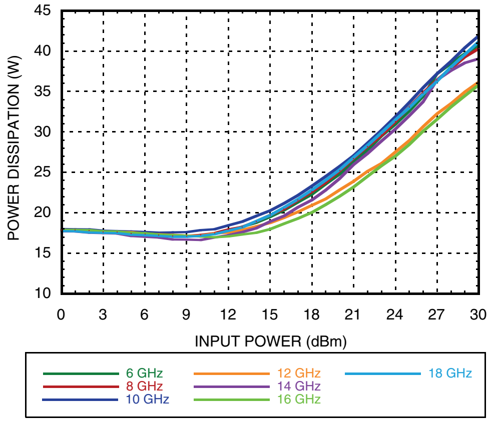
Second Harmomonics vs. Supply Current



Second Harmomonics vs. Pout



Power Dissipation



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Absolute Maximum Ratings[1]

Drain Bias Voltage (Vdd)	+32V
Gate Bias Voltage (Vgg)	-8V to +0V
Maximum Forward Gate Current	6 mA
Maximum RF Input Power (RFIN)	30 dBm
Maximum Junction Temperature (Tj)	225 °C
Maximum Pdiss (T=85°C) (Derate 357 mW/°C above 85°C)	50 W
Thermal Resistance [2]	2.8 °C/W
Maximum VSWR [3]	6:1
Storage Temperature	-55 to +150 °C
Operating Temperature	-40 to +85 °C

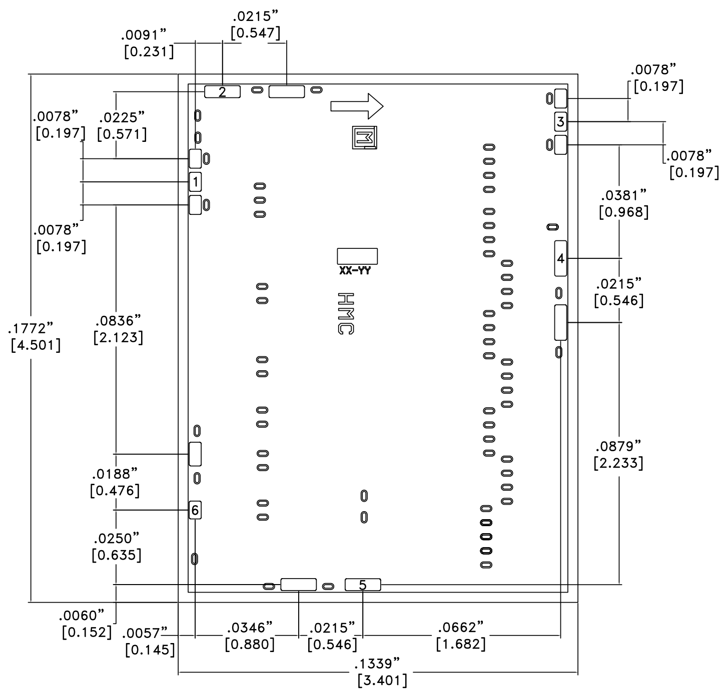
Typical Supply Current vs. Vdd

Vdd (V)	Idd (mA)
+28.0	680

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

[1] Operation outside parameter ranges above can cause permanent damage to the device. These are maximum stress ratings only. Continuous operation of the device at these conditions is not implied.
[2] Assumes 1mil AuSn die attach to a 40mil CuMo Carrier with 85°C at the back of the carrier.
[3] Restricted by maximum power dissipation

Outline Drawing



Die Packaging Information [1]

Standard	Alternate
GP-1 (Gel Pack)	[2]

[1] Refer to the “Packaging Information” section for die packaging dimensions.
[2] For alternate packaging information contact Hittite Microwave Corporation.

NOTES:
1. ALL DIMENSIONS ARE IN INCHES [MM]
2. DIE THICKNESS IS .004”
3. TYPICAL BOND PAD IS .004” SQUARE
4. BACKSIDE METALLIZATION: GOLD
5. BOND PAD METALLIZATION: GOLD
6. BACKSIDE METAL IS GROUND.
7. CONNECTION NOT REQUIRED FOR UNLABELED BOND PADS.
8. OVERALL DIE SIZE ± .002

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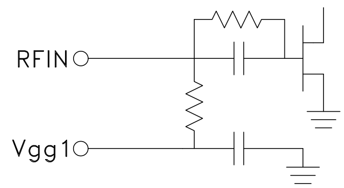
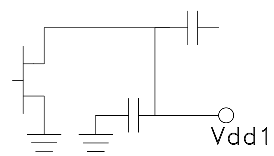
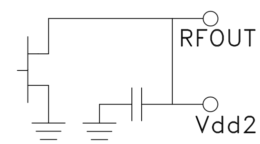
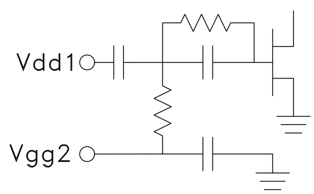
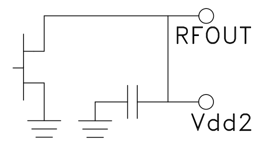
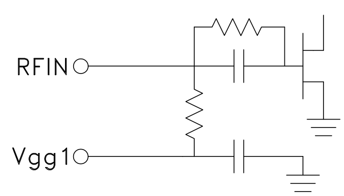
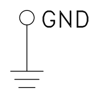
Pad Descriptions

Pad Number	Function	Description	Interface Schematic
1	RFIN	This pad is AC coupled and is matched to 50 Ohms. External blocking capacitor is required.	
2	Vdd1	Drain Bias	
3	RFOUT	This pad is DC coupled and is matched to 50 Ohms. External blocking capacitor is required.	
4	Vgg2	Gate Bias	
5	Vdd2	Drain Bias	
6	Vgg1	Gate Bias	
Die Bottom	GND	Die bottom must be connected to RF/DC ground.	

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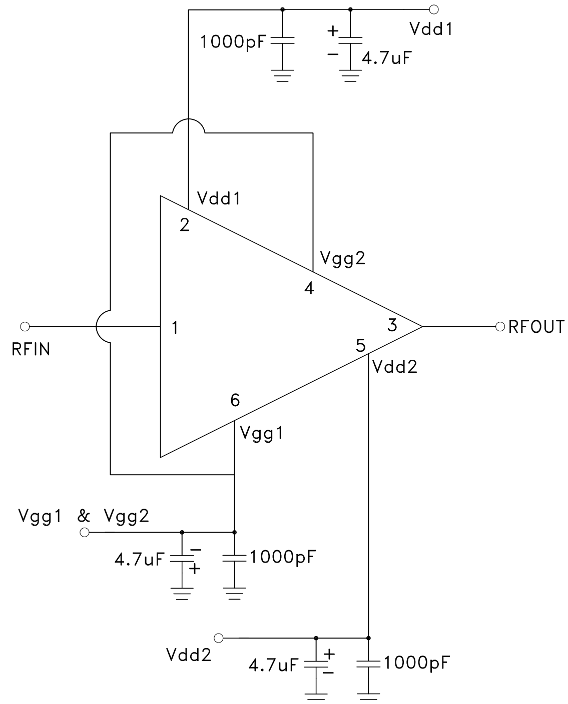
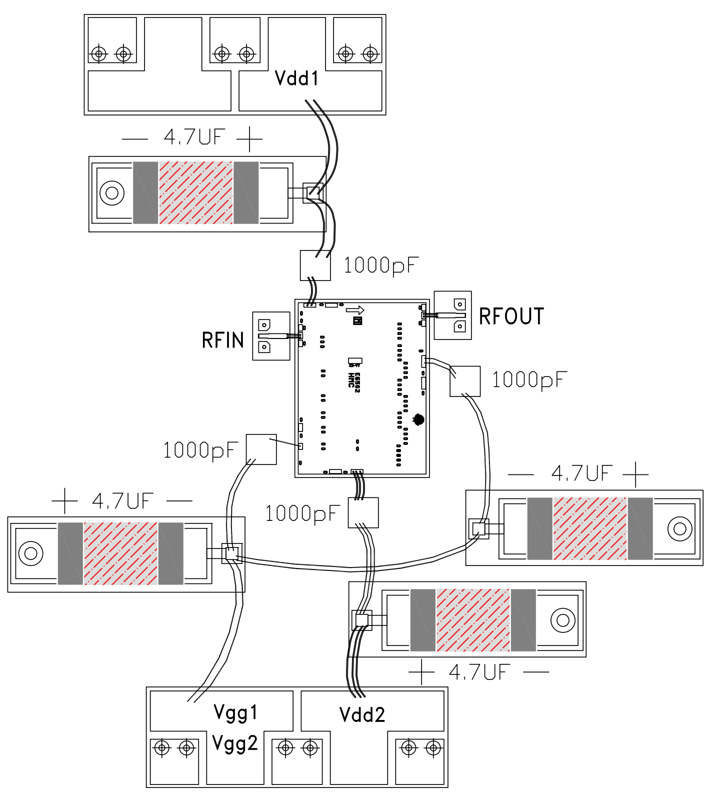
Application Circuit



Assembly Diagram



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Mounting & Bonding Techniques for GaN MMICs

The die should be eutectically attached directly to the ground plane (see HMC general Handling, Mounting, Bonding Note).

50 Ohm Microstrip transmission lines on 0.127mm (5 mil) thick alumina thin film substrates are recommended for bringing RF to and from the chip (Figure 1). If 0.254mm (10 mil) thick alumina thin film substrates must be used, the die should be raised 0.150mm (6 mils) so that the surface of the die is coplanar with the surface of the substrate. One way to accomplish this is to attach the 0.102mm (4 mil) thick die to a copper tungsten or CuMo heat spreader which is then attached to the thermally conductive ground plane (Figure 2).

Microstrip substrates should be placed as close to the die as possible in order to minimize bond wire length. Typical die-to-substrate spacing is 0.076mm to 0.152 mm (3 to 6 mils).

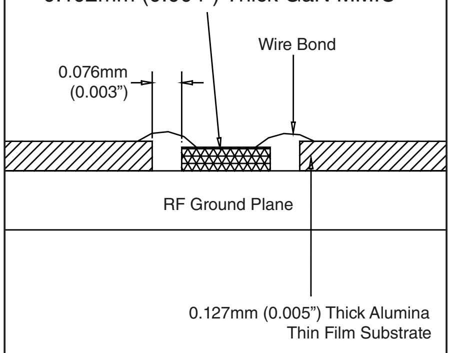

Figure 1.

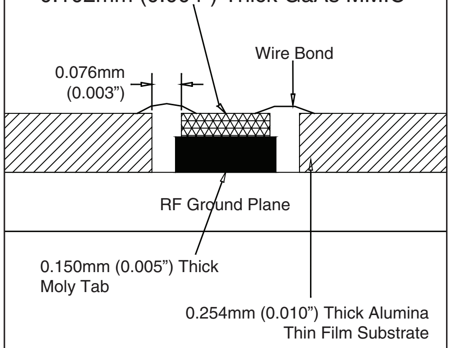

Figure 2.

Handling Precautions

Follow these precautions to avoid permanent damage.

Storage: All bare die are placed in either Waffle or Gel based ESD protective containers, and then sealed in an ESD protective bag for shipment. Once the sealed ESD protective bag has been opened, all die should be stored in a dry nitrogen environment.

Cleanliness: Handle the chips in a clean environment. DO NOT attempt to clean the chip using liquid cleaning systems.

Static Sensitivity: Follow ESD precautions to protect against ESD strikes.

Transients: Suppress instrument and bias supply transients while bias is applied. Use shielded signal and bias cables to minimize inductive pick-up.

Die placement: A heated vacuum collet (180°C) is the preferred method of pick up. Ensure that the area of vacuum contact on the die is minimized to prevent cracking under differential pressure. All air bridges (if applicable) must be avoided during placement. Minimize impact forces applied to the die during auto-placement.

Mounting

The chip is back-metallized with a minimum of 5 microns of gold and is the RF ground and thermal interface. It is recommended that the chip be die mounted with AuSn eutectic preforms. The mounting surface should be clean and flat.

Eutectic Reflow Process: An 80/20 gold tin 0.5mil (13um) thick preform is recommended with a work surface temperature of 280°C. Limit exposure to temperatures above 300°C to 30 seconds maximum. A die bonder or furnace with 95% N_2 / 5% H_2 reducing atmosphere should be used. No organic flux should be used. Coefficient of thermal expansion matching is critical for long term reliability.

Die Attach Inspection: X-ray or acoustic scan is recommended.

Wire Bonding

Thermosonic ball or wedge bonding is the preferred interconnect technique. Gold wire must be used in a diameter appropriate for the pad size and number of bonds applied. Force, time and ultrasonics are critical parameters: optimize for a repeatable, high bond pull strength. Limit the die bond pad surface temperature to 200°C maximum.

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