

## Product Summary

BV <sub>DSS</sub>	BV <sub>DSS</sub> @ T <sub>J</sub> Max	R <sub>DS(ON)</sub> Max	I <sub>D</sub> Max T <sub>A</sub> = +25°C
115V	120V	85mΩ @ V <sub>GS</sub> = 4.5V	3.5A
		90mΩ @ V <sub>GS</sub> = 2.5V	3.4A

## Features and Benefits

- Low Q<sub>g</sub> & Q<sub>gd</sub>
- Small Footprint 1.5mm × 1.5mm
- ESD Protection
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](#) or your local Diodes representative. <https://www.diodes.com/quality/product-definitions/>**

## Description and Applications

This new generation MOSFET is designed to minimize the on-state resistance (R<sub>DS(ON)</sub>), making it ideal for high efficiency power management applications.

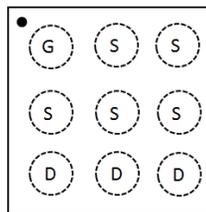
- Battery managements
- Load switches
- Battery protections

## Mechanical Data

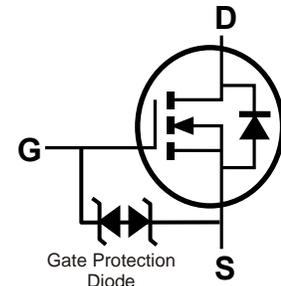
- Package: X4-DSN1515-9
- Terminal Connections: See Diagram Below
- Moisture Sensitivity: Level 1 per J-STD-020
- UBM Size: 250μm
- Terminal Material: Finish – NiAu. Solderable per MIL-STD-202, Method 208 @4
- Weight: 0.0006 grams (Approximate)



X4-DSN1515-9



Top-View  
Pin Configuration



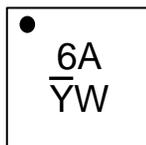
Equivalent Circuit

## Ordering Information (Notes 4 & 5)

Part Number	Package	Packing	
		Qty.	Carrier
DMT12H060LCA9-7	X4-DSN1515-9	3000	Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
  2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  4. Device with exposed silicon sidewall is non-isolated area.
  5. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

## Marking Information



6A = Product Type Marking Code  
 YW = Date Code Marking  
 Y = Year (ex: 2 = 2022)  
 W = Week (ex: a = week 27; z represents week 52 and 53)

### Date Code Key

Year	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032
Code	1	2	3	4	5	6	7	8	9	0	1	2

Week	1-26	27-52	53
Code	A-Z	a-z	z

**Maximum Ratings** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Drain-Source Voltage	V <sub>DSS</sub>	115	V
Gate-Source Voltage	V <sub>GSS</sub>	±5.5	V
Continuous Drain Current (Note 6) V <sub>GS</sub> = 4.5V	I <sub>D</sub>	T <sub>A</sub> = +25°C	3.5
		T <sub>A</sub> = +70°C	2.8
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)	I <sub>DM</sub>	26	A
Maximum Body Diode Continuous Current (Note 6)	I <sub>S</sub>	3.5	A
Pulsed Body Diode Continuous Current (10µs Pulse, Duty Cycle = 1%)	I <sub>SM</sub>	26	A
Avalanche Current, L = 0.3mH (Note 7)	I <sub>AS</sub>	10	A
Avalanche Energy, L = 0.3mH (Note 7)	E <sub>AS</sub>	15	mJ

**ESD Ratings** (Note 11)

Characteristic	Symbol	Value	Unit	JEDEC Class
Electrostatic Discharge - Human Body Model	ESD HBM	2000	V	1C
Electrostatic Discharge - Machine Model	ESD MM	200	V	M2

**Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Power Dissipation (Note 8)	P <sub>D</sub>	1.1	W
Thermal Resistance, Junction to Ambient @T <sub>A</sub> = +25°C (Note 8)	R <sub>θJA</sub>	115	°C/W
Power Dissipation (Note 6)	P <sub>D</sub>	1.9	W
Thermal Resistance, Junction to Ambient @T <sub>A</sub> = +25°C (Note 6)	R <sub>θJA</sub>	65	°C/W
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C

**Electrical Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS (Note 9)</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	115	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 10mA
Zero Gate Voltage Drain Current T <sub>J</sub> = +25°C	I <sub>DSS</sub>	—	—	1	µA	V <sub>DS</sub> = 92V, V <sub>GS</sub> = 0V
Gate-Source Leakage	I <sub>GSS</sub>	—	—	±50	µA	V <sub>GS</sub> = ±8V, V <sub>DS</sub> = 0V
		—	—	±10	µA	V <sub>GS</sub> = ±5.5V, V <sub>DS</sub> = 0V
<b>ON CHARACTERISTICS (Note 9)</b>						
Gate Threshold Voltage	V <sub>GS(TH)</sub>	0.5	—	1.4	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250µA
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	—	56	85	mΩ	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 3A
		—	61	90		V <sub>GS</sub> = 2.5V, I <sub>D</sub> = 2A
		—	75	130		V <sub>GS</sub> = 1.5V, I <sub>D</sub> = 50mA
Diode Forward Voltage	V <sub>SD</sub>	—	0.7	1.0	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = 1A
Reverse Recovery Charge	Q <sub>R</sub>	—	53	—	nC	I <sub>F</sub> = 4.5A, di/dt = 300A/µs
Reverse Recovery Time	t <sub>RR</sub>	—	30	—	ns	
<b>DYNAMIC CHARACTERISTICS (Note 10)</b>						
Input Capacitance	C <sub>iss</sub>	—	560	—	pF	V <sub>DS</sub> = 50V, V <sub>GS</sub> = 0V, f = 1MHz
Output Capacitance	C <sub>oss</sub>	—	80	—		
Reverse Transfer Capacitance	C <sub>r</sub>	—	9.5	—		
Series Gate Resistance	R <sub>g</sub>	—	4.4	—	Ω	V <sub>DS</sub> = 0V, V <sub>GS</sub> = 0V, f = 1MHz
Total Gate Charge	Q <sub>g</sub>	—	8	—	nC	V <sub>DS</sub> = 50V, R <sub>L</sub> = 11Ω V <sub>GS</sub> = 5V, R <sub>GEN</sub> = 3Ω
Gate-Source Charge	Q <sub>gs</sub>	—	1	—		
Gate-Drain Charge	Q <sub>gd</sub>	—	2.4	—		
Gate Charge at V <sub>TH</sub>	Q <sub>g(TH)</sub>	—	0.5	—		
Turn-On Delay Time	t <sub>d(ON)</sub>	—	2	—	ns	V <sub>DS</sub> = 50V, R <sub>L</sub> = 11Ω V <sub>GS</sub> = 5V, R <sub>GEN</sub> = 3Ω
Turn-On Rise Time	t <sub>r</sub>	—	8	—		
Turn-Off Delay Time	t <sub>d(OFF)</sub>	—	29	—		
Turn-Off Fall Time	t <sub>f</sub>	—	11	—		

- Notes:
- Device mounted on FR-4 material with 1inch<sup>2</sup> (6.45cm<sup>2</sup>), 2oz. (0.071mm thick) Cu.
  - Repetitive rating, pulse width limited by junction temperature.
  - Device mounted on FR-4 PCB with minimum recommended pad layout, single sided.
  - Short duration pulse test used to minimize self-heating effect.
  - Guaranteed by design. Not subject to production testing.
  - Refer to ANSI/ESDA/JEDEC specification JS-001-2017 and AEC-Q100-003-Rev-E.

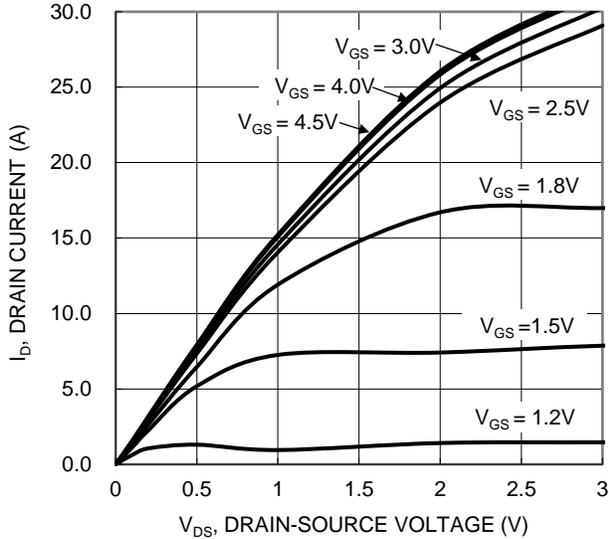


Figure 1. Typical Output Characteristic

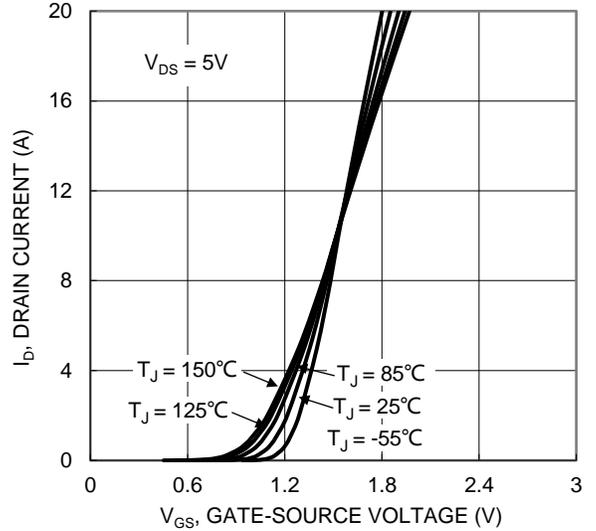


Figure 2. Typical Transfer Characteristic

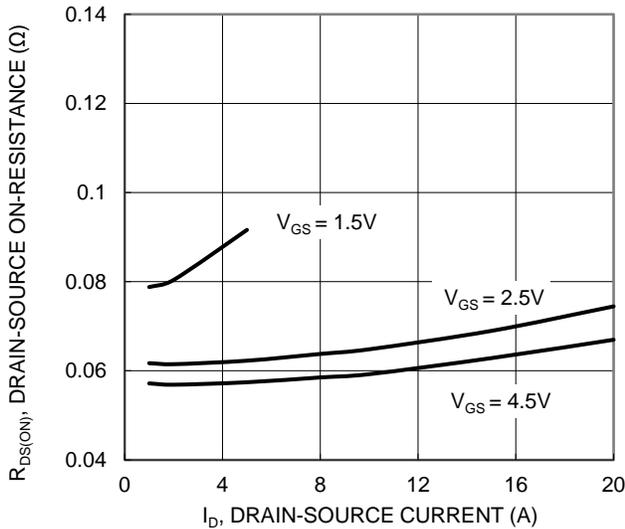


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

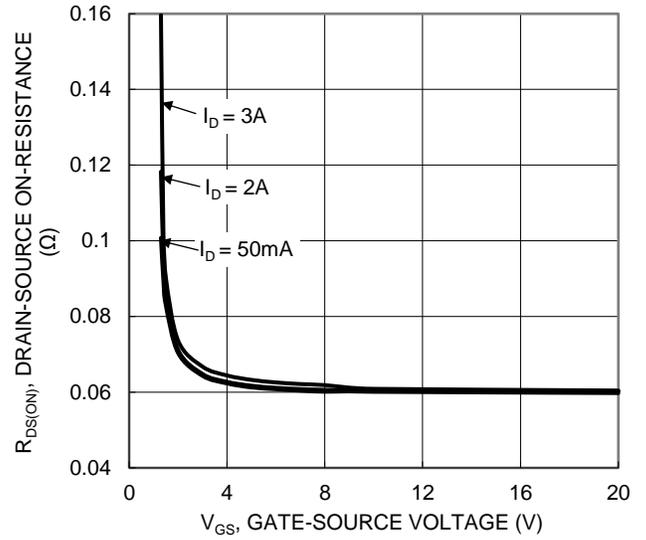


Figure 4. Typical Transfer Characteristic

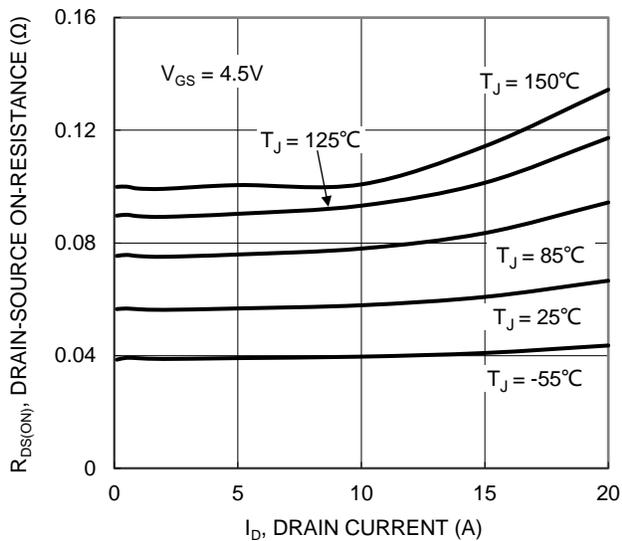


Figure 5. Typical On-Resistance vs. Drain Current and Temperature

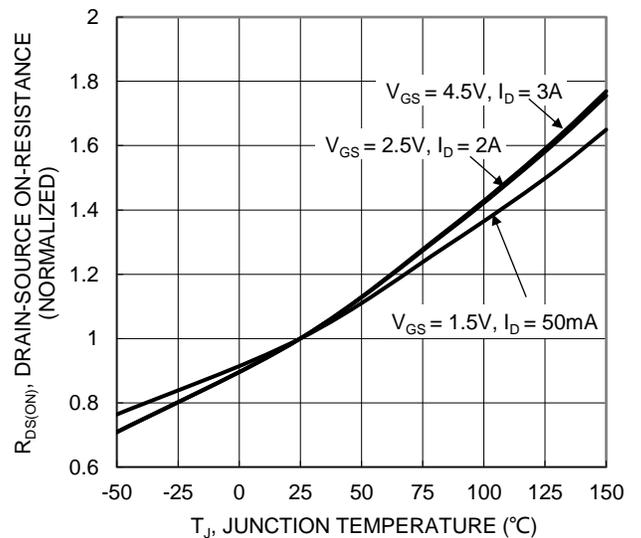


Figure 6. On-Resistance Variation with Temperature

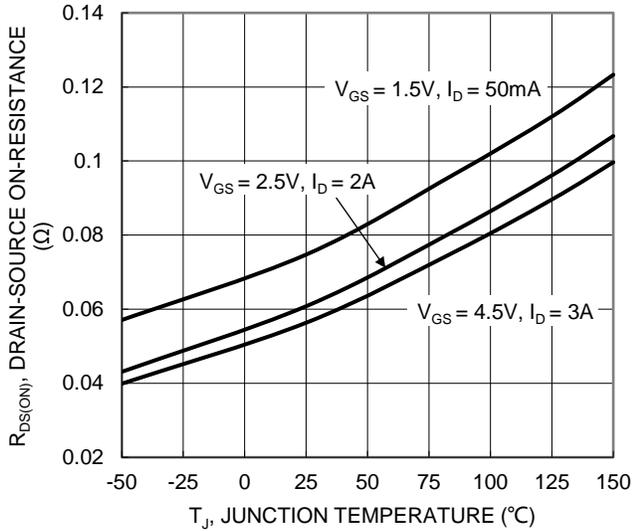


Figure 7. On-Resistance Variation with Temperature

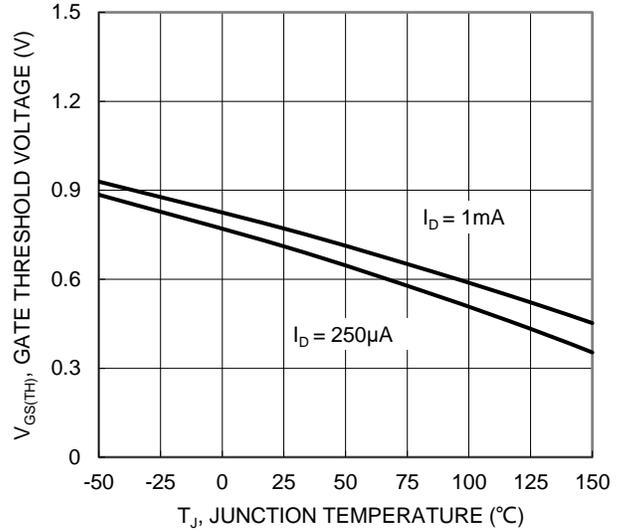


Figure 8. Gate Threshold Variation vs. Junction Temperature

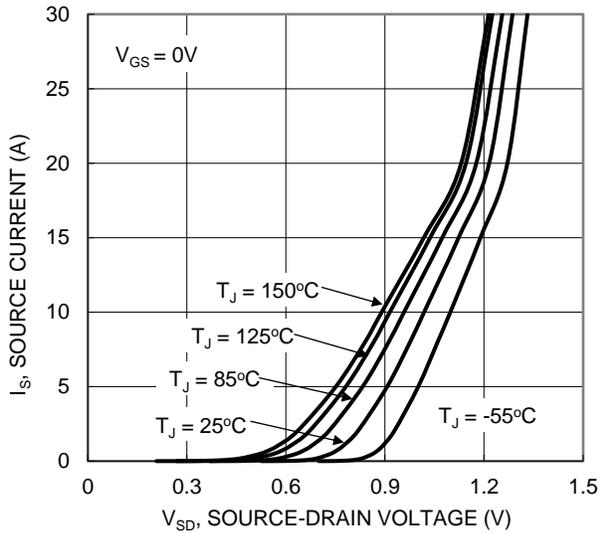


Figure 9. Diode Forward Voltage vs. Current

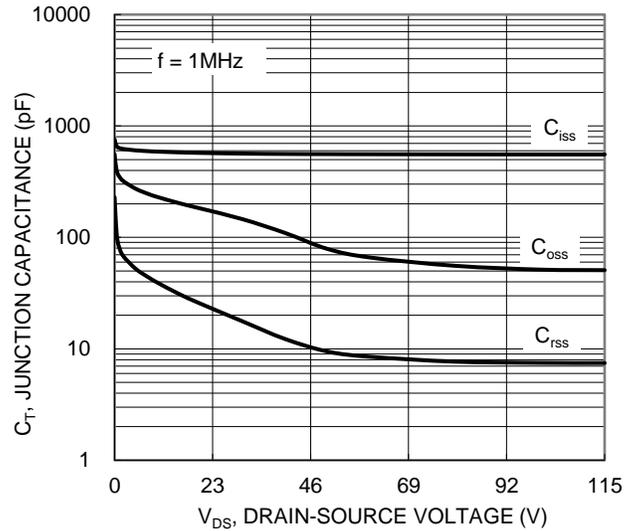


Figure 10. Typical Junction Capacitance

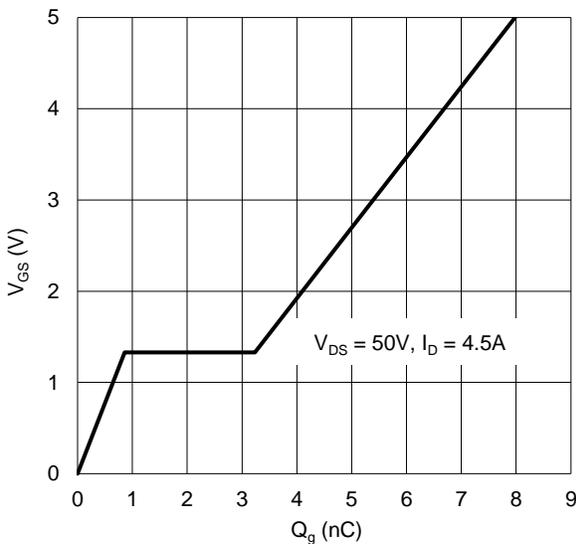


Figure 11. Gate Charge

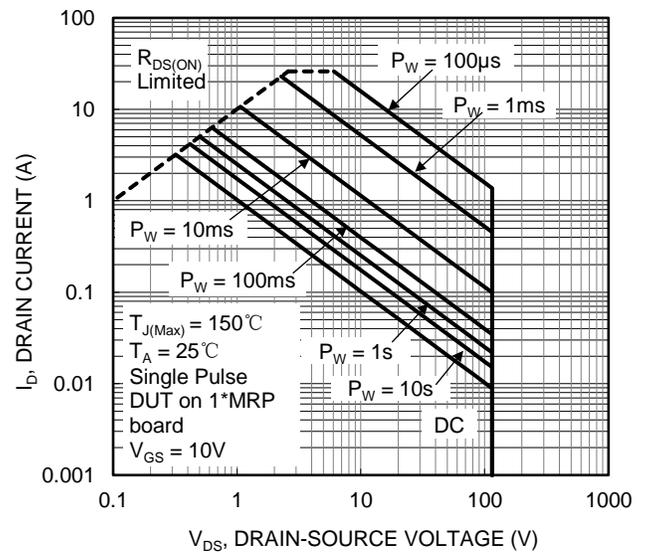


Figure 12. SOA, Safe Operation Area

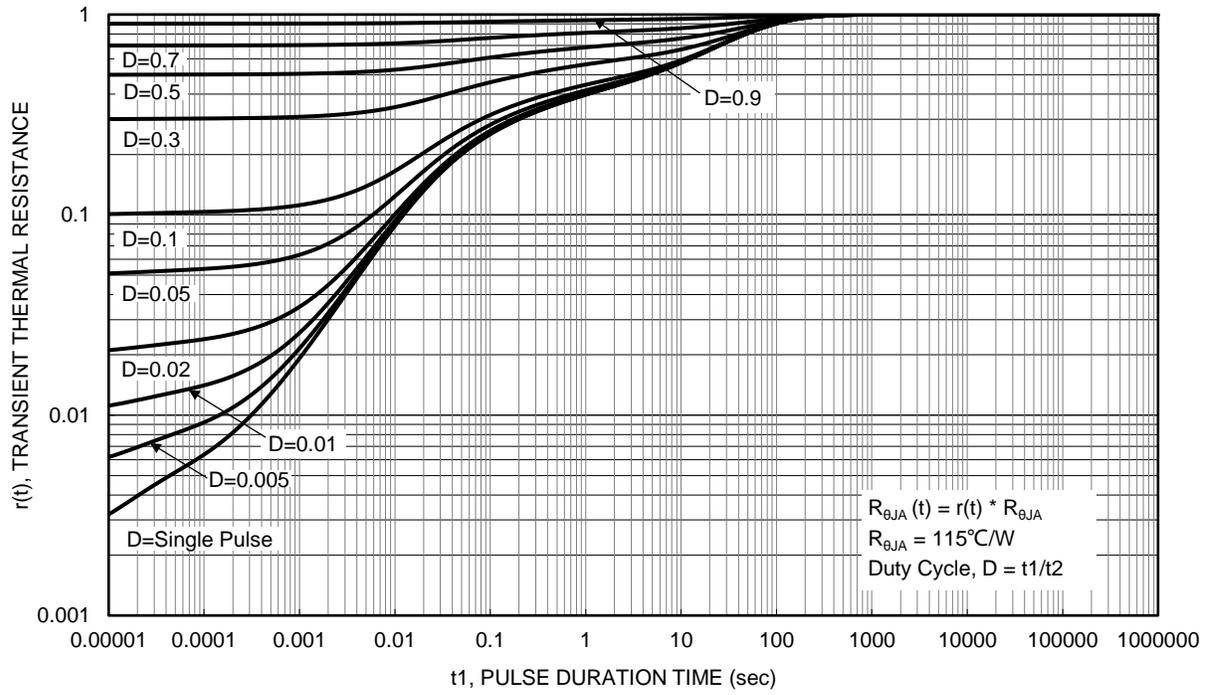
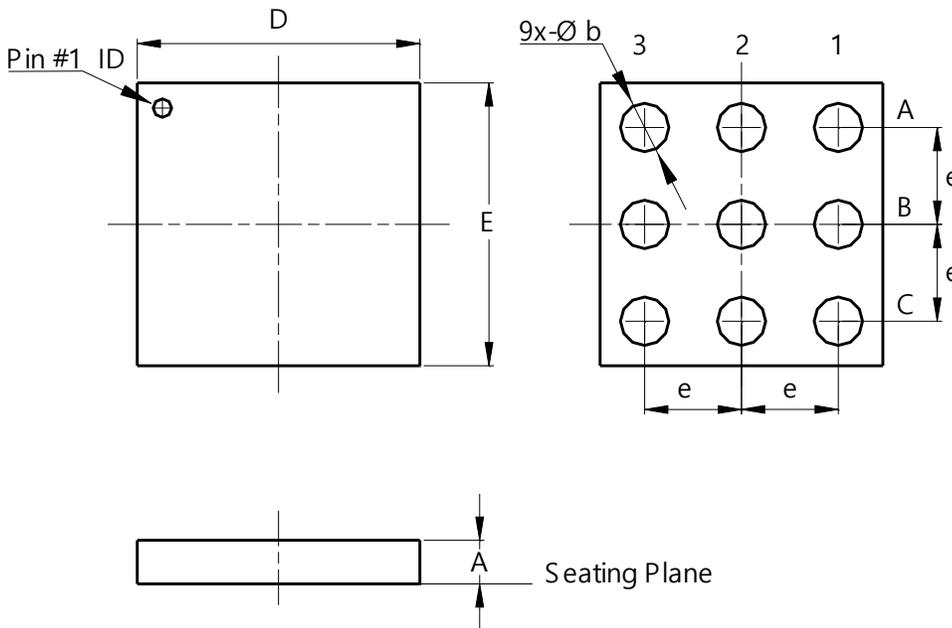


Figure 13. Transient Thermal Resistance

**Package Outline Dimensions**

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**X4-DSN1515-9**

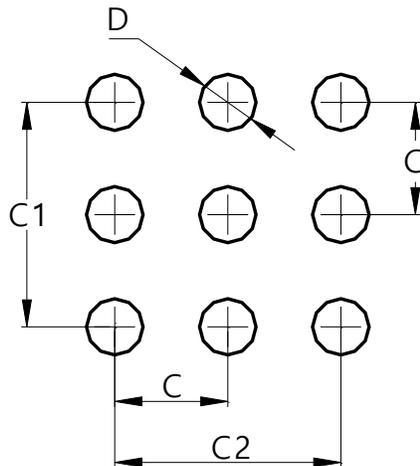


X4-DSN1515-9			
Dim	Min	Max	Typ
A	0.17	0.25	0.225
b	0.21	0.29	0.25
D	1.420	1.50	1.46
E	1.420	1.50	1.46
e	--	--	0.50
All Dimensions in mm			

**Suggested Pad Layout**

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**X4-DSN1515-9**



Dimensions	Value (in mm)
C	0.50
C1	1.00
C2	1.00
D	0.25

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