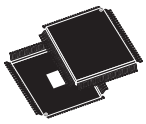
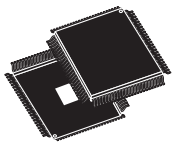
SPC572Lx

32-bit Power Architecture® based MCU for automotive powertrain applications

Datasheet - production data



eTQFP80
10 mm × 10 mm × 1.0 mm
0.4 mm pitch



eTQFP100
14 mm × 14 mm × 1.0 mm
0.5 mm pitch

Features

- AEC-Q100 qualified
- One main 32-bit Power Architecture® VLE Compliant CPU core, single issue
  - Single-precision floating point operations
- 1568 KB on-chip RWW flash memory
  - Supporting EEPROM emulation (32 KB)
- 64 KB general-purpose data SRAM
- System Memory Protection Unit (SMPU)
- Multi-channel direct memory access controllers (eDMA) with 16-channel for up to 60 DMA sources
- Interrupt controller (INTC)
- Four 32-bit and one 64-bit Periodic Interrupt Timer channels (PIT)
- Single phase-locked loops with stable clock domain for peripherals and core (PLL)
- System integration unit lite (SIUL2)
- Boot assist flash (BAF) supports factory programming through UART/LIN, CAN
- Generic timer module (GTM101)
  - Intelligent complex timer module
  - 72 channels (16 input and 56 output)
- Enhanced analog-to-digital converter system with:
  - Three 12-bit SAR analog converters
  - One 16-bit Sigma-Delta analog converters
- Decimation unit to support SD ADC data conditioning
- Two deserial serial peripheral interface (DSPI) modules
- Two LIN and UART communication interfaces (LINFlexD) modules
- One µs-bus channel (composed by one DSPI and one LINFlexD)
- Four SENT channels
- Two modular controller area network (M_CAN) modules
- Fast Ethernet controller (FEC)
- Fast Asynchronous Serial Transmission (LFAST)
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 standard, with some support for 2010 standard
- Device and board test support per Joint Test Action Group (JTAG) (IEEE 1149.1 and IEEE 1149.7)
- Single 5 V +/-10% Power supply supporting cold start conditions (down to 3.0 V)
- Self Test capability
- Designed for eTQFP80 and eTQFP100

Table 1. Device summary

Memory Flash size	Root Part Numbers	
	Package eTQFP80	Package eTQFP100
1056 KByte	SPC572L60F2	SPC572L60E3
1568 KByte	SPC572L64F2	SPC572L64E3

This is information on a product in full production. www.st.com

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1 Introduction

1.1 Document overview

This document provides electrical specifications, pin assignments, and package diagrams for the SPC572Lx series of microcontroller units (MCUs). For functional characteristics, see the device reference manual.

1.2 Description

This family of MCUs is targeted at automotive powertrain controller applications for four-cylinder gasoline and diesel engines, chassis control applications, transmission control applications, steering and braking applications, as well as low-end hybrid applications.

The family is designed to achieve ISO26262 ASIL-A compliance.

1.3 Device feature summary

Table 2. SPC572Lx device feature summary

Feature		Description
Process		55 nm
Main processor	Core	e200z2
	Number of main cores	1
	Single precision floating point	Yes
	VLE	Yes
Main processor frequency		80 MHz
SMPU		Yes
Software watchdog timer (task SWT/safety SWT)		2 (1/1)
Core Nexus class		3
Sequence processing unit (SPU)		Yes
System SRAM		64 KB
Flash memory		1536 KB
Flash memory fetch accelerator		8 × 128 bit
Data flash memory (EEPROM)		2 × 16 KB
Flash memory overlay RAM		8 KB
DMA channels		16
LINFlexD (UART/MSC)		3 (2/1)
M_CAN/M_TTCAN		2/0
DSPI (SPI/MSC/sync SCI)		2 (1/1/0)
Microsecond bus downlink		Yes

Table 2. SPC572Lx device feature summary (continued)

Feature	Description
SENT bus	4 channels
Ethernet	Yes
Zipwire (SIPI / LFAST) Interprocessor bus	High speed (4-phase only)
System timers	4 PIT channels 1 AUTOSAR® (STM) 64-bit PIT
GTM timer	16 input channels, 56 output channels
GTM RAM	18.53 KB
Interrupt controller	1024 sources
ADC (SAR)	3
ADC (SD)	1
Temperature sensor	Yes
PLL	Single PLL with no FM
Internal linear voltage regulator	1.2 V
External power supplies	5 V(1) 3.3 V(2)
Low-power modes	Stop mode Slow mode
Packages	eTQFP80 eTQFP100

1. The device can be powered up at 5 V only.
2. Optional: can be used for special I/O segments

1.4 Block diagram

Figure 1 and *Figure 2* show the top-level block diagrams.

Figure 1. Block diagram

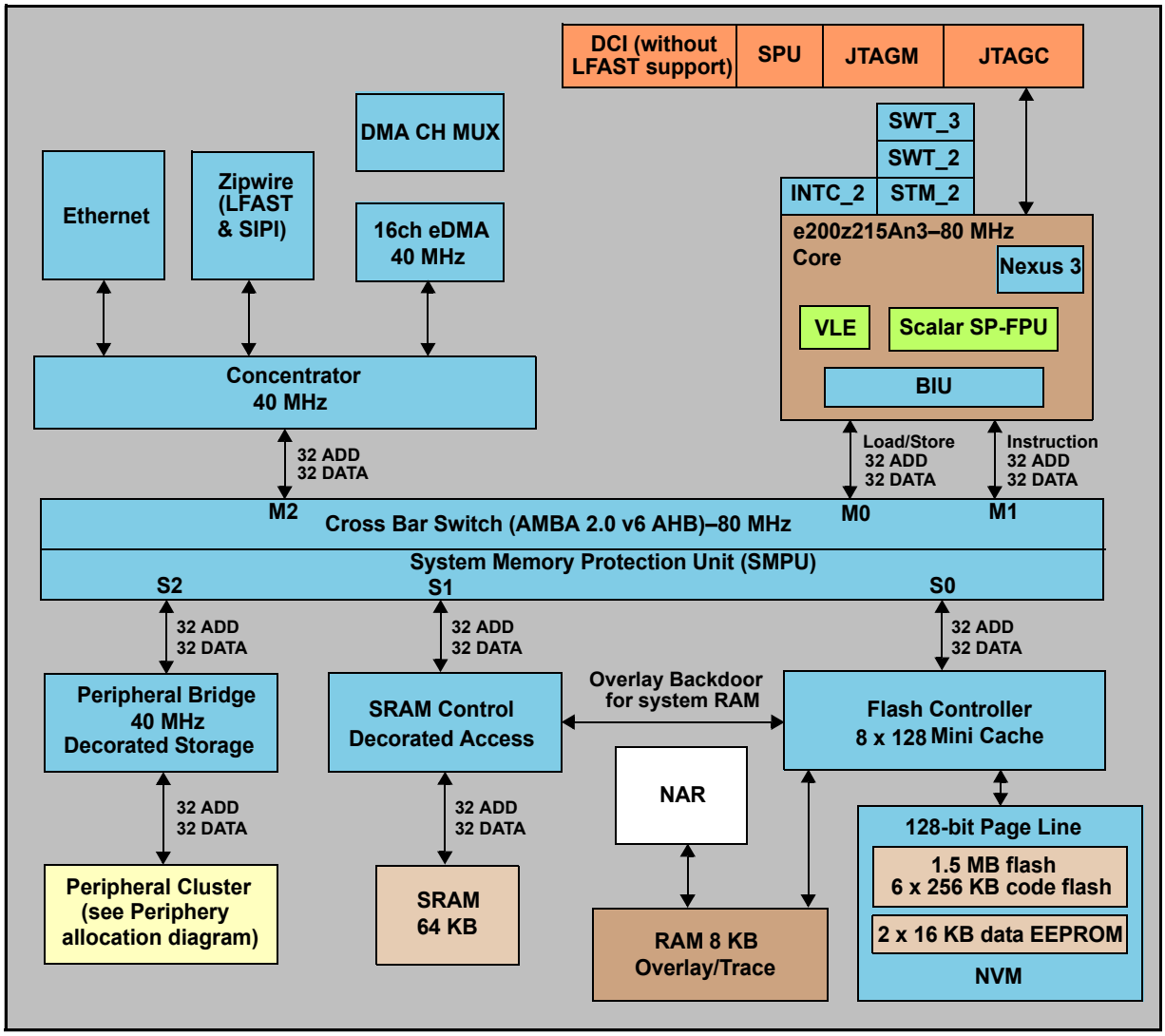
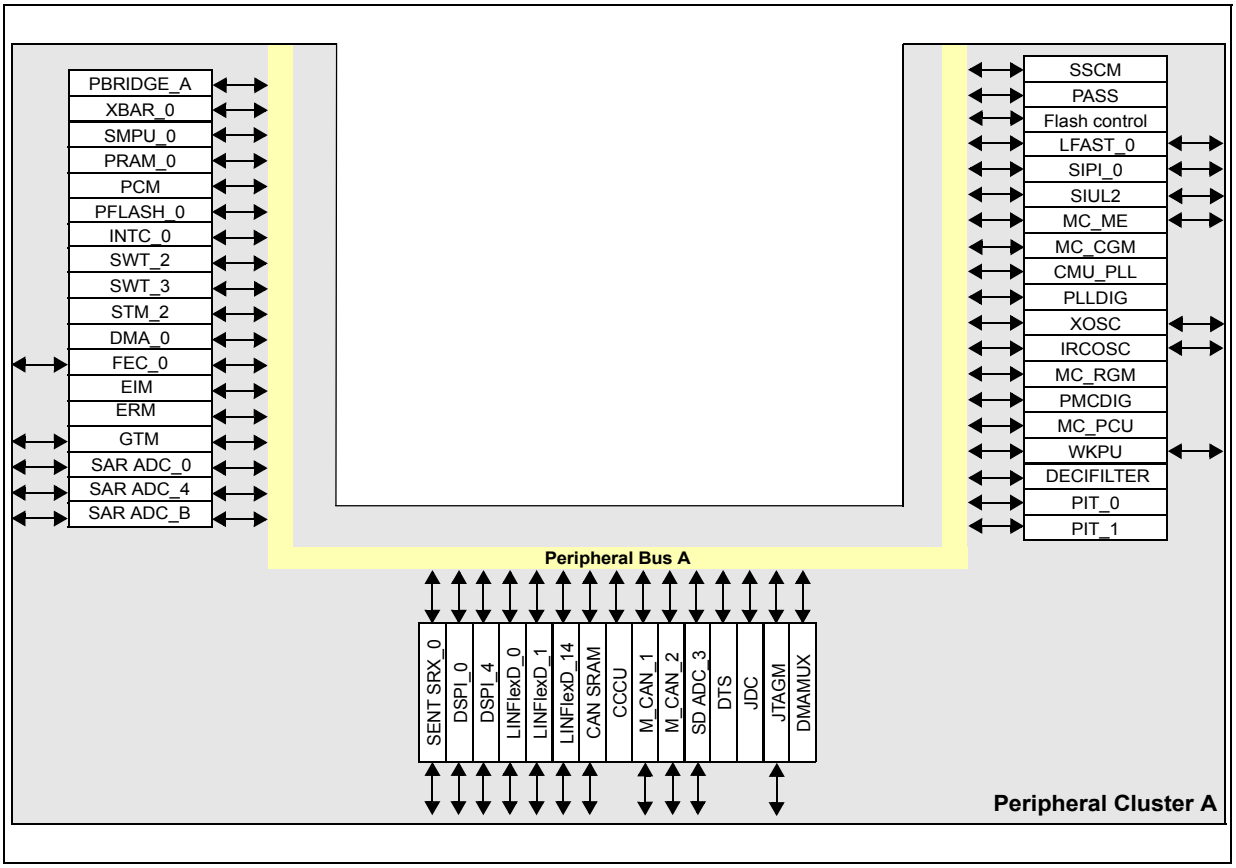


Figure 2. Periphery allocation



1.5 Features overview

On-chip modules within SPC572Lx include the following features:

- 1 main CPU, single issue, 32-bit CPU core complex (e200z2)
  - Power Architecture embedded specification compliance
  - Instruction set enhancement allowing variable length encoding (VLE), encoding a mix of 16-bit and 32-bit instructions, for code size footprint reduction
  - Single-precision floating point operations
  - Saturation Instructions Extension adding scalar saturating arithmetic support to the *PowerISA* Integer Saturation (ISAT)
- 1568 KB (1536 KB code flash + 32 KB data flash) on-chip flash memory
  - Supporting multiple blocks allowing EEPROM emulation
  - RWW between data EEPROM and code flash memory
- 64 KB general-purpose data SRAM
- System Memory Protection Unit (SMPU)
- 16-channel Direct Memory Access controllers (eDMA) with two channel multiplexers for up to 60 DMA sources
- Interrupt Controller (INTC) supporting up to 1024 interrupt sources (all are not assigned)
- System Timer Module (STM)
- 2 Software Watchdog Timers (SWT)
- 2 Periodic Interrupt Timers (PIT)
  - 1 PIT with four standard 32-bit timer channels
  - 1 PIT with two 32-bit timer channels which can be combined into one 64-bit channel
- Single phase-locked loop with stable clock domain for peripherals and core (PLL)
- Single crossbar switch architecture for concurrent access to peripherals, flash memory, or SRAM from multiple bus masters
- System Integration Unit Lite (SIUL2)
- Boot Assist Flash (BAF) supports factory programming using a serial bootload through the UART Serial Boot Mode Protocol (physical interface (PHY) can be e.g., UART and CAN)
- PASS module (supporting 256-bit JTAG password protection)
- Device life cycle monitoring
- Generic Timer Module (GTM101)
- Enhanced analog-to-digital converter system with:
  - Three 12-bit SAR analog converters
  - One 16-bit Sigma-Delta analog converter
- Decimation unit to support SD ADC data conditioning
- 1 Deserial Serial Peripheral Interface (DSPI) module
- 2 LIN and UART communication interfaces (LINFlexD) modules
- 1 microsecond-bus channel (composed of one DSPI and one LINFlexD)
- 4 SENT (Single Edge Nibble Transmission) channels
- 2 Modular Controller Area Network (M_CAN) modules

- 1 Clock Calibration on CAN Unit (CCCU)
- Fast Ethernet Controller (FEC)
- Fast Asynchronous Serial Transmission (LFAST)
- Nexus Development Interface (NDI) per IEEE-ISTO 5001-2003 standard, with partial support for 2010 standard
- Device and board test support per Joint Test Action Group (JTAG) (IEEE 1149.1 and IEEE 1149.7)
- On-chip voltage regulator controller manages the supply voltage down to 1.2 V for core logic
- Self-test capability

2 Package pinouts and signal descriptions

2.1 Package pinouts

The QFP package pinouts are shown in *Figure 3* and *Figure 4*.

Figure 3. 80-pin QFP configuration (top view)

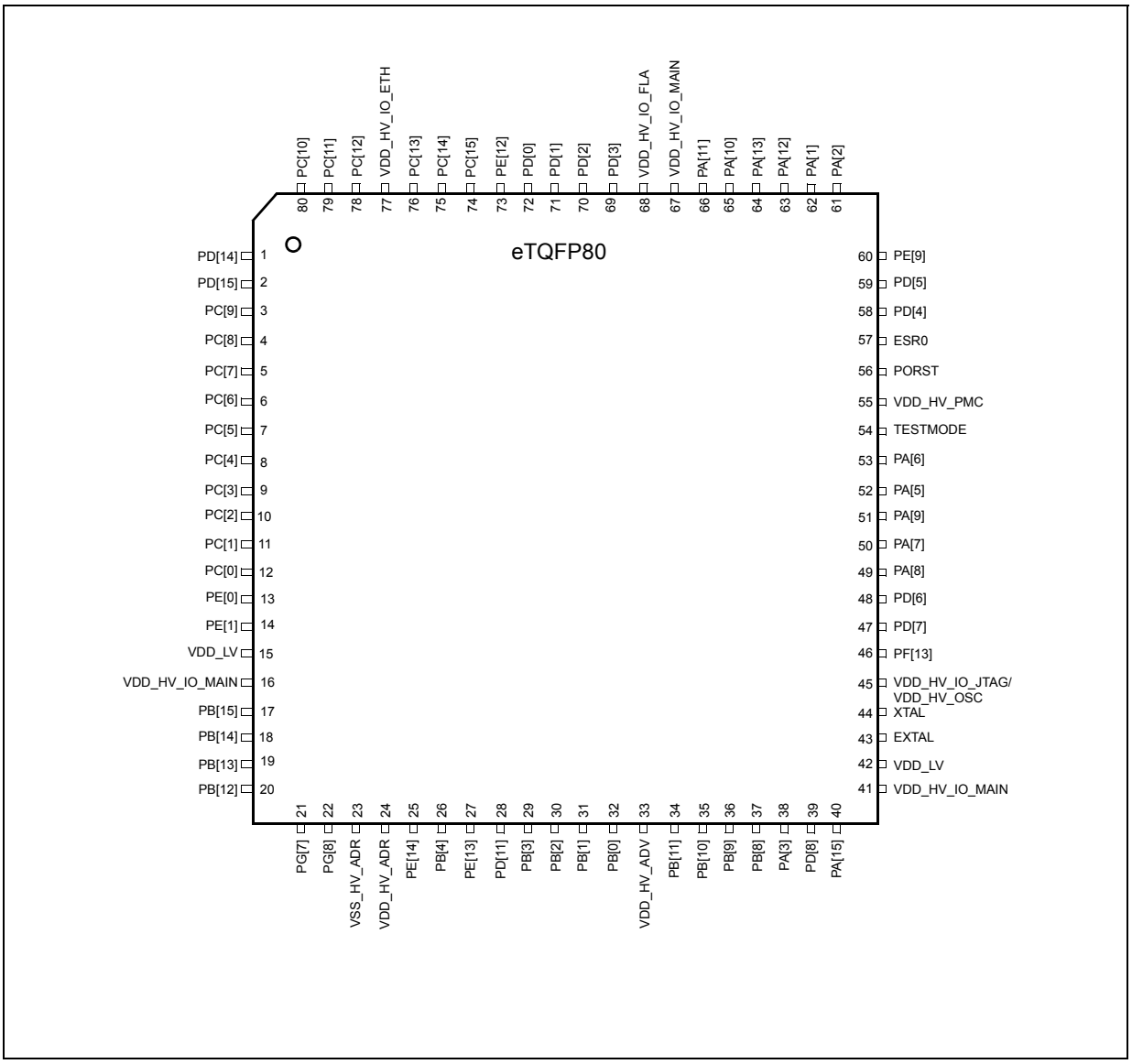
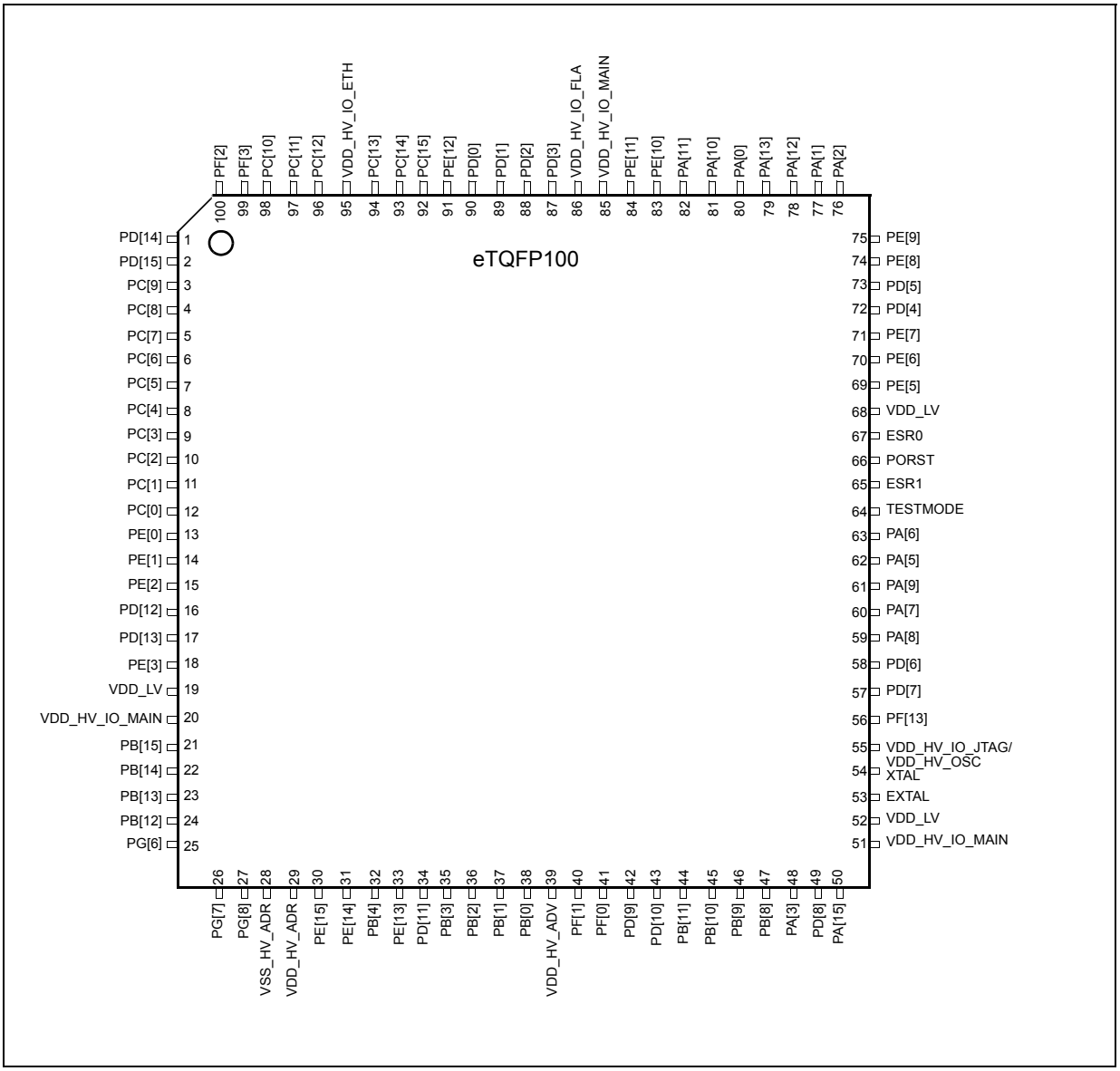


Figure 4. 100-pin QFP configuration (top view)



2.2 Pin descriptions

The following sections provide signal descriptions and related information about device functionality and configuration.

2.2.1 Power supply and reference voltage pins

Table 3 contains information on power supply and reference pin functions for the devices. See the Signal Table (Excel file) attached to this document. Locate the paperclip symbol on the left side of the PDF window, and click it. Double-click on the excel file to open it and select the Supply Pins Table tab.

Table 3. Power supply and reference pins

Supply			QFP pin	
Symbol	**Type**	**Description**	**80**	**100**
V_{SS_HV}	Ground	High voltage ground	Exposed pad 81	Exposed pad 101
V_{SS_LV}	Ground	Low voltage ground	Exposed pad 81	Exposed pad 101
$V_{SS\_HV\_OSC}$	Ground	Ground supply for the oscillator	Exposed pad 81	Exposed pad 101
V_{DD_LV}	Power	Low voltage power supply for production device (PLL is also powered by this pin.)	15, 42, 68	19, 52, 68
$V_{DD\_HV\_PMC}$	Power	High voltage power supply for internal power management unit	55	—
$V_{DD\_HV\_IO\_MAIN}$	Power	High voltage power supply for I/O	16, 41, 67	20, 51, 85
$V_{DD\_HV\_IO\_JTAG}$	Power	JTAG/Oscillator power supply	45	55
$V_{DD\_HV\_OSC}$	Power	Oscillator voltage supply	45	55
$V_{DD\_HV\_IO\_ETH}$	Power	Ethernet 3.3 V I/O supply	77	95
$V_{DD\_HV\_FLA}$	Power	Decoupling supply pin for flash	68	86
$V_{DD\_HV\_ADV}$	Power	High voltage supply for ADC	33	39
$V_{SS\_HV\_ADR}$	Reference	Ground reference of ADCs	23	28
$V_{DD\_HV\_ADR}$	Reference	Voltage reference of ADCs	24	29

2.2.2 System pins

Table 4 contains information on system pin functions for the devices.

Table 4. System pins

Symbol	Description	Direction	QFP pin	
			80	**100**
PORST	Power on reset with Schmitt trigger characteristics and noise filter. PORST is active low	Bidirectional	56	66
ESR0	External functional reset with Schmitt trigger characteristics and noise filter. ESR0 is active low	Bidirectional	57	67
TESTMODE	Pin for testing purpose only. An internal pull-down is implemented on the TESTMODE pin to prevent the device from entering TESTMODE. It is recommended to connect the TESTMODE pin to $V_{SS\_HV\_IO}$ on the board. The value of the TESTMODE pin is latched at the negation of reset and has no affect afterward. The device will not exit reset with the TESTMODE pin asserted during power-up.	Input only	54	64

Table 4. System pins (continued)

Symbol	Description	Direction	QFP pin	
			80	100
XTAL	Analog output of the oscillator amplifier circuit needs to be grounded if oscillator is used in bypass mode.	Output	44	54
EXTAL	Analog input of the oscillator amplifier circuit when oscillator is not in bypass mode Analog input for the clock generator when oscillator is in bypass mode	Input	43	53

2.2.3 LVDS pins

Table 5 contains information on LVDS pin functions for the devices.

Table 5. LVDSM pin descriptions

Functional block	Port pin	Signal	Signal description	Direction	Package pin number	
					eTQFP80	eTQFP100
SIPI LFAST(1)	PF[13]	SIPI_RXN	Interprocessor Bus LFAST, LVDS Receive Negative Terminal	I	46	56
	PD[7]	SIPI_RXP	Interprocessor Bus LFAST, LVDS Receive Positive Terminal	I	47	57
	PD[6]	SIPI_TXN	Interprocessor Bus LFAST, LVDS Transmit Negative Terminal	O	48	58
	PA[8]	SIPI_TXP	Interprocessor Bus LFAST, LVDS Transmit Positive Terminal	O	49	59
DSPI 4 Microsecond Bus	PD[3]	SCK_N	DSPI 4 Microsecond Bus Serial Clock, LVDS Negative Terminal	O	69	87
	PD[2]	SCK_P	DSPI 4 Microsecond Bus Serial Clock, LVDS Positive Terminal	O	70	88
	PD[1]	SOUT_N	DSPI 4 Microsecond Bus Serial Data, LVDS Negative Terminal	O	71	89
	PD[0]	SOUT_P	DSPI 4 Microsecond Bus Serial Data, LVDS Positive Terminal	O	72	90

1. DRCLK and TCK/DRCLK usage for SIPI LFAST is described in the SPC572Lx reference manual, refer to SIPI LFAST chapter.

2.2.4 Generic pins

The I/O Signal Description Table contains information on generic pins. See the I/O Signal Description and Input Multiplexing Tables (Excel file) attached to this document. Locate the

paperclip symbol on the left side of the PDF window, and click it. Double-click on the excel file to open it and select the I/O Signal Description Table tab.

3 Electrical characteristics

3.1 Introduction

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” (Controller Characteristics) is included in the “Symbol” column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” (System Requirement) is included in the “Symbol” column.

Note: Within this document, $V_{DD\_HV\_IO}$ refers to supply pins $V_{DD\_HV\_IO\_MAIN}$, $V_{DD\_HV\_IO\_JTAG}$, $V_{DD\_HV\_IO\_ETH}$, $V_{DD\_HV\_PMC}$ and $V_{DD\_HV\_FLA}$.

3.2 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in *Table 6* are used and the parameters are tagged accordingly in the tables where appropriate.

Table 6. Parameter classifications

Classification tag	Tag description
P	Parameters are guaranteed by production testing on each individual device.
C	Parameters are guaranteed by the design characterization by measuring a statistically relevant sample size across process variations.
T	Parameters are guaranteed by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Parameters are derived mainly from simulations.

Note: The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.3 Absolute maximum ratings

Table 7 describes the maximum ratings of the device.

Table 7. Absolute maximum ratings(1)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
Cycle	SR	Lifetime power cycles	—	—	1000	k
V_{SS_HV}	SR	Ground voltage	—	—	—	—
V_{DD_LV}	SR	1.2 V core supply voltage(2),(3),(4)	—	–0.3	1.5	V
$V_{DD\_HV\_IO}$(5)	SR	I/O supply voltage(6)	—	–0.3	6.0	V
$V_{DD\_HV\_ADV}$(7)	SR	SAR and S/D ADC supply voltage	Reference to $V_{SS\_HV\_ADV}$	–0.3	6.0	V
$V_{SS\_HV\_ADR}$	SR	SAR and S/D ADC low reference	Reference to V_{SS_HV}	–0.3	0.3	V
$V_{DD\_HV\_ADR}$	SR	SAR and S/D ADC high reference	Reference to corresponding $V_{SS\_HV\_ADR}$	–0.3	6.0	V
V_{IN}	SR	I/O input voltage range(8)	—	–0.3	6.0	V
			Relative to $V_{SS\_HV\_IO}$	–0.3	—	
			Relative to $V_{DD\_HV\_IO}$	—	0.3	
I_{INJD}	SR	Maximum DC injection current for digital pad	Per pin, applies to all digital pins	–5	5	mA
I_{INJA}	SR	Maximum DC injection current for analog pad	Per pin, applies to all analog pins	–5	5	mA
I_{MAXD}	SR	Maximum output DC current when driven	Medium	–7	8	mA
			Strong	–10	10	
			Very strong	–11	11	
I_{MAXSEG}	SR	Maximum current per power segment(9)	—	–90	90	mA
T_{STG}	SR	Storage temperature range and non-operating times	—	–55	175	°C
STORAGE	SR	Maximum storage time, assembled part programmed in ECU	No supply; storage temperature in range –40 °C to 60 °C	—	20	years
T_{SDR}	SR	Maximum solder temperature(10) Pb-free package	—	—	260	°C
MSL	SR	Moisture sensitivity level(11)	—	—	3	—
t_{XRAY}	T	X-ray screen time	At 80÷130 KV; 20÷50 µA; max 1 Gy dose	—	200	ms

1. Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.
2. Allowed 1.45 – 1.5 V for 60 seconds cumulative time at maximum T_J = 150 °C, remaining time as defined in note 5.
3. Allowed 1.375 – 1.45 V for 10 hours cumulative time at maximum T_J = 125 °C, remaining time as defined in note *5*.

4. 1.32 – 1.375 V range allowed periodically for supply with sinusoidal shape and average supply value below 1.288 V at maximum T_J = 125 °C
5. $V_{DD\_HV\_IO}$ refers to supply pins $V_{DD\_HV\_IO\_MAIN}$, $V_{DD\_HV\_IO\_JTAG}$, $V_{DD\_HV\_IO\_ETH}$, $V_{DD\_HV\_OSC}$, $V_{DD\_HV\_FLA}$.
6. Allowed 5.5–6.0 V for 60 seconds cumulative time with no restrictions, for 10 hours cumulative time device in reset, T_J = 150 °C remaining time at or below 5.5 V.
7. $V_{DD\_HV\_ADV}$ is also the supply for the device temperature sensor and bandgap reference.
8. The maximum input voltage on an I/O pin tracks with the associated I/O supply maximum. For the injection current condition on a pin, the voltage equals the supply plus the voltage drop across the internal ESD diode from I/O pin to supply. The diode voltage varies significantly across process and temperature, but a value of 0.3 V can be used for nominal calculations.
9. Sum of all controller pins (including both digital and analog) must not exceed 150 mA. A $V_{DD\_HV\_IO}$ power segment is defined as one or more GPIO pins located between two $V_{DD\_HV\_IO}$ supply pins.
10. Solder profile per IPC/JEDEC J-STD-020D.
11. Moisture sensitivity per JEDEC test method A112.

3.4 Electromagnetic Compatibility (EMC)

EMC measurements to IC-level IEC standards are available from STMicroelectronics on request.

3.5 Electrostatic discharge (ESD)

The following table describes the ESD ratings of the device.

Table 8. ESD ratings(1),(2)

Parameter	C	Conditions	Value	Unit
ESD for Human Body Model (HBM)(3)	T	All pins	2000	V
ESD for field induced Charged Device Model (CDM)(4)	T	All pins	500	V

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. Device failure is defined as: “If after exposure to ESD pulses, the device does not meet the device specification requirements, which includes the complete DC parametric and functional testing at room temperature and hot temperature. Maximum DC parametrics variation within 10% of maximum specification”.
3. This parameter tested in conformity with ANSI/ESD STM5.1-2007 Electrostatic Discharge Sensitivity Testing.
4. This parameter tested in conformity with ANSI/ESD STM5.3-1990 Charged Device Model - Component Level.

3.6 Operating conditions

The following table describes the operating conditions for the device for which all specifications in the datasheet are valid, except where explicitly noted.

The device operating conditions must not be exceeded or the functionality of the device is not guaranteed.

Table 9. Device operating conditions(1)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
Frequency								
f_{SYS}	CC	C	Device operating frequency(2)	T_J –40 °C to 150 °C	—	—	80	MHz
Temperature								
T_J	SR	P	Operating temperature range - junction	—	–40.0	—	150.0	°C
T_A (T_L to T_H)	SR	P	Ambient operating temperature range	—	–40.0	—	125.0	°C
Voltage								
V_{DD_LV}	CC	P	Core supply voltage measured at external pin(3)(4)	Refer to *Section 3.15: Power management: PMC, POR/LVD, sequencing*				V
$V_{DD\_HV\_IO\_MAIN}$(5)	SR	P	I/O supply voltage	LVD400 enabled(6)	4.5	—	5.5	V
		C		LVD400 disabled (6),(7),(8),(9)	4.0	—	5.9	
		C			3.0	—	5.9	
$V_{DD\_HV\_IO\_JTAG}$	SR	P	JTAG I/O supply voltage(10)	5 V range	4.5	—	5.5	V
		C		3.3 V range	3.0	—	3.6	
		C		5 V range	4.0	—	5.9	
$V_{DD\_HV\_IO\_ETH}$	SR	P	Ethernet I/O supply voltage	5 V range	4.5	—	5.5	V
		C		3.3 V range	3.0	—	3.6	
$V_{DD\_HV\_FLA}$(11),(12)	CC	P	Flash core voltage	—	3.0	—	5.5	V
$V_{DD\_HV\_ADV}$	SR	P	SARADC and SDADC supply voltage	LVD295/ enabled	4.5	—	5.5	V
		C		LVD400 disabled(10),(7),(8)	4.0	—	5.9	
		C		LVD295/ disabled(7),(8)	3.7	—	5.9	
$V_{DD\_HV\_ADR}$	SR	P	SAR and S/D ADC reference	—	4.5	—	5.5	V
		C			4.0	—	5.9	
		C			2.0	—	4.0	
$V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV}$	SR	D	SAR and S/D ADC reference voltage	—	—	—	25	mV
$V_{SS\_HV\_ADR}$	SR	P	SD ADC ground reference voltage	—	$V_{SS\_HV\_ADV}$			V
V_{RAMP_HV}	SR	D	Slew rate on HV power supply pins	—	—	—	100	V/ms

Table 9. Device operating conditions[1] (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{IN}	SR	C	I/O input voltage range	—	0	—	5.5	V
Injection current								
I_{IC}	SR	T	DC injection current (per pin)[13],[14],[15]	Digital pins and analog pins	–3.0	—	3.0	mA
I_{MAXSEG}	SR	D	Maximum current per power segment[16]	—	–80	—	80	mA

1. The ranges in this table are design targets and actual data may vary in the given range.
2. Maximum operating frequency is applicable to the core and platform for the device. See the Clocking chapter in the *SPC572Lx Microcontroller Reference Manual* for more information on the clock limitations for the various IP blocks on the device.
3. Core voltage as measured on device pin to guarantee published silicon performance.
4. During power ramp, voltage measured on silicon might be lower. Maximum performance is not guaranteed, but correct silicon operation is guaranteed. Refer to the Power Management and Reset Generation Module chapters in the *SPC572Lx Microcontroller Reference Manual* for further information.
5. The $V_{DD\_HV\_PMC}$ supply providing power to the internal regulator is shorted with the $V_{DD\_HV\_IO}$ supply within package.
6. LVD400 can be disabled by SW (always enabled after power-up).
7. Maximum voltage is not permitted for entire product life. See *Absolute maximum rating*.
8. When internal LVD/HVDs are disabled, external monitoring is required to guarantee correct device operation.
9. Reduced output/input capabilities below 4.2 V. See performance operating values in I/O pad electrical characteristics. Not all functionality are guaranteed below 4.2 V. Please check specific supply constraints by module in *Table 9 (Device operating conditions)*.
10. $V_{DD\_HV\_IO\_JTAG}$ supply is shorted with $V_{DD\_HV\_OSC}$ supply within package.
11. Flash read, program, and erase operations are supported for a minimum $V_{DD\_HV\_FLA}$ value of 3.0 V.
12. This voltage can be measured on the pin but is not supplied by an external regulator. The Power Management Controller generates PORs based on this voltage.
13. Full device lifetime without performance degradation
14. I/O and analog input specifications are only valid if the injection current on adjacent pins is within these limits. See the *Absolute maximum ratings* table for maximum input current for reliability requirements.
15. The I/O pins on the device are clamped to the I/O supply rails for ESD protection. When the voltage of the input pin is above the supply rail, current is injected through the clamp diode to the supply rail. For external RC network calculation, assume typical 0.3 V drop across the active diode. The diode voltage drop varies with temperature.
16. Sum of all controller pins (including both digital and analog) must not exceed 150 mA. A $V_{DD\_HV\_IO}$ power segment is defined as one or more GPIO pins located between two $V_{DD\_HV\_IO}$ supply pins.

3.7 DC electrical specifications

The following table describes the DC electrical specifications.

Table 10. DC electrical specifications(1)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
I_{DD}	CC	P	Operating current all supply rails	f_{MAX}(2)	—	—	145	mA
I_{DDPE}	CC	C	Operating current all supplies including program/erase	f_{MAX}(3)	—	—	165	mA
I_{DDAPP}	CC	P	Operating current all supplies with typical application	At T_J<150°C	—	—	125	mA
I_{DDAR}	CC	P	$V_{DD\_HV\_IO}$ After Run operating current	At 40 °C Total device consumption on $V_{DD\_HV\_IO}$, including consumption for V_{DD_LV} generation. No I/O activity	—	—	22	mA
	CC	T		After-run mode HV current, T_A = 55 °C, $V_{DD\_HV\_IO}$ = 5.5 V	—	—	24	
I_{SPIKE}	CC	T	Maximum short term current spike	< 20 µs observation window	—	—	60	mA
dI	CC	T	Current difference ratio to average current (dI/avg(I))	< 20 µs observation window	—	—	20	%
I_{SR}	CC	D	Current variation during boot/shut-down	—	—	—	50	mA
$V_{REF\_BG\_T}$	CC	P	Bandgap trimmed reference voltage	T_J = –40 °C to 150 °C $V_{DD\_HV\_ADV}$ = 5 V ± 10%	1.200	—	1.237	V
$V_{REF\_BG\_TC}$	CC	C	Bandgap temperature coefficient(4)	T_J = –40 °C to 150 °C $V_{DD\_HV\_ADV}$ = 5 V ± 10%	-50	—	50	ppm /°C
$V_{REF\_BG\_LR}$	CC	C	Bandgap line regulation	T_J = –40 °C $V_{DD\_HV\_ADV}$ = 5 V ± 10%	—	—	8000	ppm /V
		C		T_J = 150 °C $V_{DD\_HV\_ADV}$ = 5 V ± 10%	—	—	4000	

1. The ranges in this table are design targets and actual data may vary in the given range.
2. f_{MAX} as specified per IP, unloaded I/O with LVDS pins active and terminated. Measured on an application specific pattern.
3. f_{MAX} as specified per IP, unloaded I/O with LVDS pins active and terminated. Measured on an application specific pattern with active flash program and erase.
4. The temperature coefficient and line regulation specifications are used to calculate the reference voltage drift at an operating point within the specified voltage and temperature operating conditions.

3.8 I/O pad specification

The following table describes the different pad type configurations.

Table 11. I/O pad specification descriptions

Pad type	Description
Weak configuration	Provides a good compromise between transition time and low electromagnetic emission. Pad impedance is centered around 800 Ω.
Medium configuration	Provides transition fast enough for the serial communication channels with controlled current to reduce electromagnetic emission. Pad impedance is centered around 200 Ω.
Strong configuration	Provides fast transition speed; used for fast interface. Pad impedance is centered around 50 Ω.
Very strong configuration	Provides maximum speed and controlled symmetric behavior for rise and fall transition. Used for fast interface including Ethernet interfaces requiring fine control of rising/falling edge jitter. Pad impedance is centered around 40 Ω.
Differential configuration	A few pads provide differential capability providing very fast interface together with good EMC performances.
Input only pads	These low input leakage pads are associated with the ADC channels.

Note: Each I/O pin on the device supports specific drive configurations. See the signal description table in the device reference manual for the available drive configurations for each I/O pin.

3.8.1 I/O input DC characteristics

Table 12 provides input DC electrical characteristics as described in *Figure 5*.

Figure 5. I/O input DC electrical characteristics definition

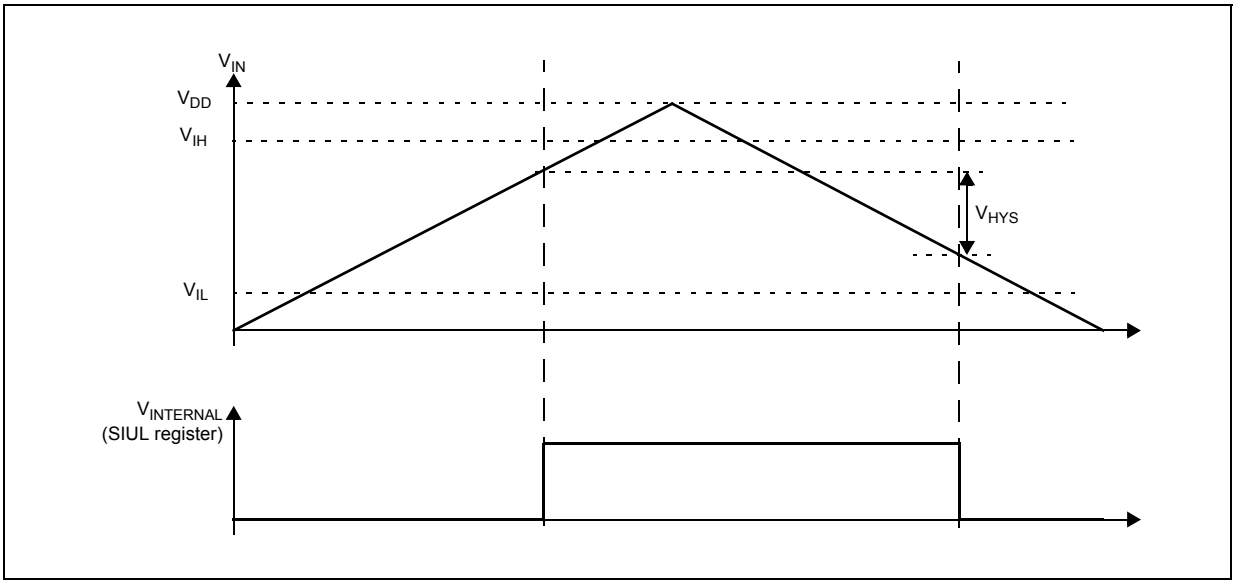


Table 12. I/O input DC electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
TTL								
V_{IHTTL}	SR	P	Input high level TTL	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V(6)	2	—	$V_{DD\_HV\_IO}$ + 0.3	V
V_{ILTTL}	SR	P	Input low level TTL	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V(6)	–0.3	—	0.8	
V_{HYSTTL}	—	C	Input hysteresis TTL	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V(6)	0.275	—	—	
$V_{DRFTTTL}$	—	T	Input V_{IL}/V_{IH} temperature drift TTL	—	—	—	100	mV
AUTOMOTIVE								
V_{IHAUT}(1)	SR	P	Input high level AUTOMOTIVE	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	3.8	—	$V_{DD\_HV\_IO}$ + 0.3	V
V_{ILAUT}(2)	SR	P	Input low level AUTOMOTIVE	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	–0.3	—	2.1(3)	V
V_{HYSAUT}(4)	—	C	Input hysteresis AUTOMOTIVE	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	0.4(3)	—	—	V
$V_{DRFTAUT}$	—	T	Input V_{IL}/V_{IH} temperature drift	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	—	—	100(5)	mV
CMOS								
V_{IHCMOS_H}(6)	SR	P	Input high level CMOS (with hysteresis)	3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	0.65 * $V_{DD\_HV\_IO}$	—	$V_{DD\_HV\_IO}$ + 0.3	V
				4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V				
V_{IHCMOS}(7)	SR	P	Input high level CMOS (without hysteresis)	3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	0.6 * $V_{DD\_HV\_IO}$	—	$V_{DD\_HV\_IO}$+ 0.3	V
				4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V				
V_{ILCMOS_H}(6)	SR	P	Input low level CMOS (with hysteresis)	3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	–0.3	—	0.35 * $V_{DD\_HV\_IO}$	V
				4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V				
V_{ILCMOS}(7)	SR	P	Input low level CMOS (without hysteresis)	3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	–0.3	—	0.4 * $V_{DD\_HV\_IO}$	V
				4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V				
$V_{HYSCMOS}$	—	C	Input hysteresis CMOS	3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	0.1 * $V_{DD\_HV\_IO}$	—	—	V
				4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V(8)				
$V_{DRFTCMOS}$	—	T	Input V_{IL}/V_{IH} temperature drift CMOS	3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	—	—	100(5)	mV
				4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V				
INPUT CHARACTERISTICS(7)								

Table 12. I/O input DC electrical characteristics (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
I_{LKG}	CC	P	Digital input leakage	4.5 V < V_{DD_HV} < 5.5 V 0.1*V_{DD_HV} < V_{IN} < 0.9*V_{DD_HV} TJ < 150 °C	—	—	1	µA
		C		4.5 V < V_{DD_HV} < 5.5 V V_{SS_HV} < V_{IN} < V_{DD_HV}	—	—	2	
I_{LKG_MED}	CC	C	Digital input leakage for MEDIUM pad	4.5 V < V_{DD_HV} < 5.5 V 0.1*V_{DD_HV} < V_{IN} < 0.9*V_{DD_HV}	—	—	500	nA
C_{IN}	CC	D	Digital input capacitance	GPIO input pins	—	—	10	pF
				Ethernet input pins	—	—	8	

1. A good approximation for the variation of the minimum value with supply is given by formula V_{IHAUT} = 0.69 × $V_{DD\_HV\_IO}$.
2. A good approximation for the variation of the maximum value with supply is given by formula V_{ILAUT} = 0.49 × $V_{DD\_HV\_IO}$.
3. Sum of V_{ILAUT} and V_{HYSAUT} is guaranteed to remain above 2.6 V in the 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V. Production test done with 2.06 V limit at cold, T_J < 25 °C.
4. A good approximation of the variation of the minimum value with supply is given by formula V_{HYSAUT} = 0.11 × $V_{DD\_HV\_IO}$.
5. In a 1 ms period, assuming stable voltage and a temperature variation of ±30 °C, V_{IL}/V_{IH} shift is within ±50 mV. For SENT requirement refer to NOTE on *page 34*.
6. Only for $V_{DD\_HV\_IO\_JTAG}$ and $V_{DD\_HV\_IO\_ETH}$ power segment. The TTL threshold are controlled by the VSIO bit. VSIO[VSIO_xx] = 0 in the range 3.0 V < $V_{DD\_HV\_IO}$ < 4.0 V, VSIO[VSIO_xx] = 1 in the range 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V.
7. For LFAST, microsecond bus and LVDS input characteristics, refer to dedicated communication module chapters.
8. Only for $V_{DD\_HV\_IO\_JTAG}$ and $V_{DD\_HV\_IO\_ETH}$ power segment.

Table 13 provides weak pull figures. Both pull-up and pull-down current specifications are provided.

Table 13. I/O pull-up/pull-down DC electrical characteristics

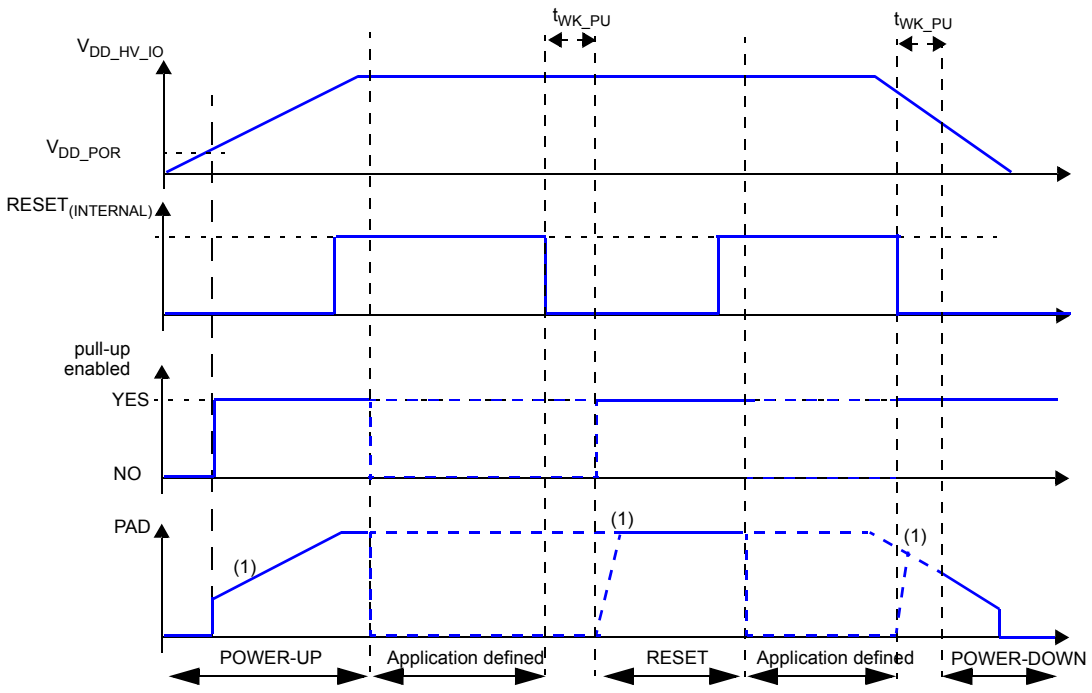
Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$\|I_{WPU}\|$	CC	T	Weak pull-up current absolute value(1)	V_{IN} = 0 V V_{DD_POR}(2) < $V_{DD\_HV\_IO}$ < 3.0 V(3)(4)	10.6 * V_{DD_HV} – 10.6	—	—	µA
	CC	T		V_{IN} > V_{IL} = 1.1 V (TTL) 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	—	—	130	
	CC	P		V_{IN} = 0.69* $V_{DD\_HV\_IO}$ 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	23	—	65	
	CC	T		V_{IN} = 0.49* $V_{DD\_HV\_IO}$ 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	—	—	82	
R_{WPU}	CC	D	Weak pull-up resistance	0.49* V_{DD_HVIO} < V_{IN} < 0.69* $V_{DD\_HV\_IO}$ 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	34	—	62	kΩ

Table 13. I/O pull-up/pull-down DC electrical characteristics (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$\|I_{WPD}\|$	CC	T	Weak pull-down current absolute value	$V_{IN} < V_{IL}$ = 0.9 V (TTL) 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	16	—	—	µA
		P		V_{IN} = 0.69* $V_{DD\_HV\_IO}$ 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	50	—	130	
		T		V_{IN} = 0.49* $V_{DD\_HV\_IO}$ 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	40	—	—	
R_{WPD}	CC	D	Weak pull-down resistance	0.49* $V_{DD\_HV\_IO}$ < V_{IN} < 0.69* $V_{DD\_HV\_IO}$ 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	30	—	55	kΩ

1. Weak pull-up/down is enabled within t_{WK_PU} = 1 µs after internal/external reset has been asserted. Output voltage will depend on the amount of capacitance connected to the pin.
2. V_{DD_POR} is the minimum $V_{DD\_HV\_IO}$ supply voltage for the activation of the device pull-up/down, and is given in the *Reset electrical characteristics* table of Section *Reset pad (PORST, ESR0) electrical characteristics* in this Datasheet.
3. V_{DD_POR} is defined in the *Table 19: Reset electrical characteristics* of *Section 3.10: Reset pad (PORST, ESR0) electrical characteristics* in this Datasheet.
4. Weak pull-up behavior during power-up. Operational with $V_{DD\_HV\_IO}$ > V_{DD_POR}.

Figure 6. Weak pull-up electrical characteristics definition

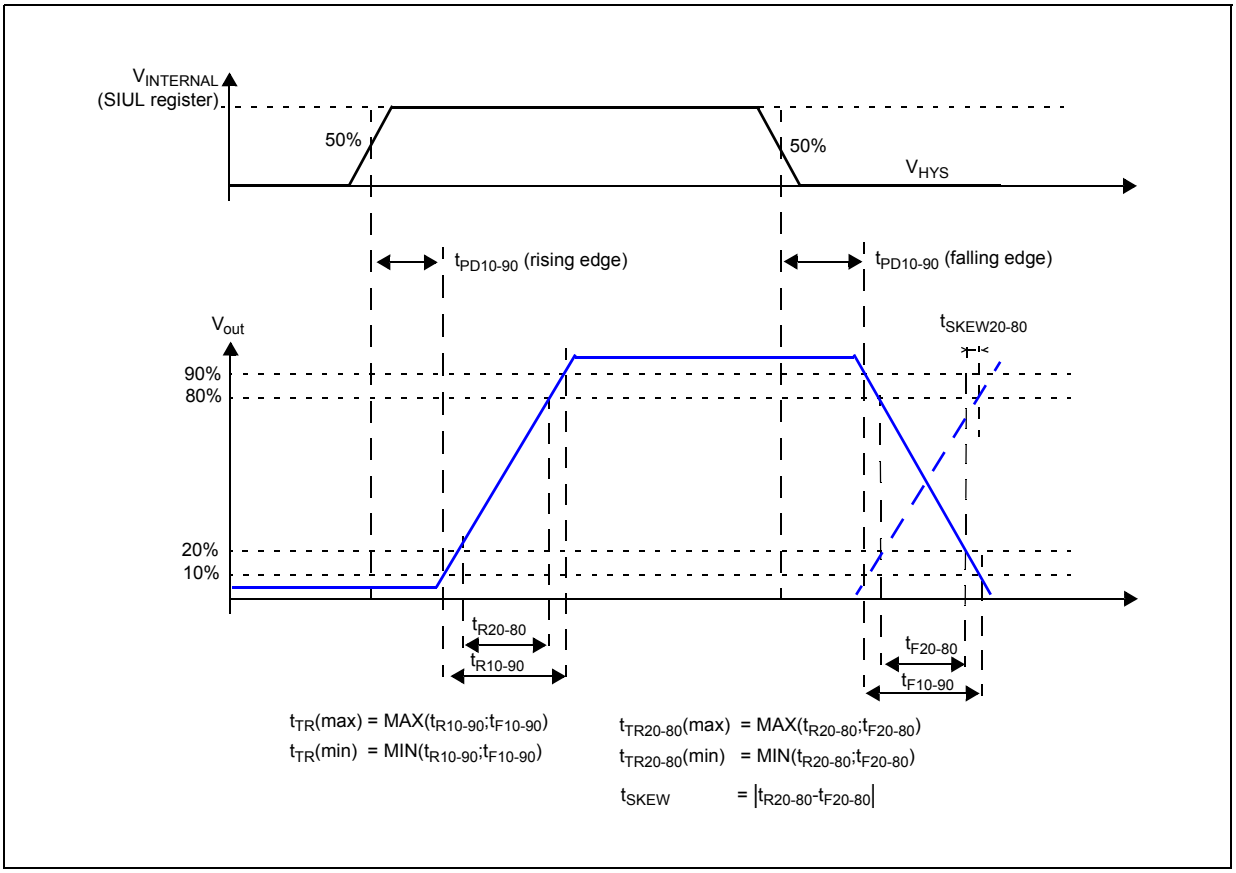


1. Actual PAD slopes will depend on external capacitances and VDD_HV_IO supply.

3.8.2 I/O output DC characteristics

The figure below provides description of output DC electrical characteristics.

Figure 7. I/O output DC electrical characteristics definition



The following tables provide DC characteristics for bidirectional pads:

- *Table 14* provides output driver characteristics for I/O pads when in WEAK configuration.
- *Table 15* provides output driver characteristics for I/O pads when in MEDIUM configuration.
- *Table 16* provides output driver characteristics for I/O pads when in STRONG configuration.
- *Table 17* provides output driver characteristics for I/O pads when in VERY STRONG configuration.

Note: Driver configuration is controlled by SIUL2_MSCRn registers. It is available within two PBRIDGEA_CLK clock cycles after the associated SIUL2_MSCRn bits have been written.

Table 14 shows the WEAK configuration output buffer electrical characteristics.

Table 14. WEAK configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
R_{OH_W}	CC	P	PMOS output impedance weak configuration	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V Push pull, I_{OH} < 0.5 mA	520	800	1040	Ω
R_{OL_W}	CC	P	NMOS output impedance weak configuration	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V Push pull, I_{OL} < 0.5 mA	520	800	1040	Ω
f_{MAX_W}	CC	T	Output frequency weak configuration	C_L = 25 pF[3]	—	—	2	MHz
				C_L = 50 pF[3]	—	—	1	
		D		C_L = 200 pF[3]	—	—	0.25	
t_{TR_W}	CC	T	Transition time output pin weak configuration[4]	C_L = 25 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	40	—	120	ns
				C_L = 50 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	80	—	240	
		D		C_L = 200 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	320	—	820	
				C_L = 25 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[5]	50	—	150	
				C_L = 50 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[5]	100	—	300	
				C_L = 200 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[5]	350	—	1050	
$\lvert t_{SKEW\_W} \rvert$	CC	T	Difference between rise and fall time	—	—	—	25	%
I_{DCMAX_W}	CC	D	Maximum DC current	—	—	—	4	mA
$T_{PHL/PLH}$	CC	D	Propagation delay	C_L = 25 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V	—	—	120	ns
				C_L = 25 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	—	—	150	
				C_L = 50 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V	—	—	240	
				C_L = 50 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[5]	—	—	300	

1. All VDD_HV_IO conditions for 4.5V to 5.5V are valid for VSIO[VSIO_xx] = 1, and all specifications for 3.0V to 3.6V are valid for VSIO[VSIO_xx] = 0
2. All values need to be confirmed during device validation.
3. C_L is the sum of external capacitance. Device and package capacitances (C_{IN}, defined in *Table 12*) are to be added to calculate total signal capacitance ($C_{TOT} = C_L + C_{IN}$).
4. Transition time maximum value is approximated by the following formula:

   0 pF < C_L < 50 pFt_{TR_W}(ns) = 22 ns + C_L(pF) × 4.4 ns/pF

   50 pF < C_L < 200 pFt_{TR_W}(ns) = 50 ns + C_L(pF) × 3.85 ns/pF
5. Only for $V_{DD\_HV\_IO\_JTAG}$ segment when VSIO[VSIO_IJ] = 0 or $V_{DD\_HV\_IO\_ETH}$ segment when VSIO[VSIO_IF] = 0.

Table 15 shows the MEDIUM configuration output buffer electrical characteristics.

Table 15. MEDIUM configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
R_{OH_M}	CC	P	PMOS output impedance MEDIUM configuration	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V Push pull, I_{OH} < 2 mA	120	200	260	Ω
R_{OL_M}	CC	P	NMOS output impedance MEDIUM configuration	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V Push pull, I_{OL} < 2 mA	120	200	260	Ω
f_{MAX_M}	CC	T	Output frequency MEDIUM configuration	C_L = 25 pF[3]	—	—	12	MHz
				C_L = 50 pF[3]	—	—	6	
		D		C_L = 200 pF[3]	—	—	1.5	
t_{TR_M}	CC	T	Transition time output pin MEDIUM configuration[4]	C_L = 25 pF 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	10	—	30	ns
				C_L = 50 pF 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	20	—	60	
		D		C_L = 200 pF 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	60	—	200	
				C_L = 25 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[5]	12	—	42	
				C_L = 50 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[5]	24	—	86	
				C_L = 200 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[5]	70	—	300	
$\lvert t_{SKEW\_M} \rvert$	CC	T	Difference between rise and fall time	—	—	—	25	%
I_{DCMAX_M}	CC	D	Maximum DC current	—	—	—	4	mA
$T_{PHL/PLH}$	CC	D	Propagation delay	C_L = 25 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V	—	—	35	ns
				C_L = 25 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	—	—	42	
				C_L = 50 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V	—	—	70	
				C_L = 50 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[5]	—	—	85	

1. All $V_{DD\_HV\_IO}$ conditions for 4.5 V to 5.5 V are valid for VSIO[VSIO_xx] = 1, and all specifications for 3.0V to 3.6V are valid for VSIO[VSIO_xx] = 0
2. All values need to be confirmed during device validation.
3. C_L is the sum of external capacitance. Device and package capacitances (C_{IN}, defined in *Table 12*) are to be added to calculate total signal capacitance (C_{TOT} = C_L + C_{IN}).

4. Transition time maximum value is approximated by the following formula:
   0 pF < C_L < 50 pFt_{TR_M}(ns) = 5.6 ns + C_L(pF) × 1.11 ns/pF
   50 pF < C_L < 200 pFt_{TR_M}(ns) = 13 ns + C_L(pF) × 0.96 ns/pF
5. Only for $V_{DD\_HV\_IO\_JTAG}$ segment when VSIO[VSIO_IJ] = 0 or $V_{DD\_HV\_IO\_ETH}$ segment when VSIO[VSIO_IF] = 0

Table 16 shows the STRONG configuration output buffer electrical characteristics.

Table 16. STRONG configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions(1)	Value(2)			Unit
					Min	Typ	Max	
R_{OH_S}	CC	P	PMOS output impedance STRONG configuration	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V Push pull, I_{OH} < 8 mA	30	50	65	Ω
R_{OL_S}	CC	P	NMOS output impedance STRONG configuration	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V Push pull, I_{OL} < 8 mA	30	50	65	Ω
f_{MAX_S}	CC	T	Output frequency STRONG configuration	C_L = 25 pF(3)	—	—	40	MHz
				C_L = 50 pF(3)	—	—	20	
				C_L = 200 pF(3)	—	—	5	
t_{TR_S}	CC	T	Transition time output pin STRONG configuration(4)	C_L = 25 pF 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	2.5	—	10	ns
				C_L = 50 pF 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	3.5	—	16	
				C_L = 200 pF 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	13	—	50	
				C_L = 25 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V(5)	4	—	15	
				C_L = 50 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V(5)	6	—	27	
				C_L = 200 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V(5)	20	—	83	
I_{DCMAX_S}	CC	D	Maximum DC current	—	—	—	10	mA
$\|t_{SKEW\_S}\|$	CC	T	Difference between rise and fall time	—	—	—	25	%

Table 16. STRONG configuration output buffer electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
$T_{PHL/PLH}$	CC	D	Propagation delay	C_L = 25 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V	—	—	12	ns
				C_L = 25 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	—	—	18	
				C_L = 50 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V	—	—	20	
				C_L = 50 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[5]	—	—	36	

1. All $V_{DD\_HV\_IO}$ conditions for 4.5 V to 5.5 V are valid for VSIO[VSIO_xx] = 1, and all specifications for 3.0 V to 3.6 V are valid for VSIO[VSIO_xx] = 0
2. All values need to be confirmed during device validation.
3. C_L is the sum of external capacitance. Device and package capacitances (C_{IN}, defined in *Table 12*) are to be added to calculate total signal capacitance ($C_{TOT} = C_L + C_{IN}$).
4. Transition time maximum value is approximated by the following formula: t_{TR_S}(ns) = 4.5 ns + C_L(pF) x 0.23 ns/pF.
5. Only for $V_{DD\_HV\_IO\_JTAG}$ segment when VSIO[VSIO_IJ] = 0 or $V_{DD\_HV\_IO\_ETH}$ segment when VSIO[VSIO_IF] = 0

Table 17 shows the VERY STRONG configuration output buffer electrical characteristics.

Table 17. VERY STRONG configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
R_{OH_V}	CC	P	PMOS output impedance VERY STRONG configuration	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%, VSIO[VSIO_xx] = 1, I_{OH} = 8 mA	20	40	60	Ω
		C		$V_{DD\_HV\_IO}$ = 3.3 V ± 10%, VSIO[VSIO_xx] = 0, I_{OH} = 7 mA[3]	30	50	75	
R_{OL_V}	CC	P	NMOS output impedance VERY STRONG configuration	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%, VSIO[VSIO_xx] = 1, I_{OL} = 8 mA	20	40	60	Ω
		C		$V_{DD\_HV\_IO}$ = 3.3 V ± 10%, VSIO[VSIO_xx] = 0, I_{OL} = 7 mA[3]	30	50	75	
f_{MAX_V}	CC	T	Output frequency VERY STRONG configuration	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%, C_L = 25 pF[4]	—	—	50	MHz
				VSIO[VSIO_xx] = 1, C_L = 15 pF[3],[4]	—	—	50	

Table 17. VERY STRONG configuration output buffer electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
t_{TR_V}	CC	T	10–90% threshold transition time output pin VERY STRONG configuration	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%, C_L = 25 pF[4]	1	—	5.3	ns
				$V_{DD\_HV\_IO}$ = 5.0 V ± 10%, C_L = 50 pF[4]	2.5	—	12	
				$V_{DD\_HV\_IO}$ = 5.0 V ± 10%, C_L = 200 pF[4]	11	—	45	
$t_{TR20-80}$	CC	—	20–80% threshold transition time output pin VERY STRONG configuration	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%, C_L = 25 pF[4]	0.8	—	4	ns
				$V_{DD\_HV\_IO}$ = 3.3 V ± 10%, C_L = 15 pF[4]	1	—	5	
t_{TRTTL}	CC	—	TTL threshold transition time[5] for output pin in VERY STRONG configuration	$V_{DD\_HV\_IO}$ = 3.3 V ± 10%, C_L = 25 pF[4]	1	—	5	ns
$\Sigma t_{TR20-80}$	CC	—	Sum of transition time 20–80% output pin VERY STRONG configuration	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%, C_L = 25 pF	—	—	9	ns
				$V_{DD\_HV\_IO}$ = 3.3 V ± 10%, C_L = 15 pF[4]	—	—	9	
$\lvert t_{SKEW\_V} \rvert$	CC	T	Difference between rise and fall time at 20–80%	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%, C_L = 25 pF[4]	0	—	1	ns
$T_{PHL/PLH}$	CC	D	Propagation delay	C_L = 25 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V	—	—	9	ns
				C_L = 25 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	—	—	10.5	
				C_L = 50 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V	—	—	15	
				C_L = 50 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	—	—	12	
I_{DCMAX_VS}	CC	D	Maximum DC current	—	—	—	10	mA

1. All $V_{DD\_HV\_IO}$ conditions for 4.5 V to 5.5 V are valid for VSIO[VSIO_xx] = 1, and all specifications for 3.0 V to 3.6 V are valid for VSIO[VSIO_xx] = 0.
2. All values need to be confirmed during device validation.
3. Only available on the $V_{DD\_HV\_IO\_JTAG}$ and $V_{DD\_HV\_IO\_ETH}$ segments.
4. C_L is the sum of external capacitance. Add device and package capacitances (C_{IN}, defined in the *Table 12: I/O input DC electrical characteristics* in this Datasheet) to calculate total signal capacitance (C_{TOT} = C_L + C_{IN}).
5. TTL transition time as for Ethernet standard.

3.9 I/O pad current specification

The I/O pads are distributed across the I/O supply segment. Each I/O supply segment is associated to a V_{DD}/V_{SS} supply pair.

Table 18 provides I/O consumption figures.

In order to ensure device reliability, the average current of the I/O on a single segment should remain below the I_{AVGSEG} maximum value.

In order to ensure device functionality, the sum of the dynamic and static currents of the I/O on a single segment should remain below the I_{DYNSEG} maximum value.

Pad mapping on each segment can be optimized using the pad usage information provided in the I/O Signal Description table. The sum of all pad usage ratios within a segment should remain below 100%.

Note: In order to maintain the required input thresholds for the SENT interface, the sum of all I/O pad output percent IR drop as defined in the I/O Signal Description table, must be below 50 %. See the I/O Signal Description attachment.

Note: The SPC572Lx I/O Signal Description and Input Multiplexing Tables are contained in a Microsoft Excel® workbook file attached to this document. Locate the paperclip symbol on the left side of the PDF window, and click it. Double-click on the Excel file to open it and select the I/O Signal Description Table tab.

Table 18. I/O consumption(1)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
I_{RMS_SEG}	SR	D	Sum of all the DC I/O current within a supply segment	V_{DD} = 5.0 V ± 10%	—	—	80	mA
				V_{DD} = 3.3 V ± 10%	—	—	80	
I_{RMS_W}	CC	D	RMS I/O current for WEAK configuration	C_L = 25 pF, 2 MHz V_{DD} = 5.0 V ± 10%	—	—	1.1	mA
				C_L = 50 pF, 1 MHz V_{DD} = 5.0 V ± 10%	—	—	1.1	
				C_L = 25 pF, 2 MHz V_{DD} = 3.3 V ± 10%	—	—	0.6	
				C_L = 50 pF, 1 MHz V_{DD} = 3.3 V ± 10%	—	—	0.6	
I_{RMS_M}	CC	D	RMS I/O current for MEDIUM configuration	C_L = 25 pF, 12 MHz V_{DD} = 5.0 V ± 10%	—	—	4.7	mA
				C_L = 50 pF, 6 MHz V_{DD} = 5.0 V ± 10%	—	—	4.8	
				C_L = 25 pF, 12 MHz V_{DD} = 3.3 V ± 10%	—	—	2.6	
				C_L = 50 pF, 6 MHz V_{DD} = 3.3 V ± 10%	—	—	2.7	

Table 18. I/O consumption(1) (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
I_{RMS_S}	CC	D	RMS I/O current for STRONG configuration	C_L = 25 pF, 50 MHz V_{DD} = 5.0 V ± 10%	—	—	19	mA
				C_L = 50 pF, 25 MHz V_{DD} = 5.0 V ± 10%	—	—	19	
				C_L = 25 pF, 50 MHz V_{DD} = 3.3 V ± 10%	—	—	10	
				C_L = 50 pF, 25 MHz V_{DD} = 3.3 V ± 10%	—	—	10	
I_{RMS_V}	CC	D	RMS I/O current for VERY STRONG configuration	C_L = 25 pF, 50 MHz, V_{DD} = 5.0V +/- 10%	—	—	22	mA
				C_L = 50 pF, 25 MHz, V_{DD} = 5.0V ± 10%	—	—	22	
				C_L = 25 pF, 50 MHz, V_{DD} = 3.3V ± 10%	—	—	11	
				C_L = 25 pF, 25 MHz, V_{DD} = 3.3V ± 10%	—	—	11	
I_{DYN_SEG}	SR	D	Sum of all the dynamic and DC I/O current within a supply segment	V_{DD} = 5.0 V ± 10%	—	—	195	mA
				V_{DD} = 3.3 V ± 10%	—	—	150	
I_{DYN_W}(2)	CC	D	Dynamic I/O current for WEAK configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%	—	—	5.0	mA
				C_L = 50 pF, V_{DD} = 5.0 V ± 10%	—	—	5.1	
				C_L = 25 pF, V_{DD} = 3.3 V ± 10%	—	—	2.2	
				C_L = 50 pF, V_{DD} = 3.3 V ± 10%	—	—	2.3	
I_{DYN_M}	CC	D	Dynamic I/O current for MEDIUM configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%	—	—	15	mA
				C_L = 50 pF, V_{DD} = 5.0 V ± 10%	—	—	15.5	
				C_L = 25 pF, V_{DD} = 3.3 V ± 10%	—	—	7.0	
				C_L = 50 pF, V_{DD} = 3.3 V ± 10%	—	—	7.1	

Table 18. I/O consumption(1) (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
I_{DYN_S}	CC	D	Dynamic I/O current for STRONG configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%	—	—	50	mA
				C_L = 50 pF, V_{DD} = 5.0 V ± 10%	—	—	55	
				C_L = 25 pF, V_{DD} = 3.3 V ± 10%	—	—	22	
				C_L = 50 pF, V_{DD} = 3.3 V ± 10%	—	—	25	
I_{DYN_V}	CC	D	Dynamic I/O current for VERY STRONG configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%	—	—	60	mA
				C_L = 50 pF, V_{DD} = 5.0 V ± 10%	—	—	64	
				C_L = 25 pF, V_{DD} = 3.3 V ± 10%	—	—	26	
				C_L = 50 pF, V_{DD} = 3.3 V ± 10%	—	—	29	

1. I/O current consumption specifications for the 4.5 V <= $V_{DD\_HV\_IO}$ <= 5.5 V range are valid for VSIO_[VSIO_xx] = 1, and VSIO[VSIO_xx] = 0 for 3.0 V <= $V_{DD\_HV\_IO}$ <= 3.6 V.
2. Stated maximum values represent peak consumption that lasts only a few ns during I/O transition. When possible (timed output) it is recommended to delay transition between pads by few cycles to reduce noise and consumption.

3.10 Reset pad ($\overline{\text{PORST}}$, $\overline{\text{ESR0}}$) electrical characteristics

The device implements a dedicated bidirectional reset pin ($\overline{\text{PORST}}$).

Note: $\overline{PORST}$ pin does not require active control. It is possible to implement an external pull-up to ensure correct reset exit sequence. Recommended value is 4.7 kΩ.

Figure 8. Start-up reset requirements

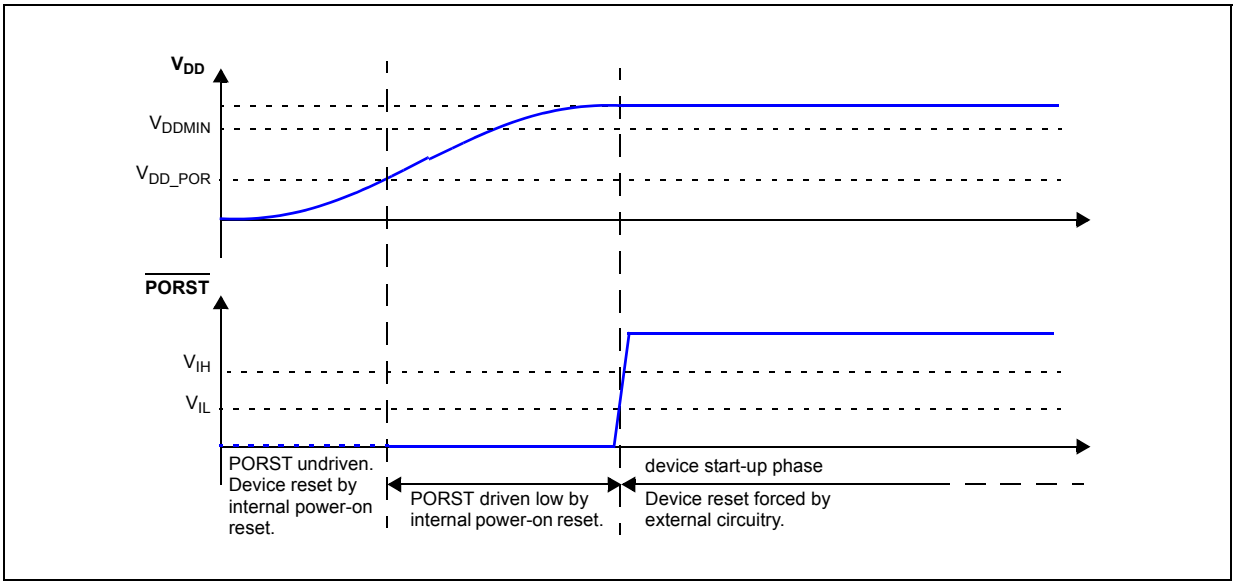


Figure 9 describes device behavior depending on supply signal on $\overline{PORST}$:

1. $\overline{PORST}$ low pulse amplitude is too low—it is filtered by input buffer hysteresis. Device remains in current state.
2. $\overline{PORST}$ low pulse duration is too short—it is filtered by a low pass filter. Device remains in current state.
3. $\overline{PORST}$ low pulse generates a reset:
   a) $\overline{PORST}$ low but initially filtered during at least W_{FRST}. Device remains initially in current state.
   b) $\overline{PORST}$ potentially filtered until W_{NFRST}. Device state is unknown: it may either be reset or remains in current state depending on other factors (temperature, voltage, device).
   c) $\overline{PORST}$ asserted for longer than W_{NFRST}. Device is under reset.

Figure 9. Noise filtering on reset signal

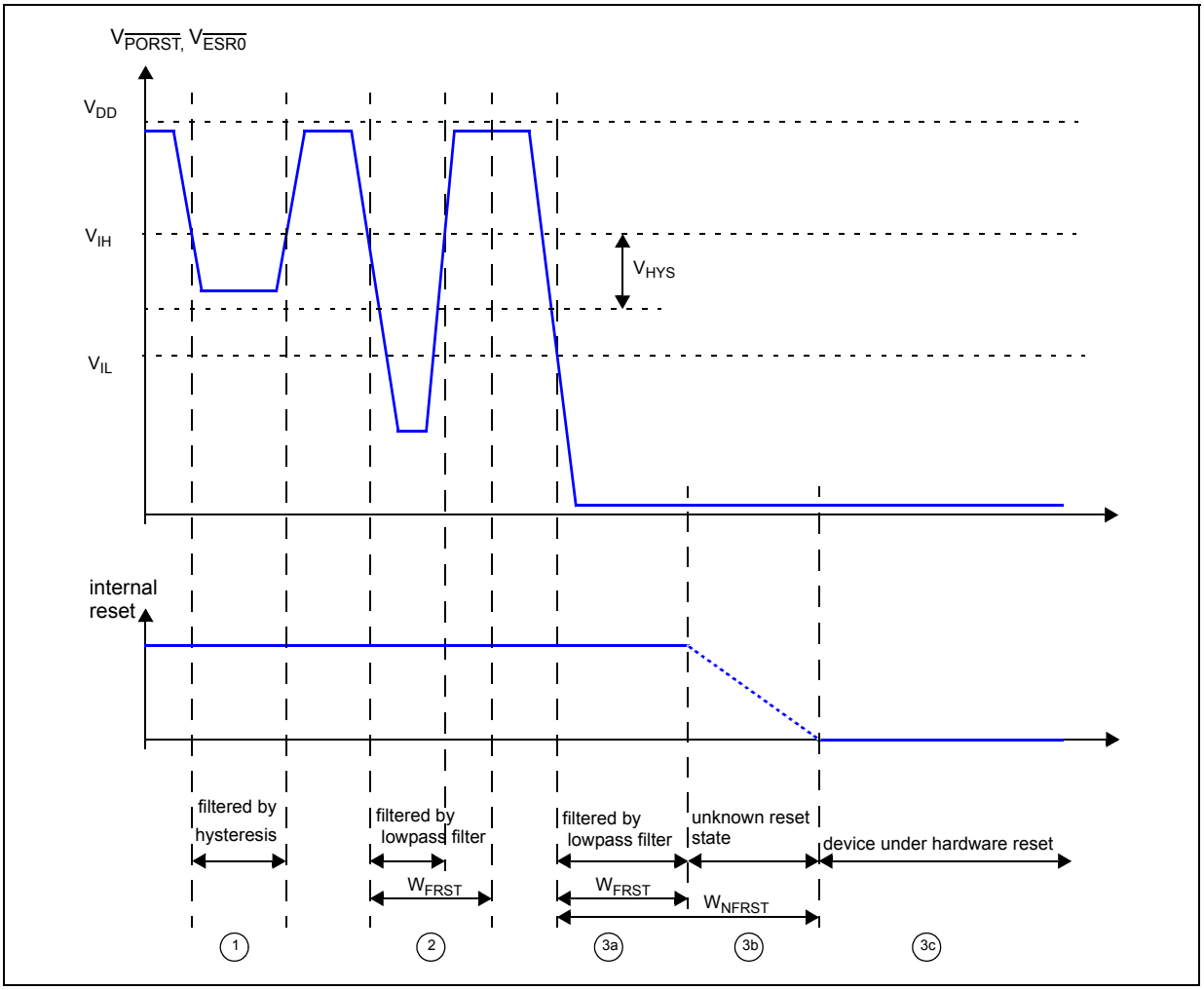


Table 19. Reset electrical characteristics

Symbol			Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{IH}	SR	P	Input high level TTL (Schmitt trigger)	—	2.0	—	$V_{DD\_HV\_IO}$ +0.4	V
V_{IL}	SR	P	Input low level TTL (Schmitt trigger)	—	–0.4	—	0.8	V
V_{HYS}	CC	C	Input hysteresis TTL (Schmitt trigger)	—	275	—	—	mV
V_{DD_POR}	CC	C	Minimum supply for strong pull-down activation	—	—	—	1.2	V

Table 19. Reset electrical characteristics (continued)

Symbol			Parameter	Conditions	Value			Unit
					Min	Typ	Max	
I_{OL_R}	CC	C	Strong pull-down current(1)	Device under power-on reset $V_{DD\_HV\_IO} = V_{DD\_POR}$, $V_{OL} = 0.35 * V_{DD\_HV\_IO}$	0.2	—	—	mA
				—	—	—	—	—
				Device under power-on reset $3.0\ V < V_{DD\_HV\_IO} < 5.5\ V$, $V_{OL} > 1.0\ V$	12	—	—	mA
$\lvert I_{WPU} \rvert$	CC	P	Weak pull-up current absolute value	$\overline{ESR0}$ pin $V_{IN} = 0.69 * V_{DD\_HV\_IO}$	23	—	—	µA
				$\overline{ESR0}$ pin $V_{IN} = 0.49 * V_{DD\_HV\_IO}$	—	—	82	
$\lvert I_{WPD} \rvert$	CC	P	Weak pull-down current absolute value	$\overline{PORST}$ pin $V_{IN} = 0.69 * V_{DD\_HV\_IO}$	—	—	130	µA
				$\overline{PORST}$ pin $V_{IN} = 0.49 * V_{DD\_HV\_IO}$	40	—	—	
W_{FRST}	SR	P	$\overline{PORST}$ and $\overline{ESR0}$ input filtered pulse	—	—	—	500	ns
W_{NFRST}	SR	P	$\overline{PORST}$ and $\overline{ESR0}$ input not filtered pulse	—	2000	—	—	ns
W_{FNMI}	SR	P	ESR1 input filtered pulse	—	—	—	15	ns
W_{NFNMI}	SR	P	ESR1 input not filtered pulse	—	400	—	—	ns

1. I_{OL_R} applies to both PORST and ESR0: Strong pull-down is active on PHASE0 for PORST. Strong pull-down is active on PHASE0, PHASE1, PHASE2, and the beginning of PHASE3 for ESR0.

$\overline{PORST}$ must be connected to an external power-on supply circuitry. Minimum requested circuitry is external pull-up to ensure device can exit reset.

Note: No restrictions exist on reset signal slew rate apart from absolute maximum rating compliance.

3.11 Oscillator and PLL

Single phase-locked loop (PLL) module with the reference PLL (PLL0) generating the system and auxiliary clocks from the main oscillator driver.

Figure 10. PLL integration

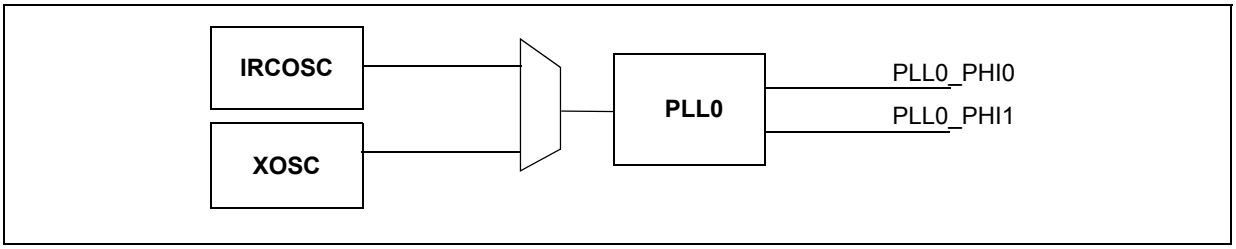


Table 20. PLL0 electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
f_{PLL0IN}	SR	—	PLL0 input clock[1],[2]	—	8	—	44	MHz
Δ_{PLL0IN}	SR	—	PLL0 input clock duty cycle[1]	—	40	—	60	%
$f_{PLL0VCO}$	CC	P	PLL0 VCO frequency	—	600	—	1250	MHz
$f_{PLL0PHI0}$	CC	P	PLL0 output frequency	—	4.762	—	80	MHz
$f_{PLL0PHI1}$	CC	P	PLL0 output frequency	—	4.762	—	100	MHz
$t_{PLL0LOCK}$	CC	P	PLL0 lock time	—	—	—	110	µs
$\lvert\Delta_{PLL0PHI0SPJ}\rvert$	CC	T	PLL0_PHI0 single period jitter f_{PLL0IN} = 20 MHz (resonator)	$f_{PLL0PHI0}$ = 400 MHz, 6-sigma pk-pk	—	—	200	ps
$\lvert\Delta_{PLL0PHI1SPJ}\rvert$	CC	T	PLL0_PHI1 single period jitter f_{PLL0IN} = 20 MHz (resonator)	$f_{PLL0PHI1}$ = 40 MHz, 6-sigma pk-pk	—	—	300[3]	ps
$\Delta_{PLL0LTJ}$	CC	T	PLL0 output long term jitter[3] f_{PLL0IN} = 20 MHz (resonator), VCO frequency = 800 MHz	10 periods accumulated jitter (80 MHz equivalent frequency), 6-sigma pk-pk	—	—	± 250	ps
				16 periods accumulated jitter (50 MHz equivalent frequency), 6-sigma pk-pk	—	—	± 300	ps
				long term jitter (< 1 MHz equivalent frequency), 6-sigma pk-pk	—	—	± 500	ps
I_{PLL0}	CC	C	PLL0 consumption	FINE LOCK state	—	—	5	mA
$f_{PLL0FREE}$	CC	D	VCO free running frequency	—	35	—	400	MHz

1. PLL0IN clock retrieved directly from either Internal RC Oscillator (IRCOSC) or External Oscillator (XOSC) clock. Input characteristics are granted when using XOSC.
2. f_{PLL0IN} frequency must be scaled down using PLLDIG_PLL0DV[PREDIV] to ensure PFD input signal is in the range of 8 MHz-20 MHz.
3. V_{DD_LV} noise due to application in the range V_{DD_LV} = 1.25 V ± 5% with frequency below PLL bandwidth (40 kHz) is filtered.

Table 21. External oscillator electrical specifications

Symbol		C	Parameter	Conditions		Value		Unit
						Min	Max	
f_{XTAL}	CC	D	Crystal frequency range(1)	—		4	8	MHz
				—		> 8	20	
				—		> 20	40	
t_{cst}	CC	T	Crystal start-up time(2)(3)	—		—	5	ms
t_{rec}	CC	T	Crystal recovery time(4)	—		—	0.5	ms
V_{IHEXT}	CC	D	EXTAL input high voltage (External Reference)	V_{REF} = 0.28 * $V_{DD\_HV\_IO\_JTAG}$		V_{REF} + 0.6	—	V
V_{ILEXT}	CC	D	EXTAL input low voltage(5)	V_{REF} = 0.28 * $V_{DD\_HV\_IO\_JTAG}$		—	V_{REF} - 0.6	V
C_{S_EXTAL}	CC	T	Total on-chip stray capacitance on EXTAL pin	—		—	2.5 + value from *Table 22*	pF
C_{S_XTAL}	CC	T	Total on-chip stray capacitance on XTAL pin	—		—	2.5 + value from *Table 22*	pF
g_m	CC	D	Oscillator Transconductance	T_J = -40 °C to 150 °C 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	$f_{XTAL} \leq$ 8 MHz	2.6	11.0	mA/V
		D			$f_{XTAL} \leq$ 20 MHz	7.9	26.0	
		D			$f_{XTAL} \leq$ 40 MHz	10.4	34.0	
I_{XTAL}	CC	D	XTAL current(6)	T_J = 150 °C		—	14	mA
V_{HYS}	CC	D	Comparator Hysteresis	T_J = 150 °C		0.1	1.0	V

1. The range is selectable by DCF record.
2. This value is determined by the crystal manufacturer and board design.
3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal recovery time is the time for the oscillator to settle to the correct frequency after adjustment of the integrated load capacitor value.
5. Applies to an external clock input and not to crystal mode.
6. I_{XTAL} is the oscillator bias current out of the XTAL pin with both EXTAL and XTAL pins grounded. Test circuit is shown in *Figure 11*.

Table 22. Selectable load capacitance

load_cap_sel[4:0] from DCF record	Capacitance offered on EXTAL/XTAL (Cx and Cy)[1],[2] (pF)
00000	1.0
00001	2.0
00010	2.9
00011	3.8
00100	4.8
00101	5.7
00110	6.6
00111	7.5
01000	8.5
01001	9.4
01010	10.3
01011	11.2
01100	12.2
01101	13.1
01110	14.0
01111	15.0
10000–11111[3]	Reserved

1. Values are determined from simulation across process corners and voltage and temperature variation. Capacitance values vary ±12% across process, 0.25% across voltage, and no variation across temperature.
2. Values in this table do not include the die and package capacitances given by C_{S_XTAL}/C_{S_EXTAL} in *Table 21 (External oscillator electrical specifications)*.
3. Configurations 10000–11111 should not be used. Configurations 10000–11100 result in same capacitances of configurations 00011–01111. Configurations 11101, 11110, and 11111 select maximum capacitances.

Figure 11. Test circuit

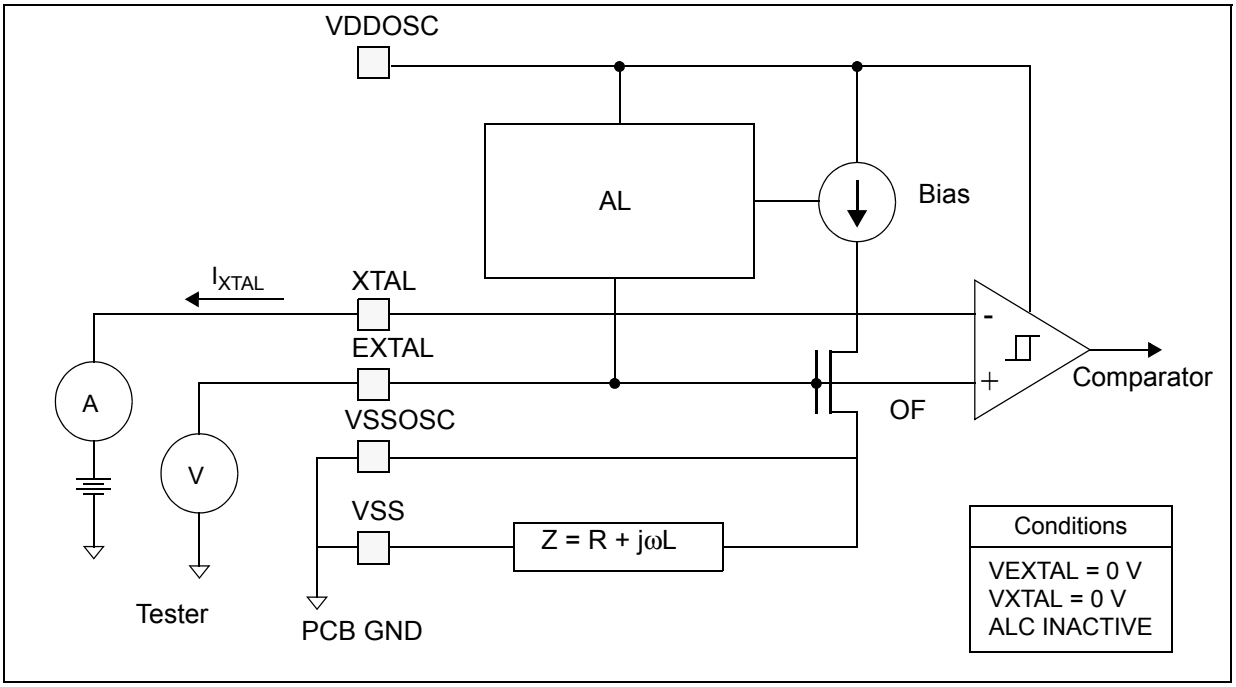


Table 23. Internal RC oscillator electrical specifications

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
f_{Target}	CC	D	IRC target frequency	—	—	16	—	MHz
δf_{var_noT}	CC	P	IRC frequency variation without temperature compensation	—	–8	—	+8	%
δf_{var_T}	CC	T	IRC frequency variation with temperature compensation	T_J < 150 °C	–1.5	—	+1.5	%
δf_{var_SW}	—	T	IRC frequency accuracy after software trimming accuracy(1)	Trimming temperature	–1	—	+1	%
t_{start_noT}	CC	T	Startup time to reach within f_{var_noT}	Factory trimming already applied	—	—	5	µs
t_{start_T}	CC	D	Startup time to reach within f_{var_T}	Factory trimming already applied	—	—	120	µs

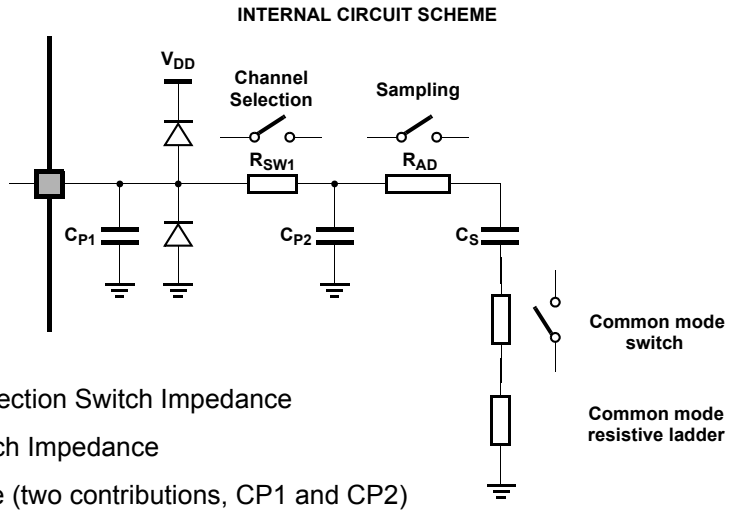
1. The typical user trim step size of δf_{TRIM} = 0.35 %

3.12 ADC specifications

3.12.1 ADC input description

Figure 12 shows the input equivalent circuit for fast SARn channels.

Figure 12. Input equivalent circuit (Fast SARn channels)



RSW1 Channel Selection Switch Impedance

RADSampling Switch Impedance

CP Pin Capacitance (two contributions, CP1 and CP2)

CS Sampling Capacitance

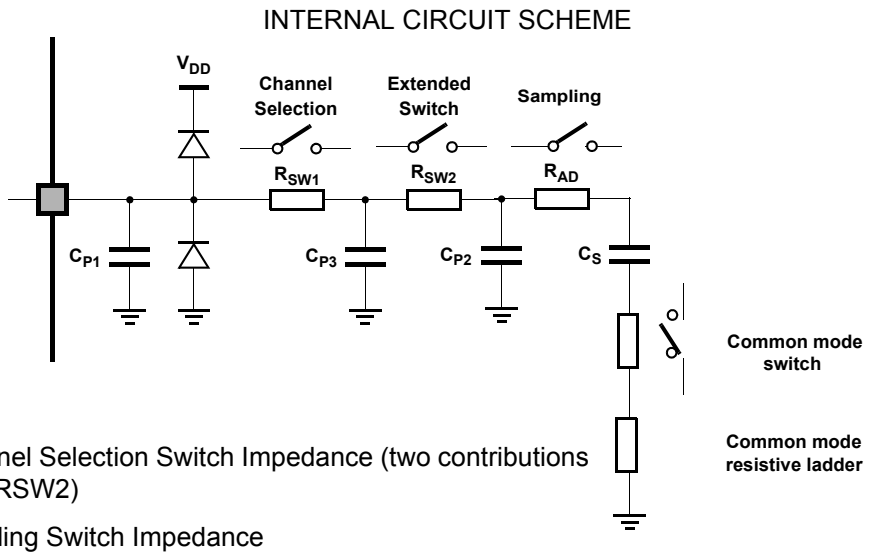
RCMSWCommon mode switch

RCMLCommon mode resistive ladder

This figure can be used as approximation circuitry for external filtering definition.It is also applicable for channel AN16, AN17 and AN24 (Fast channels).

Figure 13 shows the input equivalent circuit for SARB channels.

Figure 13. Input equivalent circuit (SARB channels)



RSW: Channel Selection Switch Impedance (two contributions RSW1 and RSW2)

RAD: Sampling Switch Impedance

CP: Pin Capacitance (three contributions, CP1, CP2 and CP3)

CS: Sampling Capacitance

RCMSW: Common mode switch

RCML: Common mode resistive ladder

The above figure can be used as approximation circuitry for external filtering definition.

It is applicable for all SARB channels except AN 16, AN17 and AN24 (Fast channels).

Table 24. ADC pin specification(1)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
I_{LK_INUD}	CC	C	Input leakage current, two ADC channels input with weak pull-up and weak pull-down	T_J < 40 °C, no current injection on adjacent pin	—	70	nA
		C		T_J < 150 °C, no current injection on adjacent pin	—	220	
I_{LK_INUSD}	CC	C	Input leakage current, two ADC channels input with weak pull-up and strong pull-down	T_J < 40 °C, no current injection on adjacent pin	—	80	nA
		C		T_J < 150 °C, no current injection on adjacent pin	—	250	

Table 24. ADC pin specification(1) (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
I_{LK_INREF}	CC	C	Input leakage current, two ADC channels input with weak pull-up and weak pull-down and alternate reference	T_J< 40 °C, no current injection on adjacent pin	—	160	nA
		C		T_J < 150 °C, no current injection on adjacent pin	—	400	
I_{LK_INOUT}	CC	C	Input leakage current, two ADC channels input, GPIO output buffer with weak pull-up and weak pull-down	T_J < 40 °C, no current injection on adjacent pin	—	140	nA
		C		T_J < 150 °C, no current injection on adjacent pin	—	380	
I_{INJ}	CC	T	Injection current on analog input preserving functionality	Applies to any analog pins	–3	3	mA
C_{HV_ADC}	SR	D	$V_{DD\_HV\_ADV}$ external capacitance(2)		1	2.2	µF
C_{P1}	CC	D	Pad capacitance	—	0	10	pF
C_{P2}	CC	D	Internal routing capacitance	SARn channels	0	0.5	pF
		D		SARB channels(3)	0	1	
C_{P3}	CC	D	Internal routing capacitance	Only for SARB channels	0	1	pF
C_S	CC	D	SAR ADC sampling capacitance	—	6	8.5	pF
R_{SWn}	CC	D	Analog switches resistance	SARn channels	0	1.1	kΩ
		D		SARB channels(4)	0	1.7	
R_{AD}	CC	D	ADC input analog switches resistance	—	0	0.6	kΩ
R_{CMSW}	CC	D	Common mode switch resistance	—	0	2.6	kΩ
R_{CMRL}	CC	D	Common mode resistive ladder	—	0	3.5	kΩ
R_{SAFEPD}(4)	CC	D	Discharge resistance for AN7 channels (strong pull-down for safety)	—	0	300	W
ΣI_{ADR}	CC	C+P	Sum of ADC and S/D reference consumption	ADC enabled	—	40	µA

1. All specifications in this table valid for the full input voltage range for the analog inputs.
2. For noise filtering, add a high frequency bypass capacitance of 0.1 µF between $V_{DD\_HV\_ADV}$ and $V_{SS\_HV\_ADV}$.
3. Characteristics corresponding to fast SARn channels also apply to SARB fast channels (AN16, AN17 and AN24).
4. Safety pull-down is available for port pin PE[14]. It enables discharge of up to 100 nF from 5 V every 300 ms.

3.12.2 SAR ADC electrical specification

The SARn ADCs are 12-bit Successive Approximation Register analog-to-digital converters with full capacitive DAC. The SARn architecture allows input channel multiplexing.

Table 25. SARn ADC electrical specification(1)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
V_{ALTREF}	SR	P	ADC alternate reference voltage	$V_{ALTREF} < V_{DD\_HV\_IO\_MAIN}$ $V_{ALTREF} < V_{DD\_HV\_ADV}$	4.5	5.5	V
		C			2.0	4.0	
		C			4.0	5.9	
V_{IN}	SR	D	ADC input signal	$0 < V_{IN} < V_{DD\_HV\_IO\_MAIN}$	$V_{SS\_HV\_ADR}$	$V_{DD\_HV\_ADR}$	V
f_{ADCK}	SR	P	Clock frequency	$T_J < 150$ °C	7.5	14.6	MHz
$t_{ADCPRECH}$	SR	T	ADC precharge time	Fast SAR—fast precharge	135	—	ns
				Fast SAR—full precharge	270	—	
				Slow SAR (SARADC_B)(2)—fast precharge	270	—	
				Slow SAR (SARADC_B)(2)—full precharge	540	—	
ΔV_{PRECH}	SR	D	ADC precharge voltage	Full precharge $V_{PRECH} = V_{DD\_HV\_ADR}/2$ $T_J < 150$ °C	–0.25	0.25	V
		D		Fast precharge $V_{PRECH} = V_{DD\_HV\_ADR}/2$ $T_J < 150$ °C	–0.5	0.5	V
ΔV_{INTREF}	CC	P	Internal reference voltage precision	Applies to all internal reference points ($V_{SS\_HV\_ADR}$, 1/3 * $V_{DD\_HV\_ADR}$, 2/3 * $V_{DD\_HV\_ADR}$, $V_{DD\_HV\_ADR}$)	–0.20	0.20	V
$t_{ADCSAMPLE}$	SR	P	ADC sample time(3)	Fast SAR – 12-bit configuration	0.750	—	µs
		D		Fast SAR – 10-bit configuration	0.555	—	
		P		Slow SAR (SARADC_B)(2) – 12-bit configuration	1.500	—	
		D		Slow SAR (SARADC_B)(2) – 10-bit configuration	0.833	—	
$t_{ADCEVAL}$	SR	P	ADC evaluation time	12-bit configuration (25 clock cycles)	1.712	—	µs
		D		10-bit configuration (21 clock cycles)	1.458	—	

Table 25. SARn ADC electrical specification[1] (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
$I_{ADCREFH}$[4], [5]	CC	T	ADC high reference current[6]	Dynamic consumption $t_{conv} \geq 5$ µs (average across all codes)	—	3.5[7]	µA
				Dynamic consumption $t_{conv} \geq 2.5$ µs (average across all codes)	—	7[8]	
				Static consumption (Power Down mode)	—	+8	
		T		Bias Current[9]	—	+2	
$I_{ADCREFL}$[5]	CC	D	ADC low reference current	Run mode $t_{conv} \geq 5$ µs $V_{DD\_HV\_ADR}$ <= 5.5 V	—	15	µA
				Run mode t_{conv} = 2.5 µs $V_{DD\_HV\_ADR}$ <= 5.5 V	—	30	
				Power Down mode $V_{DD\_HV\_ADR}$ <= 5.5 V	—	1	
I_{ADV_S}	CC	P	$V_{DD\_HV\_ADV}$ power supply current	Run mode[5] $t_{conv} \geq 5$ µs	—	4.0	mA
TUE_{12}	CC	T[10]	Total unadjusted error in 12-bit configuration[11]	T_J < 150 °C, $V_{DD\_HV\_ADV}$ > 4 V, $V_{DD\_HV\_ADR}$, V_{ALTREF}> 4 V	–4	4	LSB (12b)
		P		T_J < 150 °C, $V_{DD\_HV\_ADV}$ > 4 V, $V_{DD\_HV\_ADR}$, V_{ALTREF}> 4 V	–6	6	
		T		T_J < 150 °C, $V_{DD\_HV\_ADV}$ > 4 V, 4 V > V_{ALTREF}> 2 V	–6	6	
		T		T_J < 150 °C, 4 V > $V_{DD\_HV\_ADV}$ > 3.5 V	–12	12	
TUE_{10}	CC	T	Total unadjusted error in 10-bit configuration	T_J < 150 °C, $V_{DD\_HV\_ADV}$ > 4 V $V_{DD\_HV\_ADR}$, V_{ALTREF} > 4 V	–1.5	1.5	LSB (10b)
		T		T_J < 150 °C, $V_{DD\_HV\_ADV}$ > 4 V, 4 V > $V_{DD\_HV\_ADR}$, V_{ALTREF}> 2 V	–2.0	2.0	

Table 25. SARn ADC electrical specification[1] (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
Δ_{TUE12}	CC	D	TUE degradation due to $V_{DD\_HV\_ADR}$ offset with respect to $V_{DD\_HV\_ADV}$	$V_{IN} < V_{DD\_HV\_ADV}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [0:25 mV]	0	0	LSB (12b)
		D		$V_{IN} < V_{DD\_HV\_ADV}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [25:50 mV]	–2	2	
		D		$V_{IN} < V_{DD\_HV\_ADV}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [50:75 mV]	–4	4	
		D		$V_{IN} < V_{DD\_HV\_ADV}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [75:100 mV]	–6	6	
		D		$V_{DD\_HV\_ADV} < V_{IN} < V_{DD\_HV\_ADR}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [0:25 mV]	–2.5	2.5	
		D		$V_{DD\_HV\_ADV} < V_{IN} < V_{DD\_HV\_ADR}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [25:50 mV]	–4	4	
		D		$V_{DD\_HV\_ADV} < V_{IN} < V_{DD\_HV\_ADR}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [50:75 mV]	–7	7	
		D		$V_{DD\_HV\_ADV} < V_{IN} < V_{DD\_HV\_ADR}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [75:100 mV]	–12	12	
DNL	CC	P	Differential non-linearity	$V_{DD\_HV\_ADV} > 4$ V $V_{DD\_HV\_ADR} > 4$ V	–1	2	LSB (12b)

1. Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.
2. Characteristics corresponding to SARB channels apply only for slow SAR channels i.e., all SARB channels except AN16, AN17, and AN24.
3. Minimum ADC sample times are dependent on adequate charge transfer from the external driving circuit to the internal sample capacitor. The time constant of the entire circuit must allow the sampling capacitor to charge within 1/2 LSB within the sampling window. Please refer to *Figure 12* and *Figure 13* for models of the internal ADC circuit, and the values to use in external RC sizing and calculating the sampling window duration.
4. $I_{ADCREFH}$ and $I_{ADCREFL}$ are independent from ADC clock frequency. It depends on conversion rate: consumption is driven by the transfer of charge between internal capacitances during the conversion.
5. Current parameter values are for a single ADC.
6. Total consumption is given by the sum for all ADCs (associated to the reference pin) of their dynamic consumption and their static consumption.
7. Typical consumption is 2 µA.
8. Typical consumption is 4 µA.

9. Extra bias current is present only when BIAS is selected. Apply only once for all ADCs.
10. Extended bench validation performed on 3 samples for each process corner.
11. This parameter is guaranteed by bench validation with a small sample of typical devices, and tested in production to ± 6 LSB.

3.12.3 S/D ADC electrical specification

The SDn ADCs are Sigma Delta 16-bit analog-to-digital converters with 333 Ksps maximum output rate.

Table 26. SDn ADC electrical specification(1)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{IN}	SR	P	ADC input signal	—	0	—	$V_{DD\_HV\_ADR\_D}$	V
V_{IN_PK2PK}(2)	SR	D	Input range peak to peak $V_{IN\_PK2PK} = V_{INP}$(3) $- V_{INM}$(4)	Single ended $V_{INM} = V_{SS\_HV\_ADR}$	$V_{DD\_HV\_ADR}$/GAIN			V
		D		Single ended $V_{INM} = 0.5*V_{DD\_HV\_ADR}$ GAIN = 1	±0.5*$V_{DD\_HV\_ADR}$			
		D		Single ended $V_{INM} = 0.5*V_{DD\_HV\_ADR}$ GAIN = 2,4,8,16	±$V_{DD\_HV\_ADR}$/GAIN			
		D		Differential, $0 < V_{IN} < V_{DD\_HV\_IO\_MAIN}$	±$V_{DD\_HV\_ADR}$/GAIN			
f_{ADCD_M}	SR	P	S/D modulator Input Clock	—	4	14.4	16	MHz
f_{IN}	SR	D	Input signal frequency	SNR = 80 dB f_{ADCD_S} = 150 kHz	0.01	—	50(5)	kHz
		D		SNR = 74 dB f_{ADCD_S} = 333 kHz	0.01	—	111(5)	
f_{ADCD_S}	SR	D	Output conversion rate	—	—	—	333	ksps
—	CC	D	Oversampling ratio	Internal modulator	24	—	256	—
				External modulator	—	—	256	—
RESOLUTION	CC	D	S/D register resolution(6)	2's complement notation	16			bit
GAIN	SR	D	ADC gain	Defined via ADC_SD[PGA] register. Only integer powers of 2 are valid gain values.	1	—	16	—

Table 26. SDn ADC electrical specification(1) (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$\lvert\delta_{GAIN}\rvert$	CC	C	Absolute value of the ADC gain error(7),(8)	Before calibration (applies to gain setting = 1)	—	—	1.5	%
		D		After calibration, $\Delta V_{DD\_HV\_ADR} < 5\%$ $\Delta V_{DD\_HV\_ADV} < 10\%$ $\Delta T_J < 50$ °C	—	—	5	mV
				After calibration, $\Delta V_{DD\_HV\_ADR} < 5\%$ $\Delta V_{DD\_HV\_ADV} < 10\%$ $\Delta T_J < 100$ °C	—	—	7.5	
				After calibration, $\Delta V_{DD\_HV\_ADR} < 5\%$ $\Delta V_{DD\_HV\_ADV} < 10\%$ $\Delta T_J < 150$ °C	—	—	10	
V_{OFFSET}	CC	P	Input Referred Offset Error(7),(8),(9)	Before calibration (applies to all gain settings – 1, 2, 4, 8, 16)	—	10* (1+1/gain)	20	mV
		D		After calibration, $\Delta V_{DD\_HV\_ADR} < 10\%$ $\Delta T_J < 50$ °C	—	—	5	
				After calibration, $\Delta V_{DD\_HV\_ADV} < 10\%$ $\Delta T_J < 100$ °C			7.5	
				After calibration, $\Delta V_{DD\_HV\_ADV} < 10\%$ $\Delta T_J < 150$ °C	0.5		10	

Table 26. SDn ADC electrical specification(1) (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$SNR_{DIFF150}$	CC	P	Signal to noise ratio in differential mode 150 ksps output rate	$4.5 < V_{DD\_HV\_ADV} < 5.5$ $V_{DD\_HV\_ADR} = V_{DD\_HV\_ADV}$ GAIN = 1 $T_J < 150$ °C	80	—	—	dBFS
		C		$4.5 < V_{DD\_HV\_ADV} < 5.5$ $V_{DD\_HV\_ADR} = V_{DD\_HV\_ADV}$ GAIN = 2 $T_J < 150$ °C	77	—	—	
		C		$4.5 < V_{DD\_HV\_ADV} < 5.5$ $V_{DD\_HV\_ADR} = V_{DD\_HV\_ADV}$ GAIN = 4 $T_J < 150$ °C	74	—	—	
		C		$4.5 < V_{DD\_HV\_ADV} < 5.5$ $V_{DD\_HV\_ADR} = V_{DD\_HV\_ADV}$ GAIN = 8 $T_J < 150$ °C	71	—	—	
		D		$4.5 < V_{DD\_HV\_ADV} < 5.5$ $V_{DD\_HV\_ADR} = V_{DD\_HV\_ADV}$ GAIN = 16 $T_J < 150$ °C	68	—	—	
$SNR_{DIFF333}$	CC	P	Signal to noise ratio in differential mode 333 ksps output rate	$4.5 < V_{DD\_HV\_ADV} < 5.5$ $V_{DD\_HV\_ADR} = V_{DD\_HV\_ADV}$ GAIN = 1 $T_J < 150$ °C	74	—	—	dBFS
		C		$4.5 < V_{DD\_HV\_ADV} < 5.5$ $V_{DD\_HV\_ADR} = V_{DD\_HV\_ADV}$ GAIN = 2 $T_J < 150$ °C	71	—	—	
		C		$4.5 < V_{DD\_HV\_ADV} < 5.5$ $V_{DD\_HV\_ADR} = V_{DD\_HV\_ADV}$ GAIN = 4 $T_J < 150$ °C	68	—	—	
		C		$4.5 < V_{DD\_HV\_ADV} < 5.5$ $V_{DD\_HV\_ADR} = V_{DD\_HV\_ADV}$ GAIN = 8 $T_J < 150$ °C	65	—	—	
		D		$4.5 < V_{DD\_HV\_ADV} < 5.5$ $V_{DD\_HV\_ADR} = V_{DD\_HV\_ADV}$ GAIN = 16 $T_J < 150$ °C	62	—	—	

Table 26. SDn ADC electrical specification(1) (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
SNR_{SE150}	CC	C	Signal to noise ratio in single ended mode 150 ksps output rate(10)	4.5 < $V_{DD\_HV\_ADV}$ < 5.5 $V_{DD\_HV\_ADR}$ = $V_{DD\_HV\_ADV}$ GAIN = 1 T_J < 150 °C	74	—	—	dBFS
		P		4.5 < $V_{DD\_HV\_ADV}$ < 5.5 $V_{DD\_HV\_ADR}$ = $V_{DD\_HV\_ADV}$ GAIN = 1 T_J < 150 °C	68	—	—	
		T		4.5 < $V_{DD\_HV\_ADV}$ < 5.5 $V_{DD\_HV\_ADR}$ = $V_{DD\_HV\_ADV}$ GAIN = 2 T_J < 150 °C	71	—	—	
				4.5 < $V_{DD\_HV\_ADV}$ < 5.5 $V_{DD\_HV\_ADR}$ = $V_{DD\_HV\_ADV}$ GAIN = 4 T_J < 150 °C	68	—	—	
				4.5 < $V_{DD\_HV\_ADV}$ < 5.5 $V_{DD\_HV\_ADR}$ = $V_{DD\_HV\_ADV}$ GAIN = 8 T_J < 150 °C	65	—	—	
		D		4.5 < $V_{DD\_HV\_ADV}$ < 5.5 $V_{DD\_HV\_ADR}$=$V_{DD\_HV\_ADV}$ GAIN = 16 T_J < 150 °C	62	—	—	
SFDR	CC	P	Spurious free dynamic range	GAIN = 1	60	—	—	dBc
		C		GAIN = 2	60	—	—	
		C		GAIN = 4	60	—	—	
		C		GAIN = 8	60	—	—	
		D		GAIN = 16	60	—	—	
Z_{DIFF}(11)	CC	D	Differential input impedance	GAIN = 1	1000	1250	1500	kΩ
				GAIN = 2	600	800	1000	
				GAIN = 4	300	400	500	
				GAIN = 8	200	250	300	
				GAIN = 16	200	250	300	
Z_{CM}(11)	CC	D	Common mode input impedance	GAIN = 1	1400	1800	2200	kΩ
				GAIN = 2	1000	1300	1600	
				GAIN = 4	700	950	1150	
				GAIN = 8	500	650	800	
				GAIN = 16	500	650	800	

Table 26. SDn ADC electrical specification(1) (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
ΔV_{INTCM}	CC	D	Common mode input reference voltage	—	-12%	—	+12%	
R_{BIAS}	CC	D	Bare bias resistance	—	110	144	180	kΩ
V_{BIAS}	CC	D	Bias voltage	—	—	$V_{DD\_HV\_ADR}/2$	—	V
δV_{BIAS}	CC	D	Bias voltage accuracy	—	–2.5	—	+2.5	%
CMRR	SR	D	Common mode rejection ratio	—	54	—	—	dB
R_{Caaf}	SR	D	Anti-aliasing filter	External series resistance	—	—	20	kΩ
	CC	D		Filter capacitances	180	—	—	pF
$f_{PASSBAND}$	CC	D	Pass band(12)	—	0.01	—	0.333 * f_{ADCD_S}	kHz
δ_{RIPPLE}	CC	D	Pass band ripple(13)	0.333 * f_{ADCD_S}	–1	—	1	%
$F_{rolloff}$	CC	D	Stop band attenuation	[0.5 * f_{ADCD_S}, 1.0 * f_{ADCD_S}]	40	—	—	dB
				[1.0 * f_{ADCD_S}, 1.5 * f_{ADCD_S}]	45	—	—	
				[1.5 * f_{ADCD_S}, 2.0 * f_{ADCD_S}]	50	—	—	
				[2.0 * f_{ADCD_S}, 2.5 * f_{ADCD_S}]	55	—	—	
				[2.5 * f_{ADCD_S}, f_{ADCD_M}/2]	60	—	—	

Table 26. SDn ADC electrical specification(1) (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
δ_{GROUP}	CC	D	Group delay	Within pass band – Tclk is f_{ADCD_M} / 2	—	—	—	—
				OSR = 24	—	—	238.5	Tclk
				OSR = 28	—	—	278	
				OSR = 32	—	—	317.5	
				OSR = 36	—	—	357	
				OSR = 40	—	—	396.5	
				OSR = 44	—	—	436	
				OSR = 48	—	—	475.5	
				OSR = 56	—	—	554.5	
				OSR = 64	—	—	633.5	
				OSR = 72	—	—	712.5	
				OSR = 75	—	—	699	
				OSR = 80	—	—	791.5	
				OSR = 88	—	—	870.5	
				OSR = 96	—	—	949.5	
				OSR = 112	—	—	1107.5	
				OSR = 128	—	—	1265.5	
				OSR = 144	—	—	1423.5	
				OSR = 160	—	—	1581.5	
				OSR = 176	—	—	1739.5	
				OSR = 192	—	—	1897.5	
				OSR = 224	—	—	2213.5	
				OSR = 256	—	—	2529.5	
				Distortion within pass band	–0.5/ f_{ADCD_S}	—	+0.5/ f_{ADCD_S}	—
f_{HIGH}	CC	D	High pass filter 3dB frequency	Enabled	—	10e-5* f_{ADCD_S}	—	—
$t_{STARTUP}$	CC	D	Start-up time from power down state	—	—	—	100	µs
$t_{LATENCY}$	CC	D	Latency between input data and converted data when input mux does not change	HPF = ON	—	—	δ_{GROUP} + f_{ADCD_S}	—
				HPF = OFF	—	—	δ_{GROUP}	—

Table 26. SDn ADC electrical specification(1) (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$t_{SETTLING}$	CC	D	Settling time after mux change	Analog inputs are muxed HPF = ON	—	—	$2*\delta_{GROUP} + 3*f_{ADCD\_S}$	—
				HPF = OFF	—	—	$2*\delta_{GROUP} + 2*f_{ADCD\_S}$	—
$t_{ODRECOVERY}$	CC	D	Overdrive recovery time	After input comes within range from saturation HPF = ON	—	—	$2*\delta_{GROUP} + f_{ADCD\_S}$	—
				HPF = OFF	—	—	$2*\delta_{GROUP}$	—
C_{S_D}	CC	D	S/D ADC sampling capacitance after sampling switch(14)	GAIN = 1, 2, 4, 8	—	—	75*GAIN	fF
		D		GAIN = 16	—	—	600	fF
IBIAS	CC	D	Bias consumption	At least 1 ADCD enabled	—	—	3.5	mA
I_{ADV_D}	CC	P	$V_{DD\_HV\_ADV}$ power supply current (single S/D ADC)	S/D ADC Dynamic consumption	—	—	3.5	mA
I_{ADCS/D_REFH}	CC	T	S/D ADC Reference High Current	Dynamic consumption (Conversion)	—	—	3.5	µA
		T		Static consumption (Power down)	—	—	+8	

1. Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.
2. For input voltage above the maximum and below the clamp voltage of the input pad, there is no latch-up concern, and the signal will only be 'clipped'.
3. V_{INP} is the input voltage applied to the positive terminal of the SDADC.
4. V_{INM} is the input voltage applied to the negative terminal of the SDADC.
5. Maximum input of 166.67 kHz supported with reduced accuracy. See SNR specifications.
6. When using a GAIN setting of 16, the conversion result will always have a value of zero in the least significant bit. This gives an effective resolution of 15 bits.
7. Offset and gain error due to temperature drift can occur in either direction (+/-) for each of the SDADCs on the device.
8. Calibration of gain is possible when gain = 1.
   Offset Calibration should be done with respect to $0.5*V_{DD\_HV\_ADR}$ for *differential mode* and *single ended mode with negative input=0.5*$V_{DD\_HV\_ADR}$*.
   Offset Calibration should be done with respect to 0 for "single ended mode with negative input=0".
   Both offset and Gain Calibration is guaranteed for ±5% variation of $V_{DD\_HV\_ADR}$, ±10% variation of $V_{DD\_HV\_ADV}$, and ± 50 °C temperature variation.
9. Conversion offset error must be divided by the applied gain factor (1, 2, 4, 8, or 16) to obtain the actual input referred offset error.
10. This parameter is guaranteed by bench validation with a small sample of typical devices, and tested in production to a value of 6 dB less.
11. Impedance given at f_{ADCD_M} = 16 MHz. Impedance is inversely proportional to frequency:
    $Z_{DIFF}(f_{ADCD\_M})$ = 16 MHz/f_{ADCD_M}* Z_{DIFF}
    $Z_{CM}(f_{ADCD\_M})$ = 16 MHz/f_{ADCD_M}* Z_{CM}
12. SNR values guaranteed only if external noise on the ADC input pin is attenuated by the required SNR value in the frequency range of $f_{ADCD\_M} - f_{ADCD\_S}$ to $f_{ADCD\_M} + f_{ADCD\_S}$, where f_{ADCD_M} is the input sampling frequency, and f_{ADCD_S} is the output sample frequency. A proper external input filter should be used to remove any interfering signals in this frequency range.
13. The ±1% passband ripple specification is equivalent to 20 * $\log_{10}$ (0.99) = 0.087 dB.

14. This capacitance does not include pin capacitance, that can be considered together with external capacitance, before sampling switch.

3.13 Temperature sensor

The following table describes the temperature sensor electrical characteristics.

Table 27. Temperature sensor electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
—	CC	—	Temperature monitoring range	—	–40	—	150	°C
T_{SENS}	CC	P	Sensitivity	—	—	5.18	—	mV/°C
T_{ACC}	CC	P	Accuracy	T_J < 150 °C	–3	—	3	°C
I_{TEMP_SENS}	CC	C	$V_{DD\_HV\_ADV}$ power supply current	—	—	—	700	µA

3.14 LVDS Fast Asynchronous Serial Transmission (LFAST) pad electrical characteristics

The LFAST pad electrical characteristics apply to both the SIPI and high-speed debug serial interfaces on the device. The same LVDS pad is used for the Microsecond Channel (MSC) and DSPI LVDS interfaces, with different characteristics given in the following tables.

3.14.1 LFAST interface timing diagrams

Figure 14. LFAST and MSC/DSPI LVDS timing definition

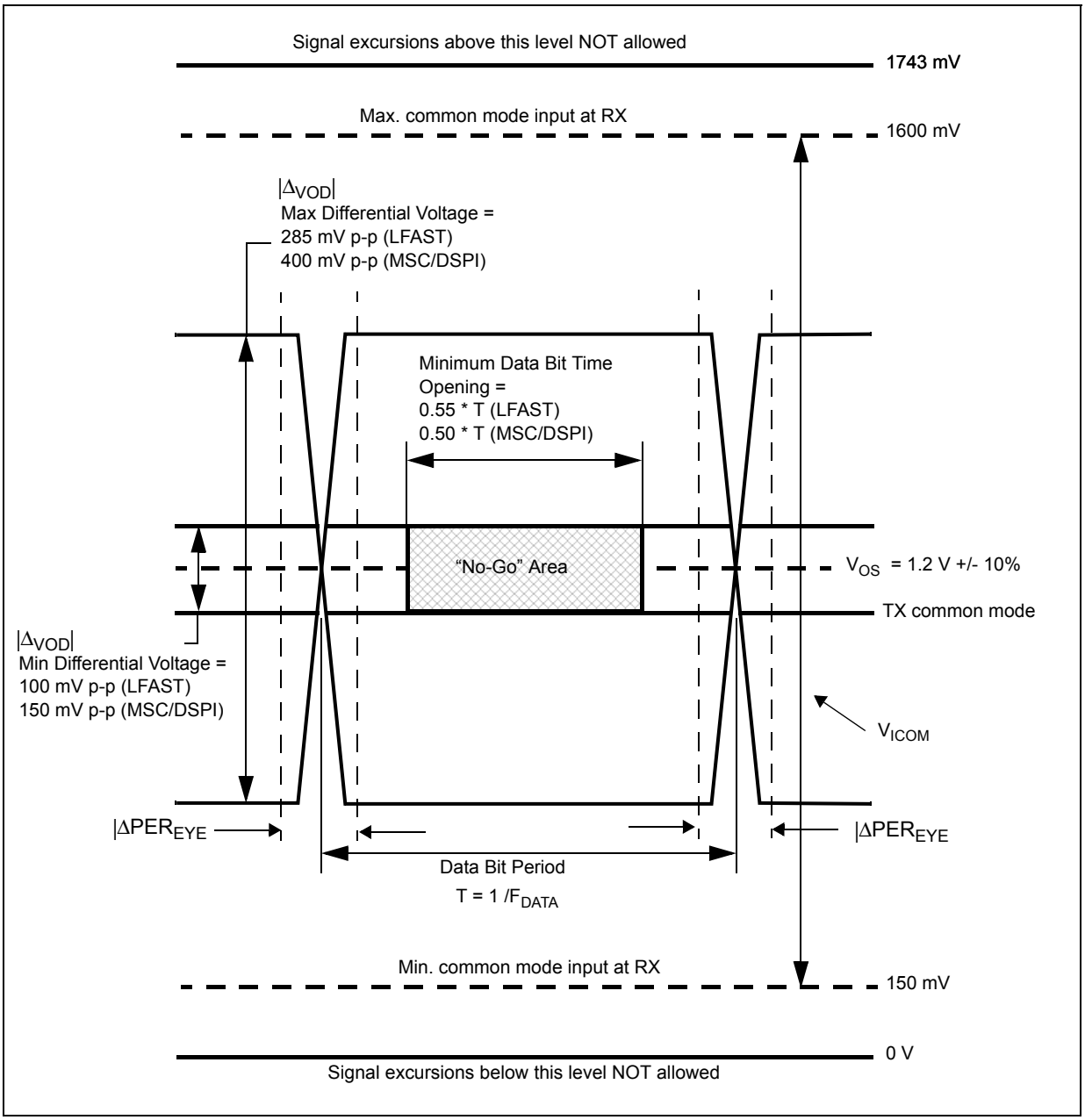


Figure 15. Power-down exit time

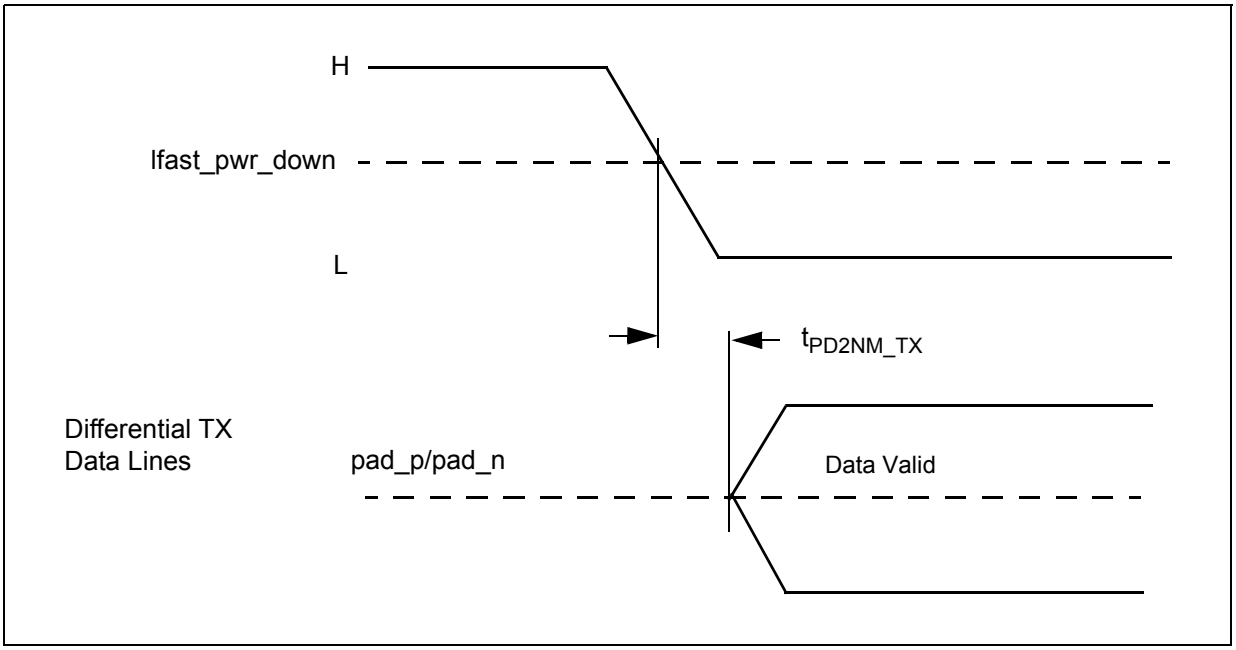
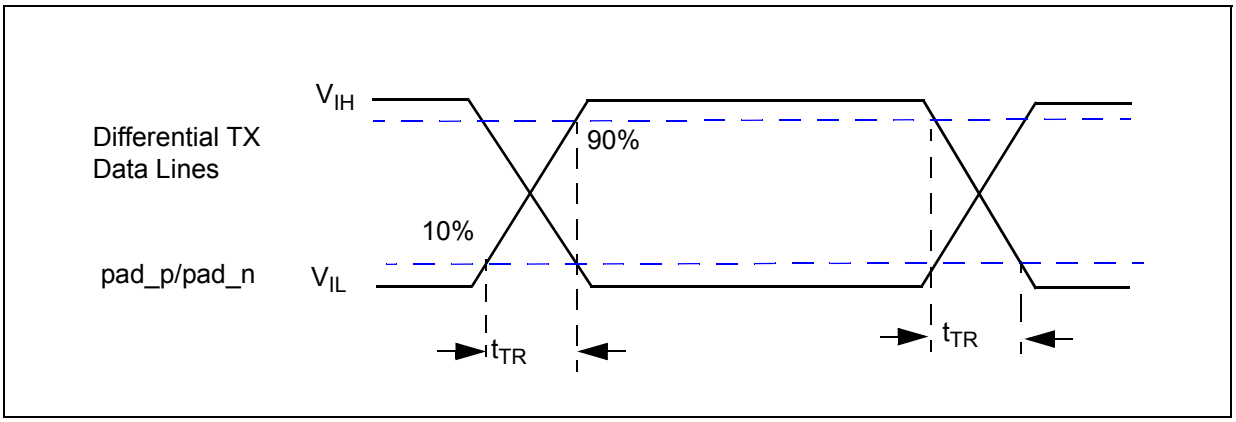


Figure 16. Rise/fall time



3.14.2 LFAST and MSC/DSPI LVDS interface electrical characteristics

The following table contains the electrical characteristics for the LFAST interface.

Table 28. LVDS pad startup and receiver electrical characteristics(1)(2)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
STARTUP(3),(4)								
t_{STRT_BIAS}	CC	T	Bias current reference startup time(5)	—	—	0.5	4	µs
t_{PD2NM_TX}	CC	T	Transmitter startup time (power down to normal mode)(6)	—	—	0.4	2.75	µs

Table 28. LVDS pad startup and receiver electrical characteristics[1][2] (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
t_{SM2NM_TX}	CC	T	Transmitter startup time (sleep mode to normal mode)[7]	Not applicable to the MSC/DSPI LVDS pad	—	0.2	0.5	µs
t_{PD2NM_RX}	CC	T	Receiver startup time (power down to normal mode)[8]	—	—	20	40	ns
t_{PD2SM_RX}	CC	T	Receiver startup time (power down to sleep mode)[9]	Not applicable to the MSC/DSPI LVDS pad	—	20	50	ns
I_{LVDS_BIAS}	CC	T	LVDS bias current consumption	Tx or Rx enabled	—	—	0.95	mA
TRANSMISSION LINE CHARACTERISTICS (PCB Track)								
Z_0	SR	D	Transmission line characteristic impedance	—	47.5	50	52.5	Ω
Z_{DIFF}	SR	D	Transmission line differential impedance	—	95	100	105	Ω
RECEIVER								
V_{ICOM}	SR	T	Common mode voltage	—	0.15[10]	—	1.6[11]	V
$\|\Delta_{VI}\|$	SR	P	Differential input voltage[12]	—	100	—	—	mV
V_{HYS}	CC	C	Input hysteresis	—	25	—	—	mV
R_{IN}	CC	D	Terminating resistance	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%	80	125	150	Ω
		D		$V_{DD\_HV\_IO}$ = 3.3 V ± 10%	80	115	150	Ω
C_{IN}	CC	D	Differential input capacitance[13]	—	—	3.5	6.0	pF
I_{LVDS_RX}	CC	T	Receiver DC current consumption	Enabled	—	—	0.5	mA

1. The LVDS pad startup and receiver electrical characteristics in this table apply to the LFAST LVDS pad, and the MSC/DSPI LVDS pad except where noted in the conditions.
2. All LVDS pad electrical characteristics are valid from –40 °C to 150 °C.
3. All startup times are defined after a 2 peripheral bridge clock delay from writing to the corresponding enable bit in the LVDS control registers (LCR) of the LFAST and module. The value of the LCR bits for the LFAST/HSD modules don't take effect until the corresponding SIUL2 MSCR ODC bits are set to LFAST LVDS mode. Startup times for MSC/DSPI LVDS are defined after 2 peripheral bridge clock delay after selecting MSC/DSPI LVDS in the corresponding SIUL2 MSCR ODC field.
4. Startup times are valid for the maximum external loads CL defined in both the LFAST/HSD and MSC/DSPI transmitter electrical characteristic tables.
5. Bias startup time is defined as the time taken by the current reference block to reach the settling bias current after being enabled.
6. Total transmitter startup time from power down to normal mode is t_{STRT_BIAS} + t_{PD2NM_TX} + 2 peripheral bridge clock periods.
7. Total transmitter startup time from sleep mode to normal mode is t_{SM2NM_TX} + 2 peripheral bridge clock periods. Bias block remains enabled in sleep mode.
8. Total receiver startup time from power down to normal mode is t_{STRT_BIAS} + t_{PD2NM_RX} + 2 peripheral bridge clock periods.
9. Total receiver startup time from power down to sleep mode is t_{PD2SM_RX} + 2 peripheral bridge clock periods. Bias block remains enabled in sleep mode.
10. Absolute min = 0.15 V – (285 mV/2) = 0 V
11. Absolute max = 1.6 V + (285 mV/2) = 1.743 V

12. The LXRXOP[0] bit in the LFAST LVDS Control Register (LCR) must be set to one to ensure proper LFAST receive timing.
13. Total internal capacitance including receiver and termination, co-bonded GPIO pads, and package contributions.

Table 29. LFAST transmitter electrical characteristics(1)(2)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
f_{DATA}	SR	D	Data rate	—	—	—	320	Mbps
V_{OS}	CC	P	Common mode voltage	—	1.08	—	1.32	V
$\|V_{OD}\|$	CC	P	Differential output voltage swing (terminated)(3)(4)	—	110	171	285	mV
t_{TR}	CC	T	Rise/Fall time (absolute value of the differential output voltage swing)(3),(4)	—	0.26	—	1.5	ns
C_L	SR	D	External lumped differential load capacitance(3)	$V_{DD\_HV\_IO}$ = 4.5 V	—	—	9.0	pF
				$V_{DD\_HV\_IO}$ = 3.0 V	—	—	8.5	
I_{LVDS_TX}	CC	T	Transmitter DC current consumption	Enabled	—	—	3.2	mA

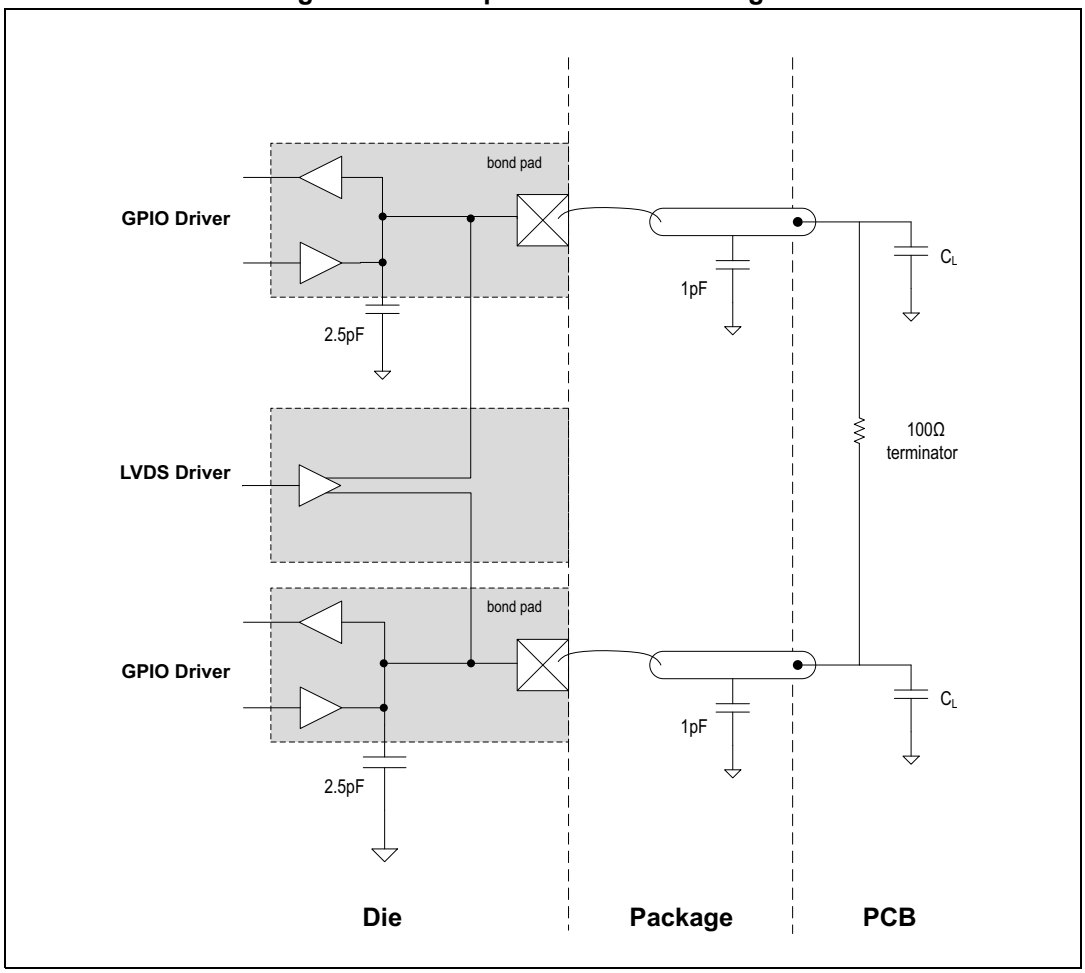
1. The LFAST pad electrical characteristics are based on worst case internal capacitance values shown in *Figure 17*.
2. All LFAST LVDS pad electrical characteristics are valid from –40 °C to 150 °C.
3. Valid for maximum data rate f_{DATA}. Value given is the capacitance on each terminal of the differential pair, as shown in *Figure 17*.
4. Valid for maximum external load C_L.

Table 30. MSC/DSPI LVDS transmitter electrical characteristics (1)(2)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
Data Rate								
f_{DATA}	SR	D	Data rate	—	—	—	80	Mbps
V_{OS}	CC	P	Common mode voltage	—	1.08	—	1.32	V
$\|V_{OD}\|$	CC	P	Differential output voltage swing (terminated)(3)(4)	—	150	214	400	mV
t_{TR}	CC	T	Rise/Fall time (absolute value of the differential output voltage swing)(3),(4)	—	0.8	—	4.0	ns
C_L	SR	D	External lumped differential load capacitance(3)	$V_{DD\_HV\_IO}$ = 4.5 V	—	—	41	pF
				$V_{DD\_HV\_IO}$ = 3.0 V	—	—	39	
I_{LVDS_TX}	CC	T	Transmitter DC current consumption	Enabled	—	—	4.0	mA

1. The MSC and DSPI LVDS pad electrical characteristics are based on the application circuit and typical worst case internal capacitance values given in *Figure 17*.
2. All MSC and DSPI LVDS pad electrical characteristics are valid from –40 °C to 150 °C.
3. Valid for maximum data rate f_{DATA}. Value given is the capacitance on each terminal of the differential pair, as shown in *Figure 17*.
4. Valid for maximum external load C_L.

Figure 17. LVDS pad external load diagram



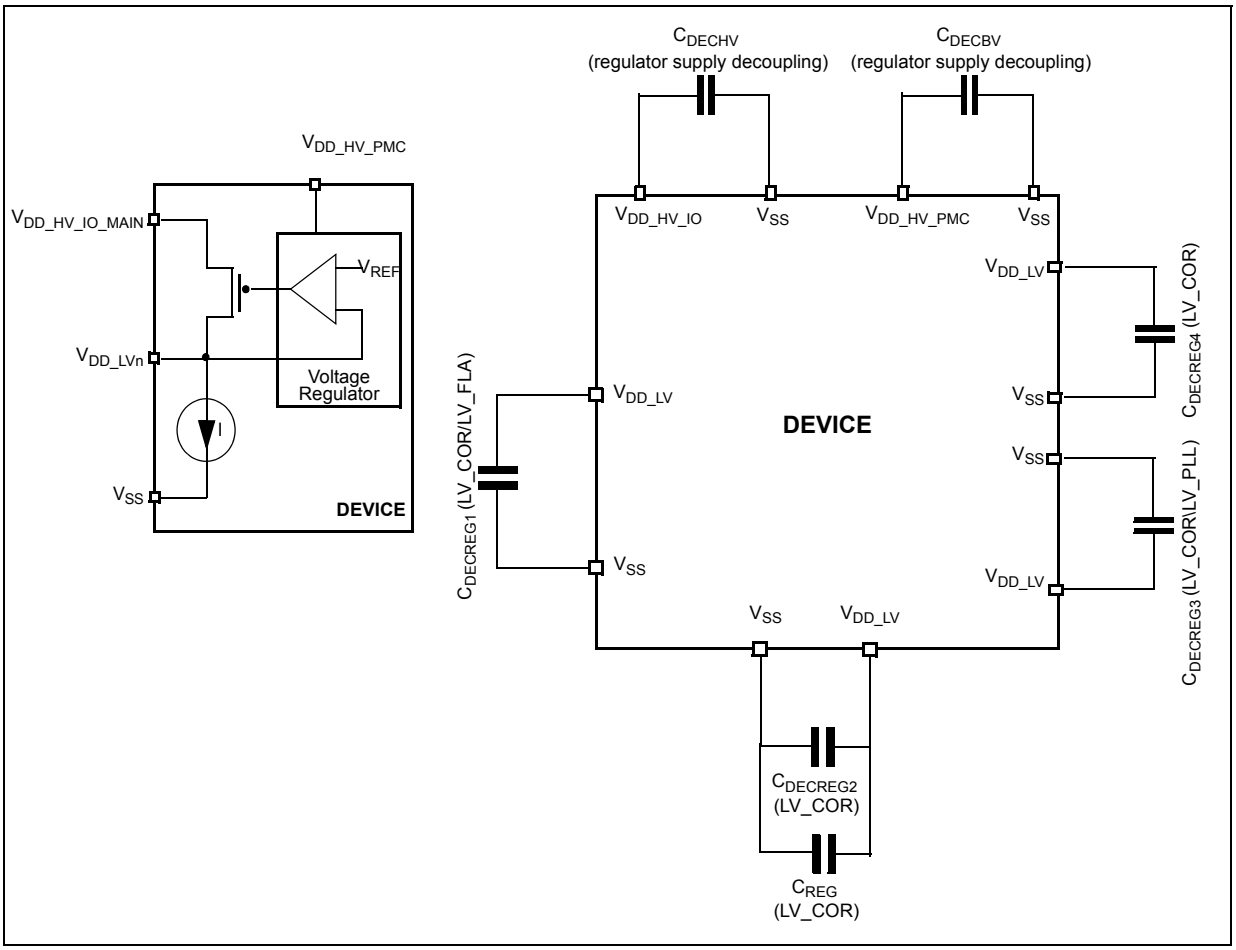
3.15 Power management: PMC, POR/LVD, sequencing

The power management module monitors the different power supplies. It also generates the internal supplies that are required for correct device functionality. The power management is supplied by the $V_{DD\_HV\_PMC}$ supply, with voltage monitors ensuring safe state operation.

3.15.1 Power management integration

Refer to the integration scheme provided below to ensure correct functionality of the device.

Figure 18. Voltage regulator capacitance connection



The internal voltage regulator requires external capacitance (C_{REGn}) to be connected to the device in order to provide a stable low voltage digital supply to the device. Capacitances should be placed on the board as near as possible to the associated pins. Care should also be taken to limit the serial inductance of the board to less than 5 nH.

A decoupling capacitor must be placed between each V_{DD_LV} supply pin and V_{SS} ground plane to ensure stable voltage. The capacitor should be placed as near as possible to the V_{DD_LV} supply pin.

3.15.2 Main voltage regulator electrical characteristics

The device implements an internal voltage regulator to generate the low voltage core supply V_{DD_LV} from the high voltage ballast supply $V_{DD\_BV\_PMC}$. The regulator itself is supplied by $V_{DD\_HV\_PMC}$.

Note: Both HV supplies, $V_{DD\_HV\_PMC}$ and $V_{DD\_BV\_PMC}$, are shorted with $V_{DD\_HV\_IO}$ supply at package level.

The following supplies are involved:

- HV—High voltage external power supply for voltage regulator module. It is shorted with $V_{DD\_HV\_IO}$.
- BV—High voltage external power supply for internal ballast module. It is shorted with $V_{DD\_HV\_IO}$.
- LV—Low voltage internal power supply for core, PLL and flash digital logic. This is generated by the internal voltage regulator but provided outside to connect stability capacitor. It is split into three further domains to ensure noise isolation between critical LV modules within the device:
  - LV_COR—Low voltage supply for the core. It is also used to provide supply for PLL through double bonding.
  - LV_FLA—Low voltage supply for code flash module. It is supplied with dedicated ballast and shorted to LV_COR through double bonding.
  - LV_PLL—Low voltage supply for PLL. It is shorted to LV_COR through double bonding.

Table 31. Voltage regulator electrical characteristics

Symbol		Parameter	Conditions[1]	Value[2]			Unit
				Min	Typ	Max	
C_{REG}	SR	Internal voltage regulator stability external capacitance	—	1.1	2.2[3]	2.97	µF
R_{REG}	SR	Stability capacitor equivalent serial resistance	Total resistance including board track	1	—	50	mΩ
$C_{DECREGn}$	SR	Internal voltage regulator decoupling external capacitance	—	50	100	135	nF
$R_{DECREGn}$	SR	Stability capacitor equivalent serial resistance	—	1	—	50	mΩ
C_{DECBV}	SR	Decoupling capacitance[4] ballast	$V_{DD\_HV\_IO\_MAIN}/V_{SS}$ pair	—	4[3]	—	µF
C_{DECHV}	SR	Decoupling capacitance regulator supply	$V_{DD\_HV\_IO\_MAIN}/V_{SS}$ pair	10	100	—	nF
C_{DECFLA}	SR	Decoupling capacitance for flash supply	$V_{DD\_HV\_FLA}/V_{SS}$ pair	65	100	—	nF
	D						
V_{MREG}	CC	Main regulator output voltage	Before trimming	1.19	1.26	1.33[5]	V
	CC		After trimming	1.16	1.28	1.32[6]	
IDD_{MREG}	SR	Main regulator current provided to V_{DD_LV} domain	—	—	—	125	mA
ΔIDD_{MREG}	SR	Main regulator current variation	20 µs observation window	–60	—	60	mA
$I_{MREGINT}$[7]	D	Main regulator current consumption	—	—	1.5	3.0	mA

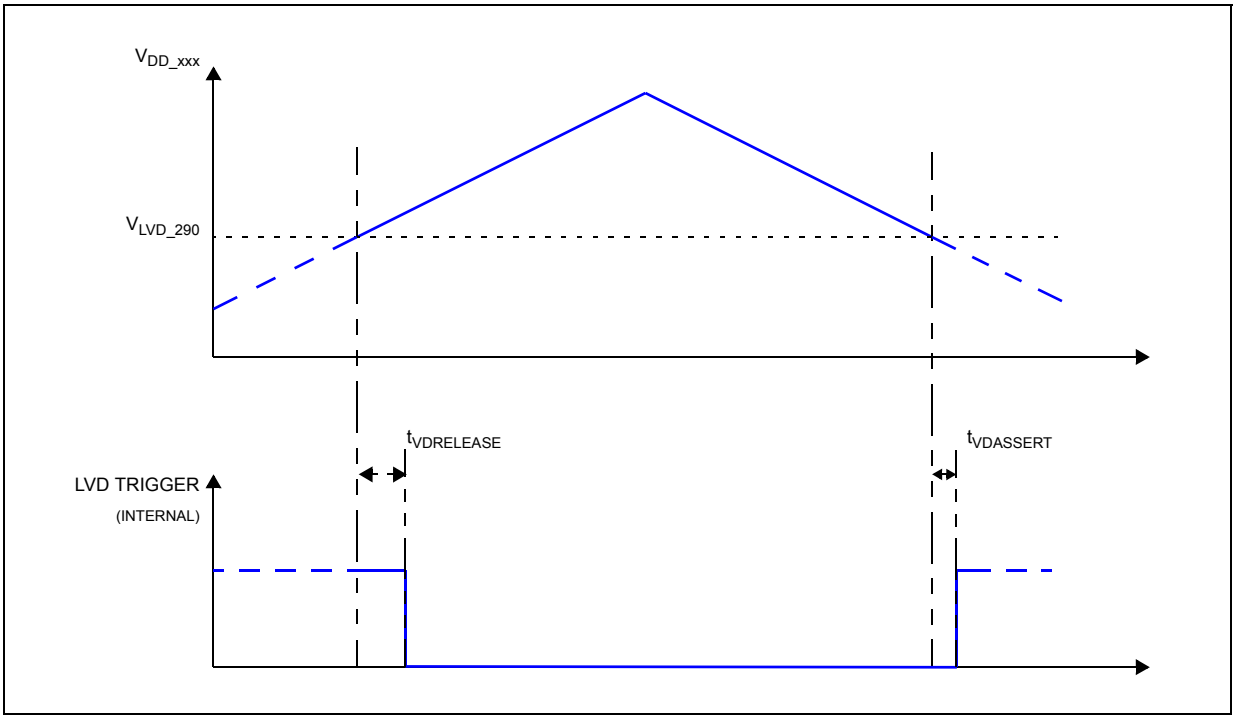
1. V_{DD} = 5.0 V ± 10%, T_A = –40 / 125 °C, unless otherwise specified.
2. All values need to be confirmed during device validation.
3. Recommended X7R or X5R ceramic –50% / +35% variation across process, temperature, voltage and after aging.
4. This capacitance value is driven by the constraints of the external voltage regulator supplying the V_{DD_BV} voltage. A typical value is in the range of 470 nF.
5. At power-up condition before trimming at 27 °C, no load.

6. Across the whole process, voltage and temperature range with full load.
7. By simulation.

3.15.3 Device voltage monitoring

Voltage monitoring thresholds are shown in the following figure.

Figure 19. Voltage monitor threshold definition



The LVDs for the device and their levels are given in the following table.

Table 32. Voltage monitor electrical characteristics(1)

Symbol		C	Parameter	Conditions	Value(2)			Unit
					Min	Typ	Max	
V_{LVD270_C}	CC	P	HV supply low voltage monitoring	Pre-trimming	2610	2760	2910	mV
				Trimmed(3)	2710	2760	2800	mV
$V_{LVD290\_C/IJ/F/IF}$	CC	P	HV supply low voltage monitoring	Pre-trimming	2660	2820	2980	mV
				Trimmed(3)	2890	2940	2990	mV
$V_{LVD400\_A/IM}$	CC	P	HV supply low voltage monitoring	Untrimmed(3)	3990	4230	4470	mV
				Trimmed(3)	4150	4230	4310	mV
V_{LVD108}	CC	P	Core LV internal supply low voltage monitoring	—	1080	—	1170	mV

Table 32. Voltage monitor electrical characteristics[1] (continued)

Symbol		C	Parameter	Conditions	Value[2]			Unit
					Min	Typ	Max	
$t_{VDASSERT}$	CC	D	Voltage detector threshold crossing assertion	—	0.1	—	2	µs
$t_{VDRELEASE}$	CC	D	Voltage detector threshold crossing de-assertion	—	5	—	20	µs

1. For V_{DD_LV} levels, a maximum of 30 mV IR drop is incurred from the pin to all sinks on the die. For other LVD, the IR drop is estimated by the multiplying the supply current by 0.5 Ω.
2. The threshold for all PORs and LVDs are defined when the output transits to 1, i.e., when the sense goes above the reference.
3. Across process, temperature and voltage range.

3.15.4 Power up/down sequencing

The following table shows the constraints and relationships for the different power supplies.

Table 33. Device supply relation during power-up/power-down sequence

		Supply 2[1]				
		V_{DD_LV}	$V_{DD\_HV\_IO}$	$V_{DD\_HV\_ADV}$	$V_{DD\_HV\_ADR}$	ALTREF[2]
Supply 1[1]	V_{DD_LV}					
	$V_{DD\_HV\_IO}$					
	$V_{DD\_HV\_ADV}$					
	$V_{DD\_HV\_ADR}$			5 mA		
	ALTREF		10 mA[3]	10 mA[3]		

1. Grey cells: Supply 1 (row) can exceed Supply 2 (column), granted that external circuitry ensures current flowing from supply1 is less than absolute maximum rating current value provided.
2. ALTREF are the alternate references for the ADC that can be used in place of the default reference ($V_{DD\_HV\_ADR\_*}$). It is the SARB.ALTREF.
3. ADC performance is not guaranteed with ALTREFn above $V_{DD\_HV\_IO}$/$V_{DD\_HV\_ADV}$.

During power-up, all functional terminals are maintained into a known state as described in the following table.

Table 34. Functional terminals state during power-up and reset

TERMINAL[1]	POWER-UP[2] pad state	RESET pad state	Default pad state[3]	Comments
PORST	Strong pull-down[4]	Weak pull-down	Weak pull-down	Power-on reset pad
ESR0[5]	Strong pull-down	Strong pull-down	Weak pull-up	Functional reset pad

Table 34. Functional terminals state during power-up and reset (continued)

TERMINAL(1)	POWER-UP(2) pad state	RESET pad state	Default pad state(3)	Comments
ESR1	High impedance	Weak pull-down	Weak pull-down	—
TEST_MODE	Weak pull-down	Weak pull-down(6)	Weak pull-down(6)	—
GPIO	Weak pull-up(4)	Weak pull-up	Weak pull-up	—
ANALOG	High impedance	High impedance	High impedance	—
ERROR	High impedance	High impedance	High impedance	—
TRST	High impedance	Weak pull-down	Weak pull-down	—
TCK	High impedance	Weak pull-down	Weak pull-down	—
TMS	High impedance	Weak pull-up	Weak pull-up	—
TDI	High impedance	Weak pull-up	Weak pull-up	—
TDO	High impedance	High impedance	High impedance	—

1. Refer to pinout information for terminal type.
2. POWER-UP state is guaranteed from $V_{DD\_HV\_IO}$ > 1.1 V and maintained until supply crosses the power-on reset threshold: V_{PORUP_LV} for LV supply, V_{PORUP_HV} for high voltage supply.
3. Before software configuration.
4. Pull-down and pull-up strength are provided as part of *Section 3.8.2, I/O output DC characteristics*.
5. As opposed to ESR0, ESR1 is provided via normal GPIO and implements weak pull-up during power-up.
6. TESTMODE pull-down is implemented to prevent device to enter TESTMODE. It is recommended to connect TESTMODE pin to $V_{SS\_HV\_IO}$ on the board.

3.16 Flash memory electrical characteristics

The flash array access time for reads is affected by the number of wait-states added to the minimum time, which is one cycle.

Wait states are set in the RWSC field of the Platform Flash Configuration Register 1 (PFCR1) to a value corresponding to the operating frequency of the flash memory controller and the actual read access time of the flash memory controller. Higher operating frequencies require non-zero settings for this field for proper flash operation.

Shown below are the maximum operating frequencies (f_{sys}) for legal RWSC settings based on specified access times at 150 °C:

Table 35. RWSC settings

Flash operating frequency range (MHz)	RWSC
00 MHz < f_{sys} < 20 MHz	0
20 MHz < f_{sys} < 40 MHz	1
40 MHz < f_{sys} < 60 MHz	2
60 MHz < f_{sys} < 80 MHz	3

Table 36 shows the estimated Program/Erase characteristics.

Table 36. Flash memory program and erase specifications (pending silicon characterization) (1)

Symbol	Characteristics(2)	Value									Unit
		Typ(3)	C	Initial max			Typical end of life(4)	Lifetime max(5)		C	
				25 °C(6)	All temp (7)	C		< 1 K cycles	≤ 100 K cycles		
$t_{dwprogram}$	Double Word (64 bits) program time [Packaged part]	38	C	150	—	—	94	500		C	µs
$t_{pprogram}$	Page (256 bits) program time	78	C	300	—	—	214	1000		C	µs
$t_{pprogrameep}$	Page (256 bits) program time EEPROM (partition 2) [Packaged part]	90	C	330	—	—	250	1000		C	µs
$t_{qprogram}$	Quad Page (1024 bits) program time	274	C	1000	1500	—	802	2000		C	µs
$t_{qprogrameep}$	Quad Page (1024 bits) program time EEPROM (partition 2) [Packaged part]	315	C	1100	1650	P	925	2000		C	µs
$t_{256kpperase}$	256 KB block pre-program and erase time	1800	C	2400	3400	P	1980	15000	—	C	ms
$t_{256kprogram}$	256 KB block program time	584	C	760	1140	P	650	17000	—	C	ms
$t_{16kprogrameep}$	Program 16 KB EEPROM (partition 1)	37	C	48	72	P	69	1000		C	ms
$t_{16keraseeep}$	Erase 16 KB EEPROM (partition 1)	350	C	1200	1200	P	600	5000		C	ms
t_{tr}	Program rate(8)	2.34	C	3.04	4.56	C	2.60	—		C	s/MB
t_{pr}	Erase rate(8)	7.2	C	14.4	28.8	C	7.92	—		C	s/MB
$t_{ffprogram}$	Full flash programming time(9)	4	C	16	24	P	5	26	—	C	s
$t_{fferase}$	Full flash erasing time(9)	12	C	24	30	P	15	40	—	C	s
t_{ESRT}	Erase suspend request rate(10)	5.5	T	—	—	—	—	—		T	ms
t_{PSRT}	Program suspend request rate(10)	20	T	—	—	—	—	—		T	µs
t_{PSUS}	Program suspend latency(11)	—	—	—	—	—	—	15		T	µs
t_{ESUS}	Erase suspend latency(11)	—	—	—	—	—	—	30		T	µs
t_{AIC0S}	Array Integrity Check Partition 0 (1.5 MB, sequential)(12)	20	T	—	—	—	—	—	—	—	ms
t_{AIC0P}	Array Integrity Check Partition 0 (1.5 MB, proprietary)(12)	3.35	T	—	—	—	—	—	—	—	s
t_{MR0S}	Margin Read Partition 0 (1.5 MB, sequential)	100	T	—	—	—	—	—	—	—	ms
t_{MR0P}	Margin Read Partition 0 (1.5 MB, proprietary)	16.7	T	—	—	—	—	—	—	—	s

1. Characteristics are valid both for DATA Flash and CODE Flash, unless specified in the characteristics column.

2. Actual hardware programming times; this does not include software overhead.
3. Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.
4. Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations. These values are characteristic, but not tested.
5. Lifetime maximum program & erase times apply across the voltages and temperatures and occur after the specified number of program/erase cycles. These maximum values are characterized but not tested or guaranteed.
6. Initial factory condition: < 100 program/erase cycles, 20 °C < T_J < 30 °C junction temperature, and nominal (± 2%) supply voltages. These values are verified at production testing.
7. Initial maximum “All temp” program and erase times provide guidance for time-out limits used in the factory and apply for less than or equal to 100 program or erase cycles, –40 °C < T_J < 150 °C junction temperature, and nominal (± 2%) supply voltages. These values are verified at production testing.
8. Rate computed based on 256K sectors.
9. Only code sectors, not including EEPROM.
10. Time between erase suspend resume and next erase suspend.
11. Timings guaranteed by design.
12. AIC is done using system clock, thus all timing is dependant on system frequency and number of wait states. Timing in the table is calculated at 160 MHz.

Table 37. Flash memory module extended life specification(1)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
P/E_{16}	CC	C	Number of program/erase cycles per block for 16 KB EEPROM emulation (2)	—	100,000	—	—	P/E cycles
P/E_{256}	CC	C	Number of program/erase cycles per block for 256 KB blocks(2)	—	1000	100,000	—	P/E cycles
Data retention	CC	C	Minimum data retention	Blocks with 0 – 10000 P/E cycles	20	—	—	years
				Blocks with 10001– 250000 P/E cycles. Data Retention limited to 2, in total, 16 KB sectors within module 1	10	—	—	

1. All stated module life data are preliminary targets, and subject to change pending silicon characterization.
2. Program and Erase supported for standard operating temperature range.

3.17 AC specifications

3.17.1 Debug and calibration interface timing

3.17.1.1 JTAG interface timing

Table 38. JTAG pin AC electrical characteristics (1)(2)

#	Symbol		C	Characteristic	Value		Unit
					Min	Max	
1	t_{JCYC}	CC	D	TCK cycle time	100	—	ns
2	t_{JDC}	CC	T	TCK clock pulse width	40	60	%
3	$t_{TCKRISE}$	CC	D	TCK rise and fall times (40%–70%)	—	3	ns
4	t_{TMSS}, t_{TDIS}	CC	D	TMS, TDI data setup time	5	—	ns
5	t_{TMSH}, t_{TDIH}	CC	D	TMS, TDI data hold time	5	—	ns
6	t_{TDOV}	CC	D	TCK low to TDO data valid	—	16(3)	ns
7	t_{TDOI}	CC	D	TCK low to TDO data invalid	0	—	ns
8	t_{TDOHZ}	CC	D	TCK low to TDO high impedance	—	15	ns
9	t_{JCMPPW}	CC	D	JCOMP assertion time	100	—	ns
10	t_{JCMPS}	CC	D	JCOMP setup time to TCK low	40	—	ns
11	t_{BSDV}	CC	D	TCK falling edge to output valid	—	600(4)	ns
12	t_{BSDVZ}	CC	D	TCK falling edge to output valid out of high impedance	—	600	ns
13	t_{BSDHZ}	CC	D	TCK falling edge to output high impedance	—	600	ns
14	t_{BSDST}	CC	D	Boundary scan input valid to TCK rising edge	15	—	ns
15	t_{BSDHT}	CC	D	TCK rising edge to boundary scan input invalid	15	—	ns

1. These specifications apply to JTAG boundary scan only. See *Table 39* for functional specifications.
2. JTAG timing specified at $V_{DD\_HV\_IO\_JTAG}$ = 4.0 V to 5.5 V, and maximum loading per pad type as specified in the I/O section of the datasheet.
3. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.
4. Applies to all pins, limited by pad slew rate. Refer to IO delay and transition specification and add 20 ns for JTAG delay.

Figure 20. JTAG test clock input timing

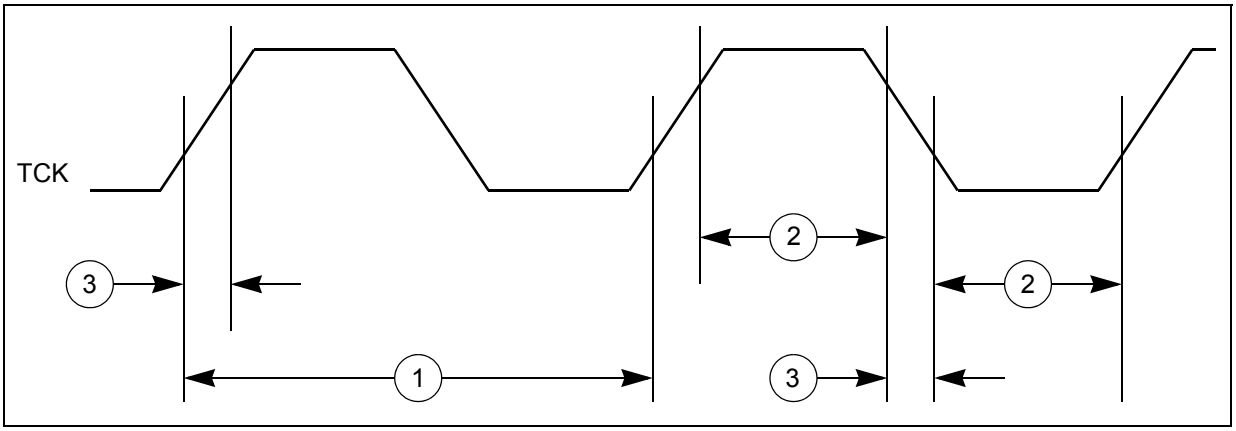


Figure 21. JTAG test access port timing

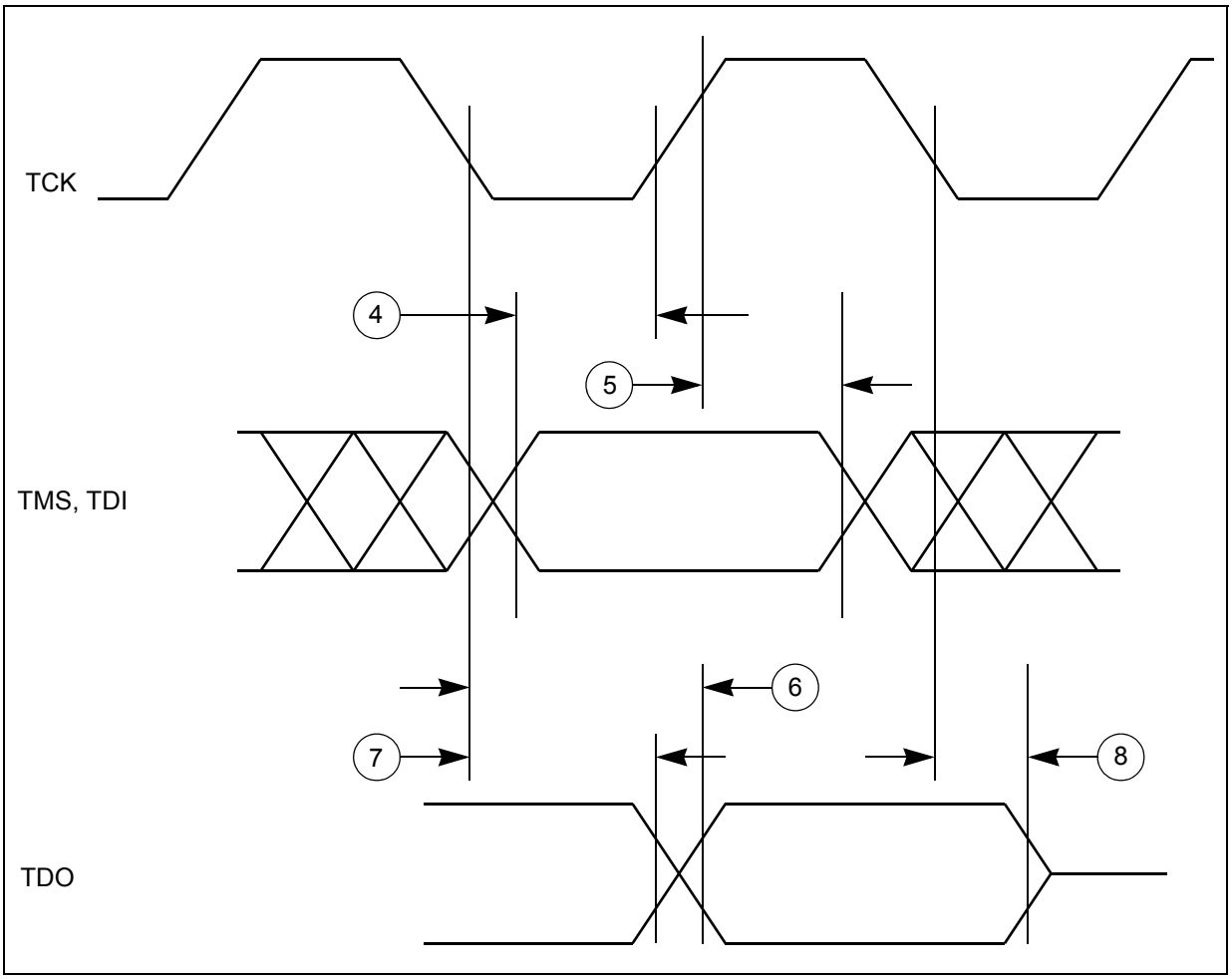


Figure 22. JTAG JCOMP timing

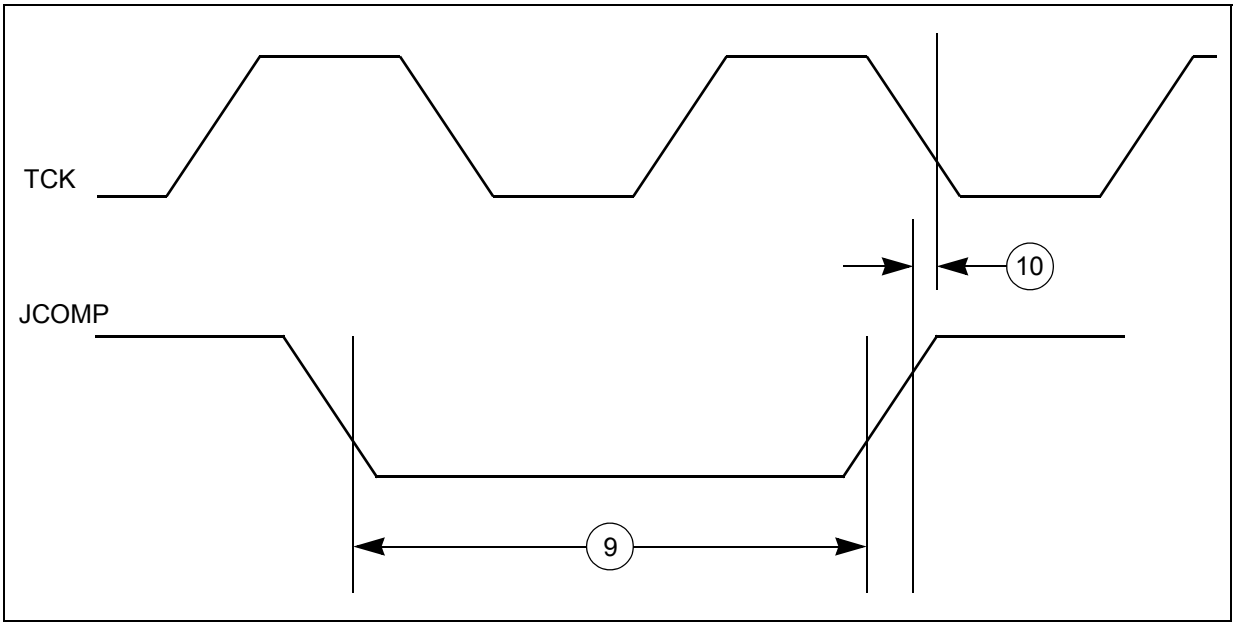
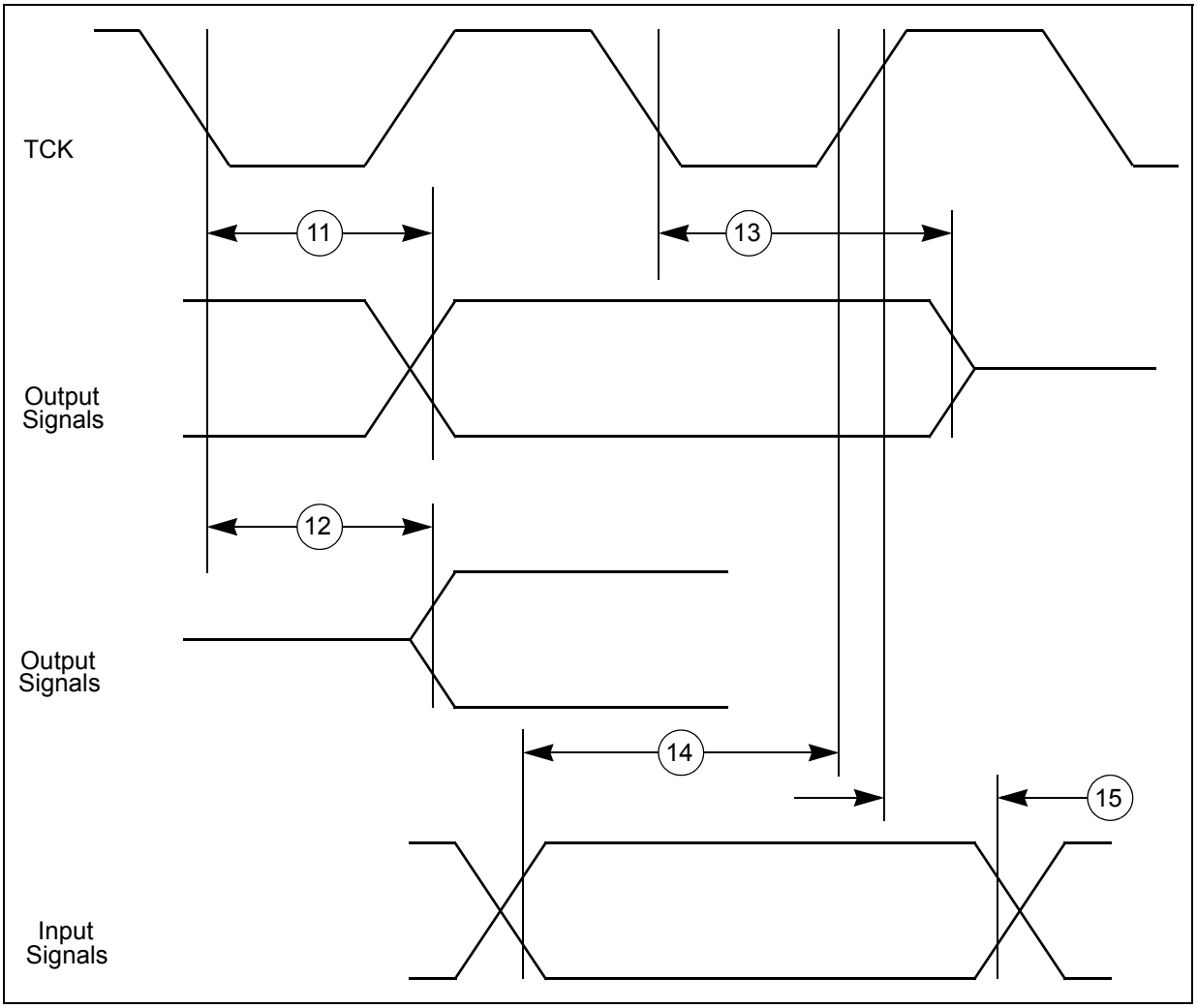


Figure 23. JTAG boundary scan timing



3.17.1.2 Nexus interface timing

Table 39. Nexus debug port timing[1]

#	Symbol		C	Characteristic	Value		Unit
					Min	Max	
7	t_{EVTIPW}	CC	D	$\overline{EVTI}$ pulse width	4	—	t_{CYC}[2]
8	t_{EVTOPW}	CC	D	$\overline{EVTO}$ pulse width	40	—	ns
9	t_{TCYC}	CC	D	TCK cycle time	2[3],[4]	—	t_{CYC}[2]
9	t_{TCYC}	CC	D	Absolute minimum TCK cycle time[5] (TDO/TDOC sampled on posedge of TCK)	40[6]	—	ns
				Absolute minimum TCK cycle time[7] (TDO/TDOC sampled on negedge of TCK)	20[6]	—	
11[8]	t_{NTDIS}	CC	D	TDI/TDIC data setup time	5	—	ns

Table 39. Nexus debug port timing[1] (continued)

#	Symbol		C	Characteristic	Value		Unit
					Min	Max	
12	t_{NTDIH}	CC	D	TDI/TDIC data hold time	5	—	ns
13[9]	t_{NTMSS}	CC	D	TMS/TMSC data setup time	5	—	ns
14	t_{NTMSH}	CC	D	TMS/TMSC data hold time	5	—	ns
15[10]	—	CC	D	TDO/TDOC propagation delay from falling edge of TCK[11]	—	16	ns
16	—	CC	D	TDO/TDOC hold time with respect to TCK falling edge (minimum TDO/TDOC propagation delay)	2.25	—	ns

1. Nexus timing specified at $V_{DD\_HV\_IO\_JTAG}$ = 4.0 V to 5.5 V, and maximum loading per pad type as specified in the I/O section of the datasheet.
2. t_{CYC} is system clock period.
3. Achieving the absolute minimum TCK cycle time may require a maximum clock speed (system frequency / 8) that is less than the maximum functional capability of the design (system frequency / 4) depending on the actual peripheral frequency being used. To ensure proper operation TCK frequency should be set to the peripheral frequency divided by a number greater than or equal to that specified here.
4. This is a functionally allowable feature. However, it may be limited by the maximum frequency specified by the Absolute minimum TCK period specification.
5. This value is TDO/TDOC propagation time 36 ns + 4 ns setup time to sampling edge.
6. This may require a maximum clock speed (system frequency / 8) that is less than the maximum functional capability of the design (system frequency / 4) depending on the actual system frequency being used.
7. This value is TDO/TDOC propagation time 16 ns + 4 ns setup time to sampling edge.
8. TDIC represents the TDI bit frame of the scan packet in compact JTAG 2-wire mode.
9. TMSC represents the TMS bit frame of the scan packet in compact JTAG 2-wire mode.
10. TDOC represents the TDO bit frame of the scan packet in compact JTAG 2-wire mode.
11. Timing includes TCK pad delay, clock tree delay, logic delay and TDO/TDOC output pad delay.

Figure 24. Nexus event trigger and test clock timings

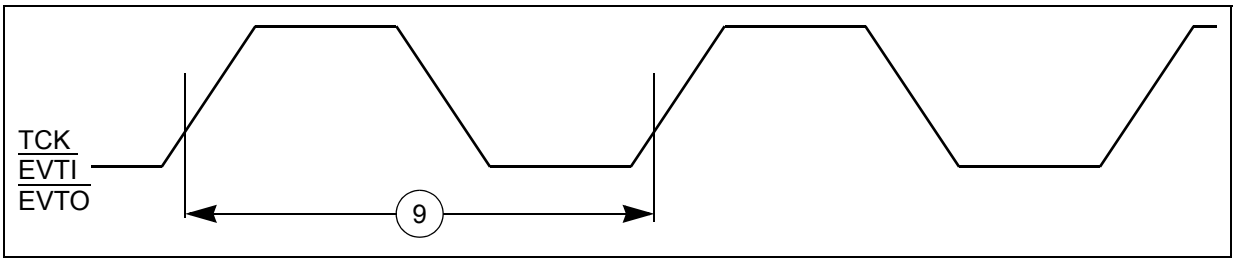
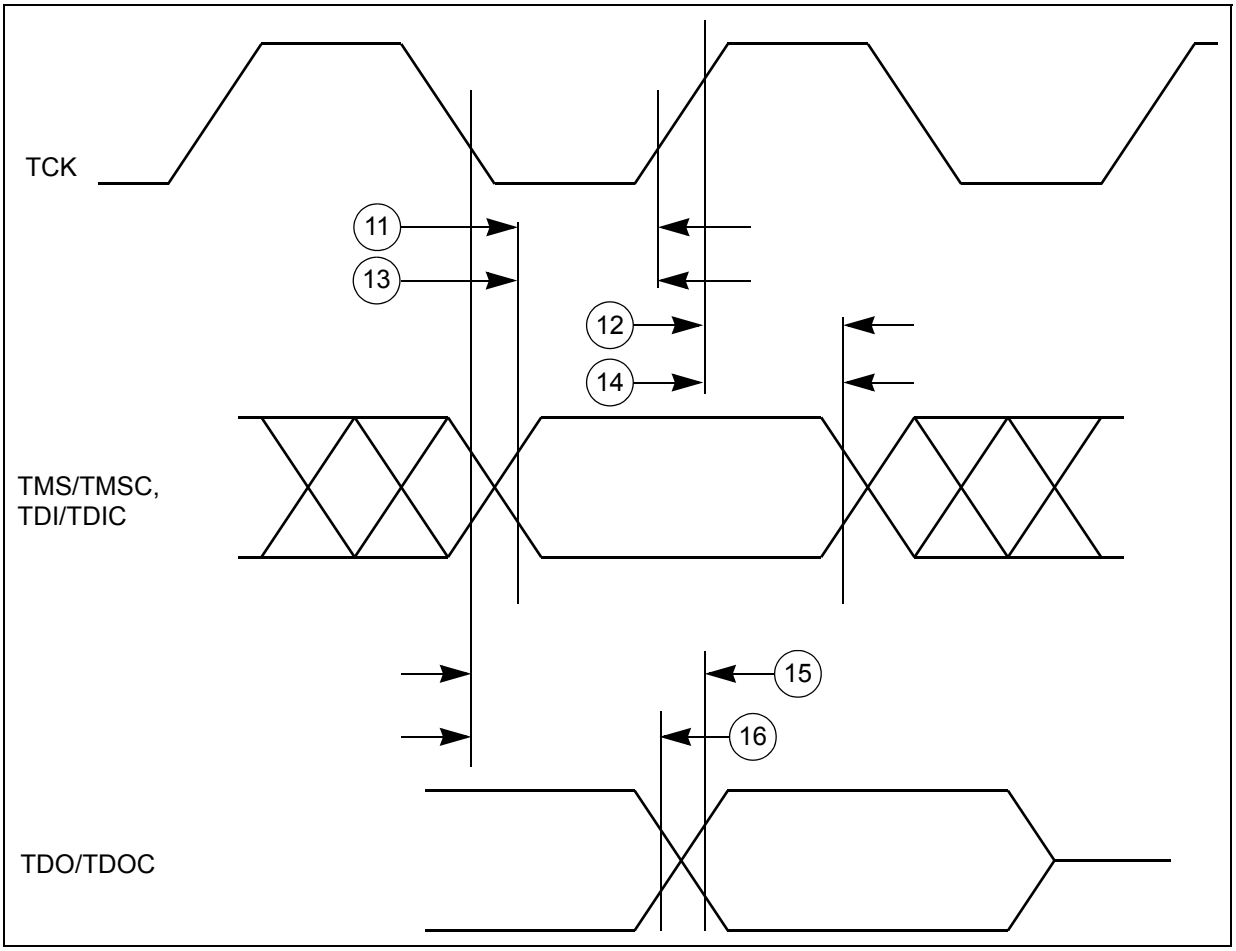


Figure 25. Nexus TDI/TDIC, TMS/TMSC, TDO/TDOC timing



3.17.2 DSPI timing with CMOS and LVDS[a] pads

DSPI channel frequency support is shown in *Table 40*. Timing specifications are shown in *Table 41*, *Table 42* and *Table 43*.

Table 40. DSPI channel frequency support

DSPI use mode		Max usable frequency (MHz)[1],[2]
CMOS (Master mode)	Full duplex – Classic timing (*Table 41*)	17
	Full duplex – Modified timing (*Table 42*)	30
	Output only mode (SCK/SOUT/PCS) (*Table 41* and *Table 42*)	30
	Output only mode TSB mode (SCK/SOUT/PCS) (*Table 44*)	30
LVDS (Master mode)	Output only mode TSB mode (SCK/SOUT/PCS) (*Table 43*)	40

1. Maximum usable frequency can be achieved if used with fastest configuration of the highest drive pads.

a. DSPI in TSB mode with LVDS pads can be used to implement Micro Second Channel bus protocol.

2. Maximum usable frequency does not take into account external device propagation delay.

3.17.2.1 DSPI master mode full duplex timing with CMOS and LVDS pads

3.17.2.1.1 DSPI CMOS Master Mode – Classic Timing

Table 41. DSPI CMOS master classic timing (full duplex and output only) – MTFE = 0, CPHA = 0 or 1[1]

#	Symbol		C	Characteristic	Condition		Value[2]		Unit
					Pad drive[3]	Load (C_L)	Min	Max	
1	t_{SCK}	CC	D	SCK cycle time	SCK drive strength				
					Very strong	25 pF	33.0	—	ns
					Strong	50 pF	80.0	—	
					Medium	50 pF	200.0	—	
2	t_{CSC}	CC	D	PCS to SCK delay	SCK and PCS drive strength				
					Very strong	25 pF	$(N^{(4)} \times t_{SYS}^{(5)}) - 16$	—	ns
					Strong	50 pF	$(N^{(4)} \times t_{SYS}^{(5)}) - 16$	—	
					Medium	50 pF	$(N^{(4)} \times t_{SYS}^{(5)}) - 26$	—	
					PCS medium and SCK strong	PCS = 50 pF SCK = 50 pF	$(N^{(4)} \times t_{SYS}^{(5)}) - 38$	—	
3	t_{ASC}	CC	D	After SCK delay	SCK and PCS drive strength				
					Very strong	PCS = 0 pF SCK = 50 pF	$(M^{(6)} \times t_{SYS}^{(5)}) - 35$	—	ns
					Strong	PCS = 0 pF SCK = 50 pF	$(M^{(6)} \times t_{SYS}^{(5)}) - 35$	—	
					Medium	PCS = 0 pF SCK = 50 pF	$(M^{(6)} \times t_{SYS}^{(5)}) - 35$	—	
					PCS medium and SCK strong	PCS = 0 pF SCK = 50 pF	$(M^{(6)} \times t_{SYS}^{(5)}) - 35$	—	
4	t_{SDC}	CC	D	SCK duty cycle[7]	SCK drive strength				
					Very strong	0 pF	$^1/_2 t_{SCK} - 2$	$^1/_2 t_{SCK} + 2$	ns
					Strong	0 pF	$^1/_2 t_{SCK} - 2$	$^1/_2 t_{SCK} + 2$	
					Medium	0 pF	$^1/_2 t_{SCK} - 5$	$^1/_2 t_{SCK} + 5$	
PCS strobe timing									
5	t_{PCSC}	CC	D	PCSx to $\overline{\text{PCSS}}$ time[8]	PCS and PCSS drive strength				
					Strong	25 pF	12.0	—	ns
6	t_{PASC}	CC	D	$\overline{\text{PCSS}}$ to PCSx time[8]	PCS and PCSS drive strength				
					Strong	25 pF	12.0	—	ns

Table 41. DSPI CMOS master classic timing (full duplex and output only) – MTFE = 0, CPHA = 0 or 1[1] (continued)

#	Symbol		C	Characteristic	Condition		Value[2]		Unit
					Pad drive[3]	Load (C_L)	Min	Max	
SIN setup time									
7	t_{SUI}	CC	D	SIN setup time to SCK[9]	SCK drive strength				
					Very strong	25 pF	25.0	—	ns
					Strong	50 pF	31.0	—	
					Medium	50 pF	52.0	—	
SIN hold time									
8	t_{HI}	CC	D	SIN hold time from SCK[9]	SCK drive strength				
					Very strong	0 pF	–1.0	—	ns
					Strong	0 pF	–1.0	—	
					Medium	0 pF	–1.0	—	
SOUT data valid time (after SCK edge)									
9	t_{SUO}	CC	D	SOUT data valid time from SCK[10]	SOUT and SCK drive strength				
					Very strong	25 pF	—	7.0	ns
					Strong	50 pF	—	9.0	
					Medium	50 pF	—	25.0	
SOUT data hold time (after SCK edge)									
10	t_{HO}	CC	D	SOUT data hold time after SCK[10]	SOUT and SCK drive strength				
					Very strong	25 pF	–7.7	—	ns
					Strong	50 pF	–11.0	—	
					Medium	50 pF	–15.0	—	

1. All output timing is worst case and includes the mismatching of rise and fall times of the output pads.
2. All timing values for output signals in this table are measured to 50% of the output voltage.
3. Timing is guaranteed to same drive capabilities for all signals, mixing of pad drives may reduce operating speeds and may cause incorrect operation.
4. N is the number of clock cycles added to time between PCS assertion and SCK assertion and is software programmable using DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, N is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
5. t_{SYS} is the period of DSPI_CLKn clock, the input clock to the DSPI module. Maximum frequency is 80 MHz (min t_{SYS} = 10 ns).
6. M is the number of clock cycles added to time between SCK negation and PCS negation and is software programmable using DSPI_CTARx[PASC] and DSPI_CTARx[ASC]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, M is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
7. t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.
8. PCSx and PCSS using same pad configuration.
9. Input timing assumes an input slew rate of 1 ns (10% – 90%) and uses TTL / Automotive voltage thresholds.
10. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

Figure 26. DSPI CMOS master mode – classic timing, CPHA = 0

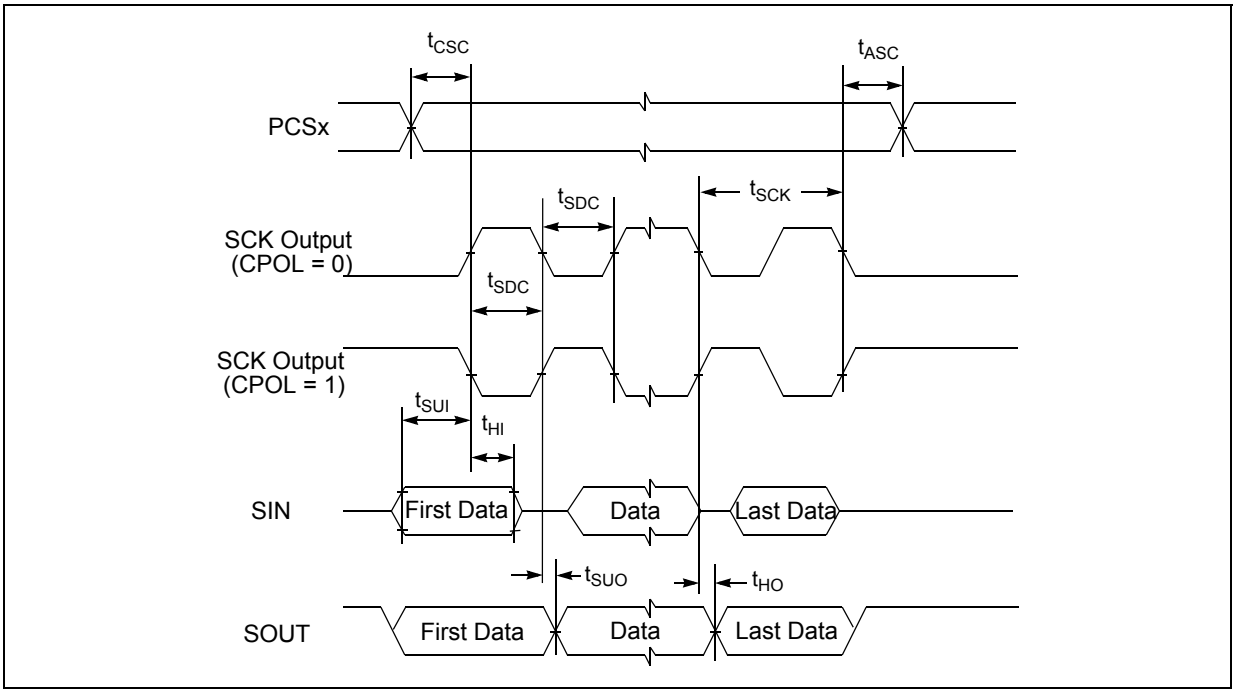


Figure 27. DSPI CMOS master mode – classic timing, CPHA = 1

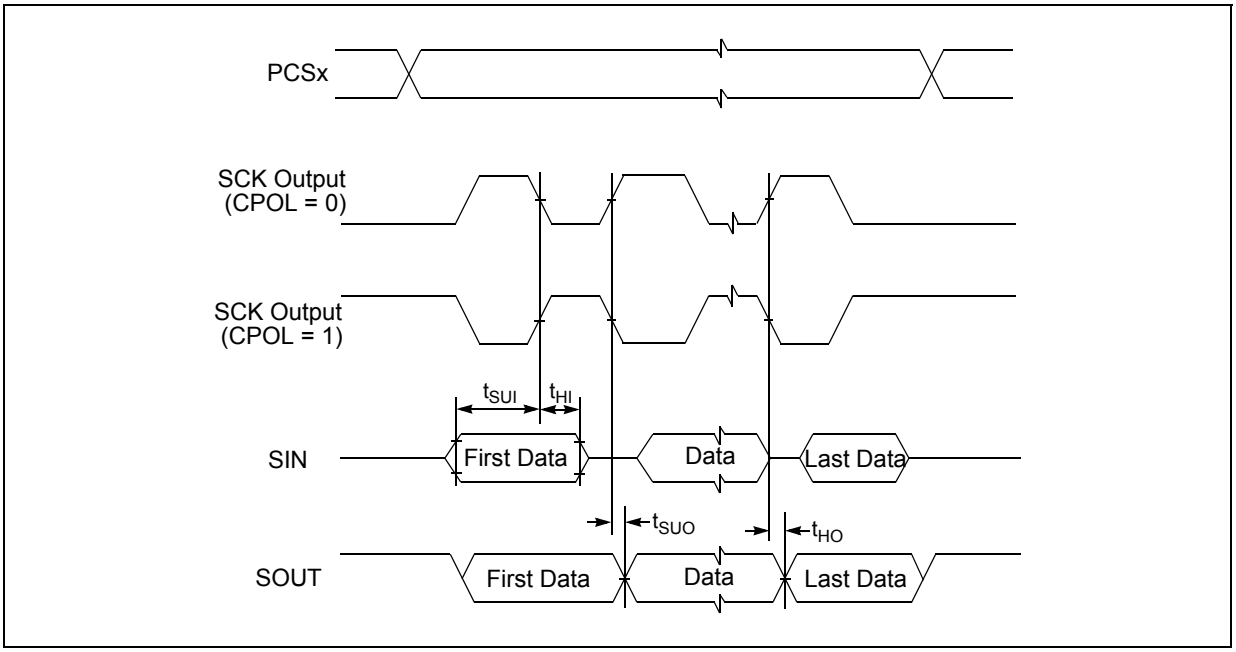
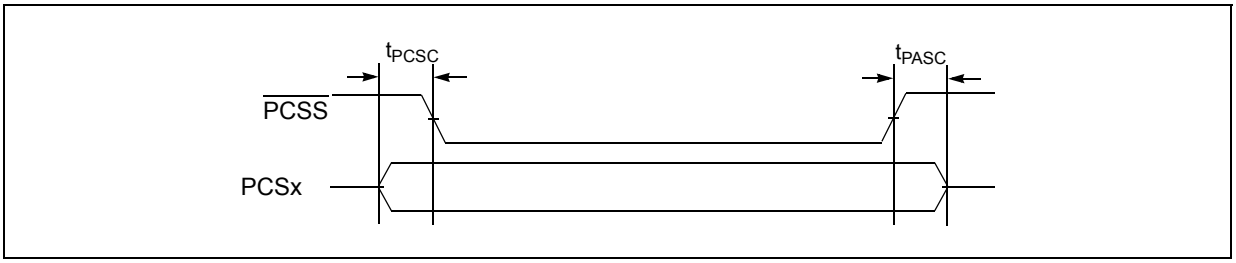


Figure 28. DSPI PCS strobe ($\overline{PCSS}$) timing (master mode)



3.17.2.1.2 DSPI CMOS Master Mode – Modified Timing

Table 42. DSPI CMOS master modified timing (full duplex and output only) – MTFE = 1, CPHA = 0 or 1(1)

#	Symbol		C	Characteristic	Condition		Value(2)		Unit
					Pad drive(3)	Load (C_L)	Min	Max	
1	t_{SCK}	CC	D	SCK cycle time	SCK drive strength				
					Very strong	25 pF	33.0	—	ns
					Strong	50 pF	80.0	—	
					Medium	50 pF	200.0	—	
2	t_{CSC}	CC	D	PCS to SCK delay	SCK and PCS drive strength				
					Very strong	25 pF	$(N^{(4)} \times t_{SYS}^{(5)}) - 16$	—	ns
					Strong	50 pF	$(N^{(4)} \times t_{SYS}^{(5)}) - 16$	—	
					Medium	50 pF	$(N^{(4)} \times t_{SYS}^{(5)}) - 26$	—	
					PCS medium and SCK strong	PCS = 50 pF SCK = 50 pF	$(N^{(4)} \times t_{SYS}^{(5)}) - 38$	—	
3	t_{ASC}	CC	D	After SCK delay	SCK and PCS drive strength				
					Very strong	PCS = 0 pF SCK = 50 pF	$(M^{(6)} \times t_{SYS}^{(5)}) - 35$	—	ns
					Strong	PCS = 0 pF SCK = 50 pF	$(M^{(6)} \times t_{SYS}^{(5)}) - 35$	—	
					Medium	PCS = 0 pF SCK = 50 pF	$(M^{(6)} \times t_{SYS}^{(5)}) - 35$	—	
					PCS medium and SCK strong	PCS = 0 pF SCK = 50 pF	$(M^{(6)} \times t_{SYS}^{(5)}) - 35$	—	
4	t_{SDC}	CC	D	SCK duty cycle(7)	SCK drive strength				
					Very strong	0 pF	$^1/_2t_{SCK} - 2$	$^1/_2t_{SCK} + 2$	ns
					Strong	0 pF	$^1/_2t_{SCK} - 2$	$^1/_2t_{SCK} + 2$	
					Medium	0 pF	$^1/_2t_{SCK} - 5$	$^1/_2t_{SCK} + 5$	
PCS strobe timing									

Table 42. DSPI CMOS master modified timing (full duplex and output only) – MTFE = 1, CPHA = 0 or 1[1] (continued)

#	Symbol		C	Characteristic	Condition		Value[2]		Unit
					Pad drive[3]	Load (C_L)	Min	Max	
5	t_{PCSC}	CC	D	PCSx to $\overline{PCSS}$ time[8]	PCS and PCSS drive strength				
					Strong	25 pF	12.0	—	ns
6	t_{PASC}	CC	D	$\overline{PCSS}$ to PCSx time[8]	PCS and PCSS drive strength				
					Strong	25 pF	12.0	—	ns
SIN setup time									
7	t_{SUI}	CC	D	SIN setup time to SCK CPHA = 0[9]	SCK drive strength				
					Very strong	25 pF	25 – ($P^{(10)}$ × $t_{SYS}^{(5)}$)	—	ns
					Strong	50 pF	31 – ($P^{(10)}$ × $t_{SYS}^{(5)}$)	—	
					Medium	50 pF	52 – ($P^{(10)}$ × $t_{SYS}^{(5)}$)	—	
				SIN setup time to SCK CPHA = 1[9]	SCK drive strength				
					Very strong	25 pF	25.0	—	ns
					Strong	50 pF	31.0	—	
					Medium	50 pF	52.0	—	
SIN hold time									
8	t_{HI}	CC	D	SIN hold time from SCK CPHA = 0[9]	SCK drive strength				
					Very strong	0 pF	– 1 + ($P^{(9)}$ × $t_{SYS}^{(4)}$)	—	ns
					Strong	0 pF	– 1 + ($P^{(9)}$ × $t_{SYS}^{(4)}$)	—	
					Medium	0 pF	– 1 + ($P^{(9)}$ × $t_{SYS}^{(4)}$)	—	
				SIN hold time from SCK CPHA = 1[9]	SCK drive strength				
					Very strong	0 pF	–1.0	—	ns
					Strong	0 pF	–1.0	—	
					Medium	0 pF	–1.0	—	
SOUT data valid time (after SCK edge)									

Table 42. DSPI CMOS master modified timing (full duplex and output only) – MTFE = 1, CPHA = 0 or 1[1] (continued)

#	Symbol		C	Characteristic	Condition		Value[2]		Unit
					Pad drive[3]	Load (C_L)	Min	Max	
9	t_{SUO}	CC	D	SOUT data valid time from SCK CPHA = 0[10]	SOUT and SCK drive strength				
					Very strong	25 pF	—	7.0 + t_{SYS}[5]	ns
					Strong	50 pF	—	9.0 + t_{SYS}[5]	
					Medium	50 pF	—	25.0 + t_{SYS}[5]	
				SOUT data valid time from SCK CPHA = 1[10]	SOUT and SCK drive strength				
					Very strong	25 pF	—	7.0	ns
					Strong	50 pF	—	9.0	
					Medium	50 pF	—	25.0	
SOUT data hold time (after SCK edge)									
10	t_{HO}	CC	D	SOUT data hold time after SCK CPHA = 0[11]	SOUT and SCK drive strength				
					Very strong	25 pF	–7.7 + t_{SYS}[5]	—	ns
					Strong	50 pF	–11.0 + t_{SYS}[5]	—	
					Medium	50 pF	–15.0 + t_{SYS}[5]	—	
				SOUT data hold time after SCK CPHA = 1[11]	SOUT and SCK drive strength				
					Very strong	25 pF	–7.7	—	ns
					Strong	50 pF	–11.0	—	
					Medium	50 pF	–15.0	—	

1. All output timing is worst case and includes the mismatching of rise and fall times of the output pads.
2. All timing values for output signals in this table are measured to 50% of the output voltage.
3. Timing is guaranteed to same drive capabilities for all signals, mixing of pad drives may reduce operating speeds and may cause incorrect operation.
4. N is the number of clock cycles added to time between PCS assertion and SCK assertion and is software programmable using DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, N is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
5. t_{SYS} is the period of DSPI_CLKn clock, the input clock to the DSPI module. Maximum frequency is 80 MHz (min t_{SYS} = 10 ns).
6. M is the number of clock cycles added to time between SCK negation and PCS negation and is software programmable using DSPI_CTARx[PASC] and DSPI_CTARx[ASC]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, M is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
7. t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.
8. PCSx and PCSS using same pad configuration.
9. Input timing assumes an input slew rate of 1 ns (10% – 90%) and uses TTL / Automotive voltage thresholds.
10. P is the number of clock cycles added to delay the DSPI input sample point and is software programmable using DSPI_MCR[SMPL_PT]. The value must be 0, 1 or 2. If the baud rate divide ratio is /2 or /3, this value is automatically set to 1.
11. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

Figure 29. DSPI CMOS master mode – modified timing, CPHA = 0

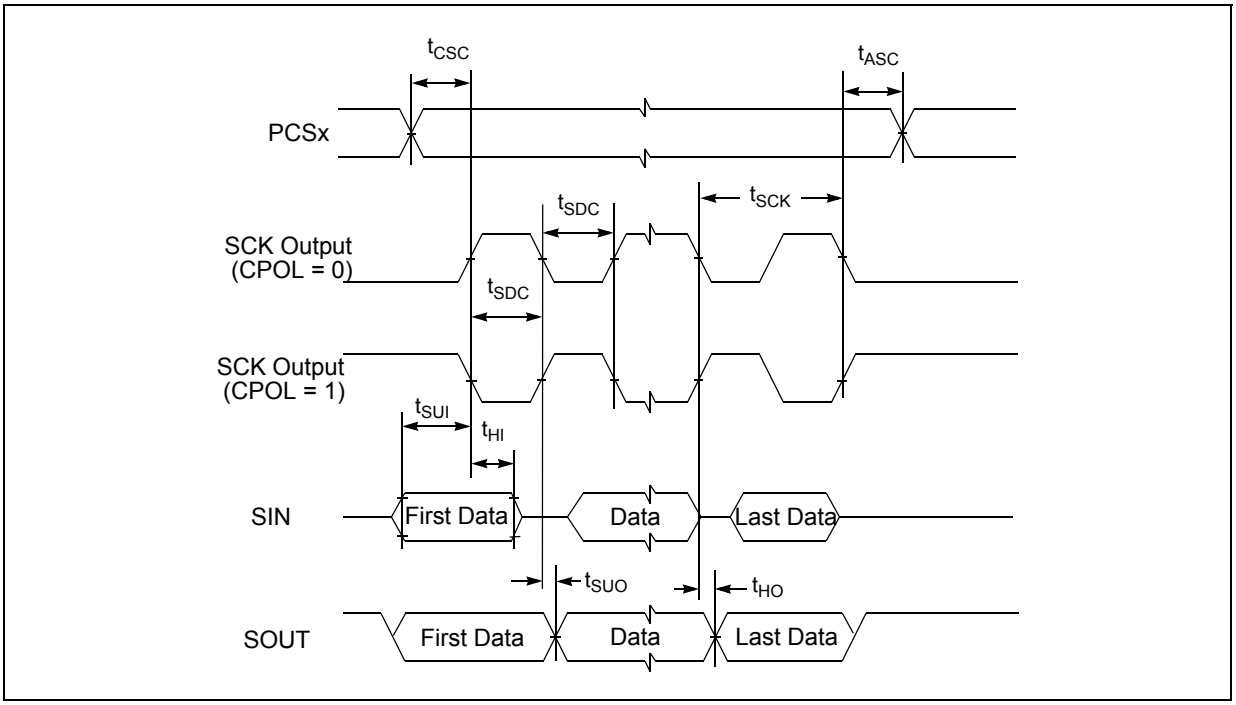


Figure 30. DSPI CMOS master mode – modified timing, CPHA = 1

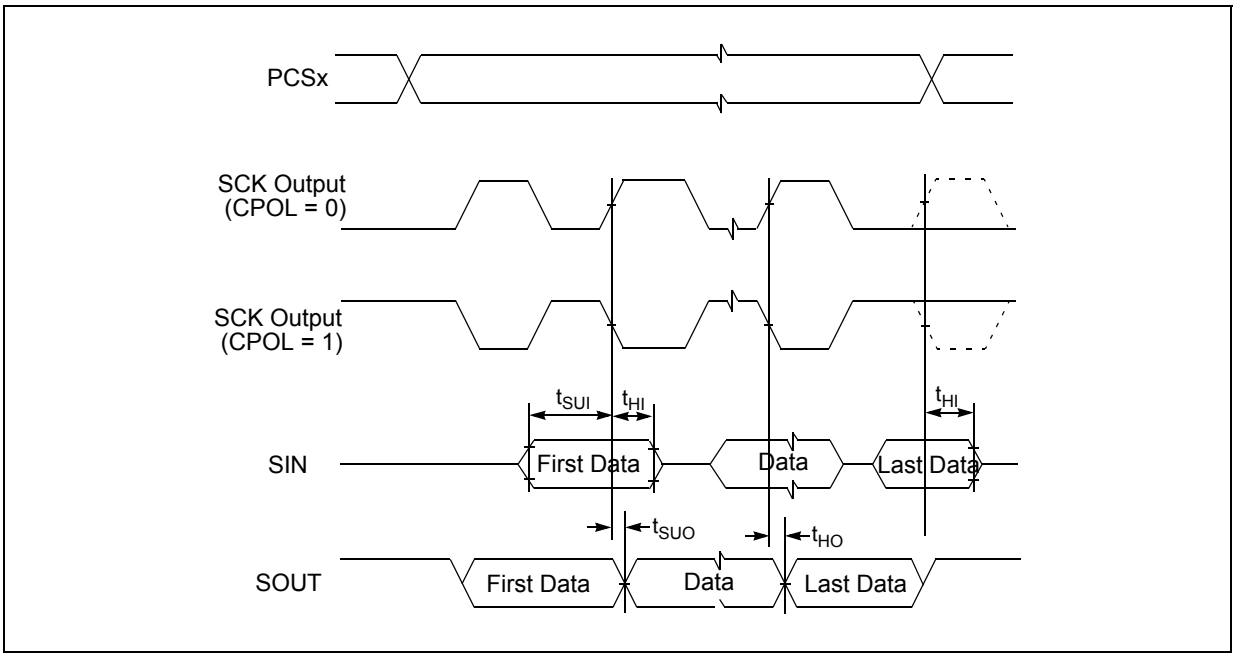
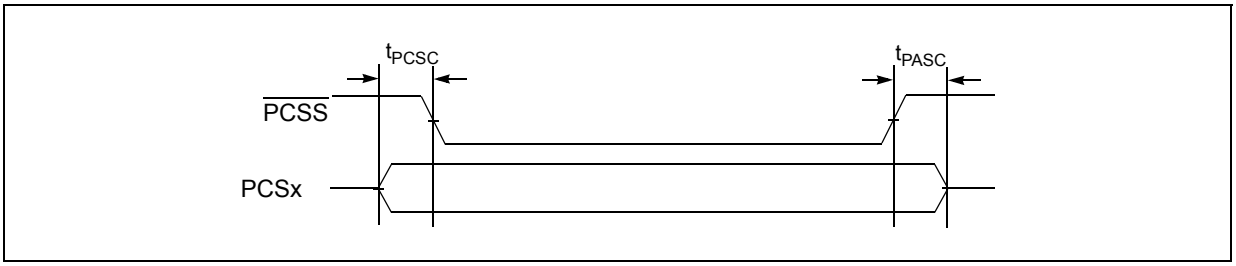


Figure 31. DSPI PCS strobe ($\overline{\text{PCSS}}$) timing (master mode)



3.17.2.1.3 DSPI Master Mode – Output Only

Table 43. DSPI LVDS master timing – output only – timed serial bus mode TSB = 1 or ITSB = 1, CPOL = 0 or 1, continuous SCK clock(1)(2)

#	Symbol		C	Characteristic	Condition		Value		Unit
					Pad drive	Load	Min	Max	
1	t_{SCK}	CC	D	SCK cycle time	LVDS	15 pF to 50 pF differential	25.0	—	ns
2	t_{CSV}	CC	D	PCS valid after SCK(3) (SCK with 50 pF differential load cap.)	Very strong	25 pF	—	6.0	ns
					Strong	50 pF	—	10.5	ns
3	t_{CSH}	CC	D	PCS hold after SCK(3) (SCK with 50 pF differential load cap.)	Very strong	0 pF	–4.0	—	ns
					Strong	0 pF	–4.0	—	ns
4	t_{SDC}	CC	D	SCK duty cycle (SCK with 50 pF differential load cap.)	LVDS	15 pF to 50 pF differential	$^1/_2t_{SCK} - 2$	$^1/_2t_{SCK} + 2$	ns
SOUT data valid time (after SCK edge)									
5	t_{SUO}	CC	D	SOUT data valid time from SCK(4)	SOUT and SCK drive strength				
					LVDS	15 pF to 50 pF differential	—	8.0	ns
SOUT data hold time (after SCK edge)									
6	t_{HO}	CC	D	SOUT data hold time after SCK(4)	SOUT and SCK drive strength				
					LVDS	15 pF to 50 pF differential	0.0	—	ns

1. All DSPI timing specifications apply to pins when using LVDS pads for SCK and SOUT and CMOS pad for PCS with pad driver strength as defined. Timing may degrade for weaker output drivers.
2. TSB = 1 or ITSB = 1 automatically selects MTFE = 1 and CPHA = 1.
3. With TSB mode or Continuous SCK clock mode selected, PCS and SCK are driven by the same edge of DSPI_CLKn. This timing value is due to pad delays and signal propagation delays.
4. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

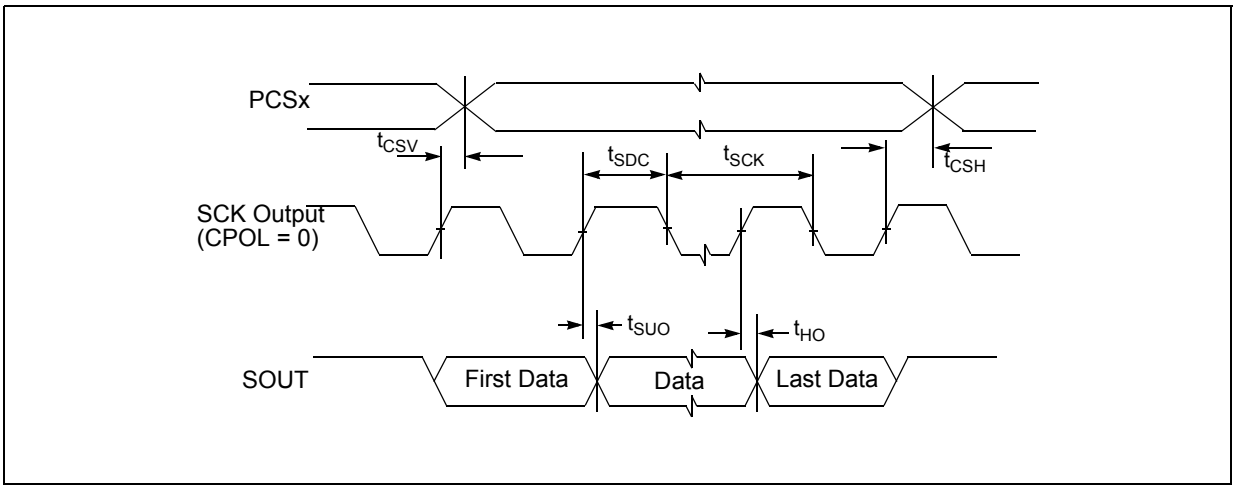
Table 44. DSPI CMOS master timing – output only – timed serial bus mode TSB = 1 or ITSB = 1, CPOL = 0 or 1, continuous SCK clock(1)(2)

#	Symbol		C	Characteristic	Condition		Value(3)		Unit
					Pad drive(4)	Load (C_L)	Min	Max	
1	t_{SCK}	CC	D	SCK cycle time	SCK drive strength				
					Very strong	25 pF	33.0	—	ns
					Strong	50 pF	80.0	—	ns
					Medium	50 pF	200.0	—	ns
2	t_{CSV}	CC	D	PCS valid after SCK(5)	SCK and PCS drive strength				
					Very strong	25 pF	16	—	ns
					Strong	50 pF	16	—	ns
					Medium	50 pF	26	—	ns
					PCS medium and SCK strong	PCS = 50 pF SCK = 50 pF	38	—	ns
3	t_{CSH}	CC	D	PCS hold after SCK(5)	SCK and PCS drive strength				
					Very strong	PCS = 0 pF SCK = 50 pF	–14	—	ns
					Strong	PCS = 0 pF SCK = 50 pF	–14	—	ns
					Medium	PCS = 0 pF SCK = 50 pF	–33	—	ns
					PCS medium and SCK strong	PCS = 0 pF SCK = 50 pF	–35	—	ns
4	t_{SDC}	CC	D	SCK duty cycle(6)	SCK drive strength				
					Very strong	0 pF	$^1/_2t_{SCK} - 2$	$^1/_2t_{SCK} + 2$	ns
					Strong	0 pF	$^1/_2t_{SCK} - 2$	$^1/_2t_{SCK} + 2$	ns
					Medium	0 pF	$^1/_2t_{SCK} - 5$	$^1/_2t_{SCK} + 5$	ns
SOUT data valid time (after SCK edge)									
9	t_{SUO}	CC	D	SOUT data valid time from SCK CPHA = 1(7)	SOUT and SCK drive strength				
					Very strong	25 pF	—	7.0	ns
					Strong	50 pF	—	9.0	ns
					Medium	50 pF	—	25.0	ns
SOUT data hold time (after SCK edge)									
10	t_{HO}	CC	D	SOUT data hold time after SCK CPHA = 1(7)	SOUT and SCK drive strength				
					Very strong	25 pF	–7.7	—	ns
					Strong	50 pF	–11.0	—	ns
					Medium	50 pF	–15.0	—	ns

1. TSB = 1 or ITSB = 1 automatically selects MTFE = 1 and CPHA = 1.
2. All output timing is worst case and includes the mismatching of rise and fall times of the output pads.

3. All timing values for output signals in this table are measured to 50% of the output voltage.
4. Timing is guaranteed to same drive capabilities for all signals, mixing of pad drives may reduce operating speeds and may cause incorrect operation.
5. With TSB mode or Continuous SCK clock mode selected, PCS and SCK are driven by the same edge of DSPI_CLKn. This timing value is due to pad delays and signal propagation delays.
6. t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.
7. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

Figure 32. DSPI LVDS and CMOS master timing – output only – modified transfer format MTFE = 1, CHPA = 1



3.17.2.2 Slave Mode timing

Table 45. DSPI CMOS Slave timing - Modified Transfer Format (MTFE = 0/1)(1)

#	Symbol		C	Characteristic	Condition		Min	Max	Unit
					Pad Drive	Load			
1	t_{SCK}	CC	D	SCK Cycle Time(2)	—	—	62	—	ns
2	t_{CSC}	SR	D	$\overline{SS}$ to SCK Delay(2)	—	—	16	—	ns
3	t_{ASC}	SR	D	SCK to $\overline{SS}$ Delay(2)	—	—	16	—	ns
4	t_{SDC}	CC	D	SCK Duty Cycle(2)	—	—	30	—	ns
5	t_A	CC	D	Slave Access Time(2),(3),(4) ($\overline{SS}$ active to SOUT driven)	Very Strong	25 pF	—	50	ns
					Strong	50 pF	—	50	ns
					Medium	50 pF	—	60	ns
6	t_{DIS}	CC	D	Slave SOUT Disable Time(2),(3),(4) ($\overline{SS}$ inactive to SOUT High-Z or invalid)	Very Strong	25 pF	5	22	ns
					Strong	50 pF	5	28	ns
					Medium	50 pF	5	54	ns
9	t_{SUI}	CC	D	Data Setup Time for Inputs(2)	—	—	10	—	ns
10	t_{HI}	CC	D	Data Hold Time for Inputs(2)	—	—	10	—	ns

Table 45. DSPI CMOS Slave timing - Modified Transfer Format (MTFE = 0/1)(1) (continued)

#	Symbol		C	Characteristic	Condition		Min	Max	Unit
					Pad Drive	Load			
11	t_{SUO}	CC	D	SOUT Valid Time(2),(3),(4) (after SCK edge)	Very Strong	25 pF	—	30	ns
					Strong	50 pF	—	30	ns
					Medium	50 pF	—	55	ns
12	t_{HO}	CC	D	SOUT Hold Time(2),(3),(4) (after SCK edge)	Very Strong	25 pF	2.5	—	ns
					Strong	50 pF	2.5	—	ns
					Medium	50 pF	2.5	—	ns

1. DSPI slave operation is only supported for a single master and single slave on the device. Timing is valid for that case only.
2. Input timing assumes an input slew rate of 1 ns (10% - 90%) and uses TTL / Automotive voltage thresholds.
3. All timing values for output signals in this table, are measured to 50% of the output voltage.
4. All output timing is worst case and includes the mismatching of rise and fall times of the output pads.

Figure 33. DSPI Slave Mode - Modified transfer format timing (MFTE = 0/1) — CPHA = 0

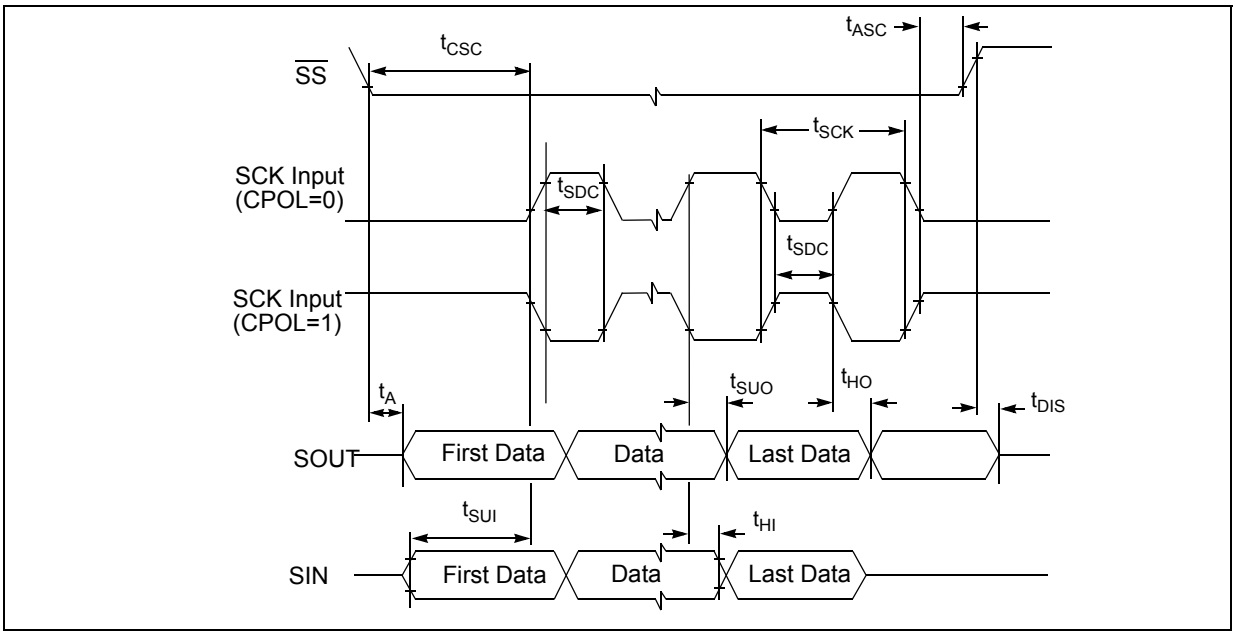
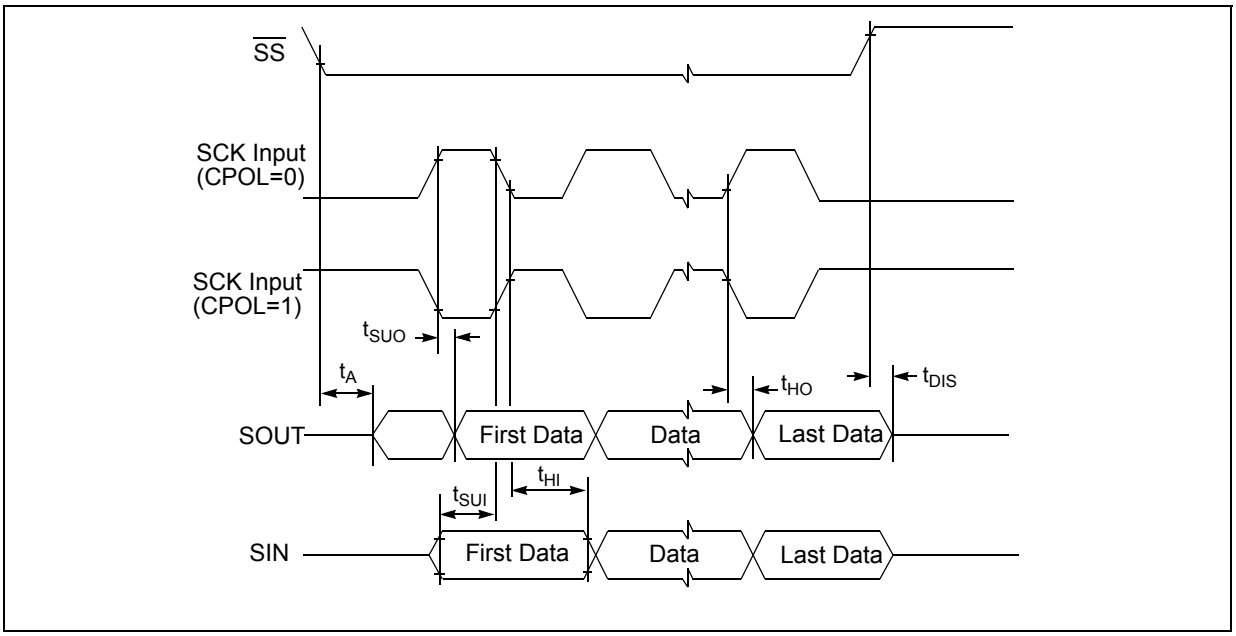


Figure 34. DSPI Slave Mode - Modified transfer format timing (MFTE = 0/1) — CPHA = 1



3.17.3 FEC timing

3.17.3.1 RMII serial management channel timing (MDIO and MDC)

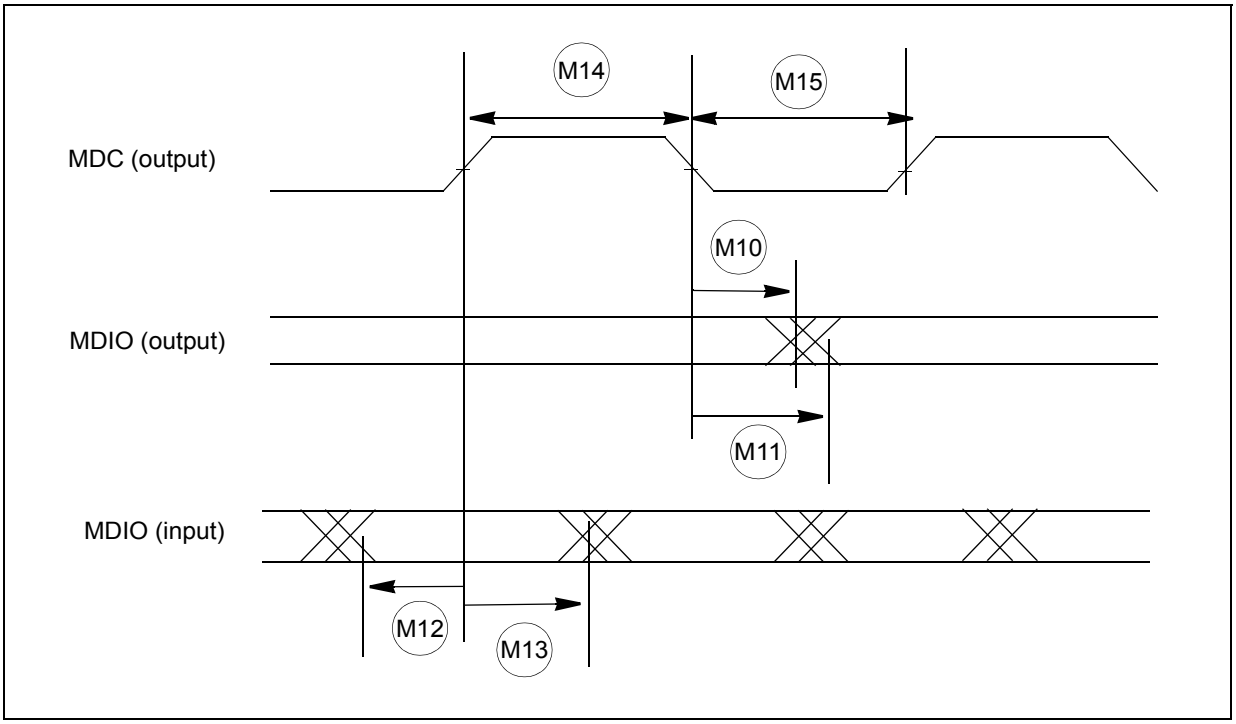
The FEC functions correctly with a maximum MDC frequency of 2.5 MHz.

Table 46. RMII serial management channel timing(1)

Symbol		C	Characteristic	Value		Unit
				Min	Max	
M10	CC	D	MDC falling edge to MDIO output invalid (minimum propagation delay)	0	—	ns
M11	CC	D	MDC falling edge to MDIO output valid (maximum propagation delay)	—	25	ns
M12	CC	D	MDIO (input) to MDC rising edge setup	10	—	ns
M13	CC	D	MDIO (input) to MDC rising edge hold	0	—	ns
M14	CC	D	MDC pulse width high	40%	60%	MDC period
M15	CC	D	MDC pulse width low	40%	60%	MDC period

1. All timing specifications are referenced from MDC = 1.4 V (TTL levels) to the valid input and output levels, 0.8 V and 2.0 V (TTL levels). For 5 V operation, timing is referenced from MDC = 50% to 2.2 V/3.5 V input and output levels.

Figure 35. RMII serial management channel timing diagram



3.17.3.2 RMII receive signal timing (RXD[1:0], CRS_DV)

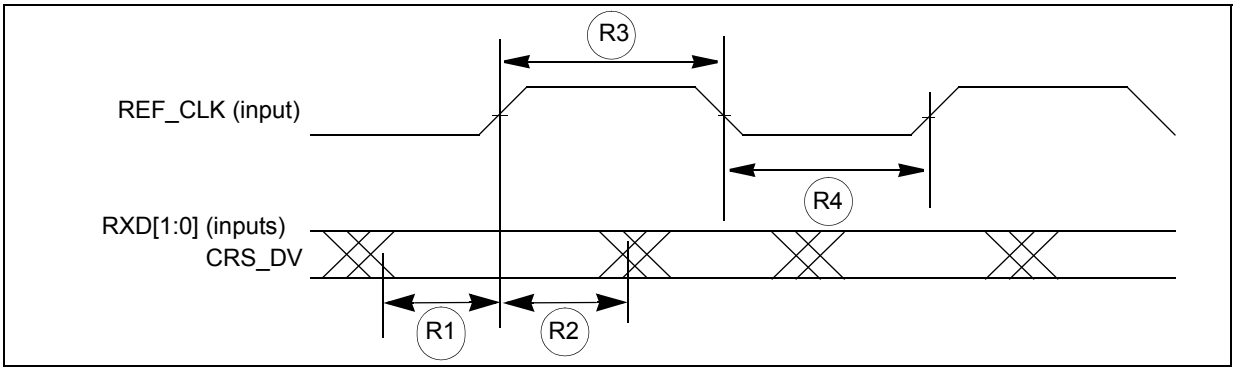
The receiver functions correctly up to a REF_CLK maximum frequency of 50 MHz +1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the RX_CLK frequency, which is half that of the REF_CLK frequency.

Table 47. RMII receive signal timing(1)

Symbol		C	Characteristic	Value		Unit
				Min	Max	
R1	CC	D	RXD[1:0], CRS_DV to REF_CLK setup	4	—	ns
R2	CC	D	REF_CLK to RXD[1:0], CRS_DV hold	2	—	ns
R3	CC	D	REF_CLK pulse width high	35%	65%	REF_CLK period
R4	CC	D	REF_CLK pulse width low	35%	65%	REF_CLK period

1. All timing specifications are referenced from REF_CLK = 1.4 V to the valid input levels, 0.8 V and 2.0 V.

Figure 36. RMII receive signal timing diagram



3.17.3.3 RMII transmit signal timing (TXD[1:0], TX_EN)

The transmitter functions correctly up to a REF_CLK maximum frequency of 50 MHz + 1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the TX_CLK frequency, which is half that of the REF_CLK frequency.

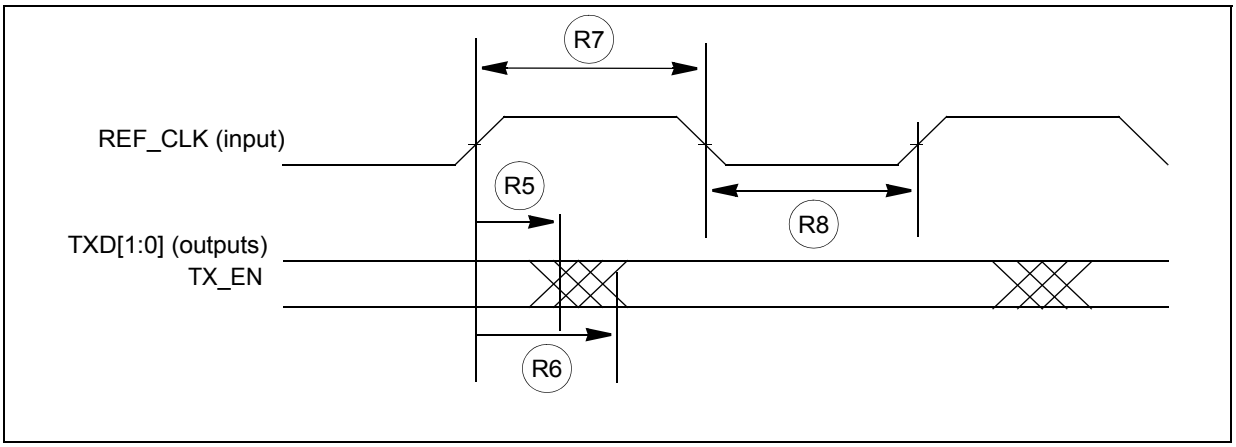
The transmit outputs (TXD[1:0], TX_EN) can be programmed to transition from either the rising or falling edge of REF_CLK, and the timing is the same in either case. This options allows the use of non-compliant RMII PHYs.

Table 48. RMII transmit signal timing(1)

Symbol		C	Characteristic	Value		Unit
				Min	Max	
R5	CC	D	REF_CLK to TXD[1:0], TX_EN invalid	2	—	ns
R6	CC	D	REF_CLK to TXD[1:0], TX_EN valid	—	16	ns
R7	CC	D	REF_CLK pulse width high	35%	65%	REF_CLK period
R8	CC	D	REF_CLK pulse width low	35%	65%	REF_CLK period

1. RMII timing is valid only up to a maximum of 150 °C junction temperature.

Figure 37. RMII transmit signal timing diagram



3.17.4 UART timing

UART channel frequency support is shown in the following table.

Table 49. UART frequency support

LINFlexD clock frequency LIN_CLK (MHz)	Oversampling rate	Voting scheme	Max usable frequency (Mbaud)
80	16	3:1 majority voting	5
	8		10
	6	Limited voting on one sample with configurable sampling point	13.33
	5		16
	4		20
100	16	3:1 majority voting	6.25
	8		12.5
	6	Limited voting on one sample with configurable sampling point	16.67
	5		20
	4		25

3.17.5 GPIO delay timing

The GPIO delay timing specification is provided in the following table.

Table 50. GPIO delay timing

Symbol		C	Parameter	Value		Unit
				Min	Max	
IO_delay	CC	D	Delay from MSCR bit update to pad function enable	5	25	ns

4 Package characteristics

4.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

4.2 eTQFP80 case drawing

Figure 38. eTQFP80 – STMicroelectronics package mechanical drawing

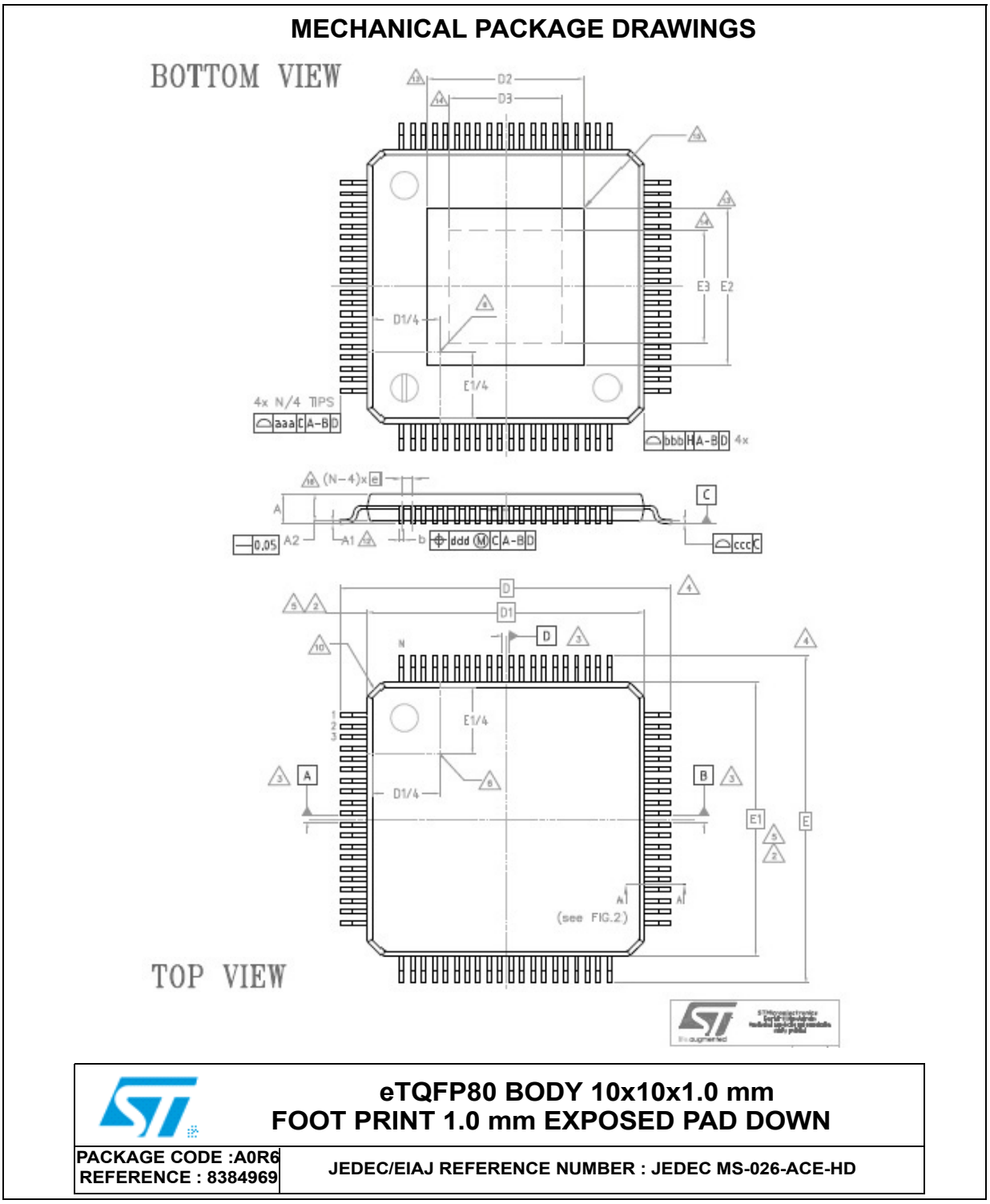


Table 51. eTQFP80 – STMicroelectronics package mechanical data

Symbol	Dimensions					
	Millimeters			Inches[1]		
	Min	Typ	Max	Min	Typ	Max
q	0°	3.5°	7°	0°	3.5°	7°
q1	0°	—	—	0°	—	—
q2	10°	12°	14°	10°	12°	14°
q3	10°	12°	14°	10°	12°	14°
A[2]	—	—	1.20	—	—	0.047
A1[3]	0.05	—	0.15	0.002	—	0.006
A2[2]	0.95	1.00	1.05	0.037	0.039	0.041
b[4] [5]	0.13	0.18	0.23	0.005	0.007	0.009
b1[4]	0.13	0.16	0.19	0.005	0.006	0.007
c[4]	0.09	—	0.20	0.004	—	0.008
c1[4]	0.09	—	0.16	0.004	—	0.006
D[6]	12.00 BSC			0.472 BSC		
D1[7] [8]	10.00 BSC			0.394 BSC		
D2[9]	—	—	5.83	—	—	0.229
D3[10]	4.00	—	—	0.157	—	—
e	0.40 BSC			0.016 BSC		
E[6]	12.00 BSC			0.472 BSC		
E1[7] [8]	10.00 BSC			0.394 BSC		
E2[9]	—	—	5.83	—	—	0.229
E3[10]	4.00	—	—	0.157	—	—
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
N[11]	80			3.149		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	—	0.003	—	—
S	0.20	—	—	0.008	—	—
aaa[12]	0.20			0.008		
bbb[12]	0.20			0.008		
ccc[12]	0.08			0.003		
ddd[12]	0.07			0.003		

1. Values in inches are converted from millimeters (mm) and rounded to three decimal digits.
2. The optional exposed pad is generally coincident with the top or bottom side of the package and not allowed to protrude beyond that surface.

3. A1 is defined as the distance from the seating plane to the lowest point on the package body.
4. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
5. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
6. To be determined at seating datum plane C.
7. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
8. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
9. Dimensions D2 and E2 show the maximum exposed metal area on the package surface where the exposed pad is located (if present). It includes all metal protrusions from exposed pad itself. Type of exposed pad is variable depending on leadframe pad design (T1, T2, T3). End user should verify D2 and E2 dimensions according to specific device application.
10. Dimensions D3 and E3 show the minimum solderable area, defined as the portion of exposed pad which is guaranteed to be free from resin flashes/bleeds, bordered by internal edge of inner groove.
11. “N” is the number of terminal positions for the specified body size.
12. Tolerance

4.3 eTQFP100 case drawing

Figure 39. eTQFP100 – STMicroelectronics package mechanical drawing

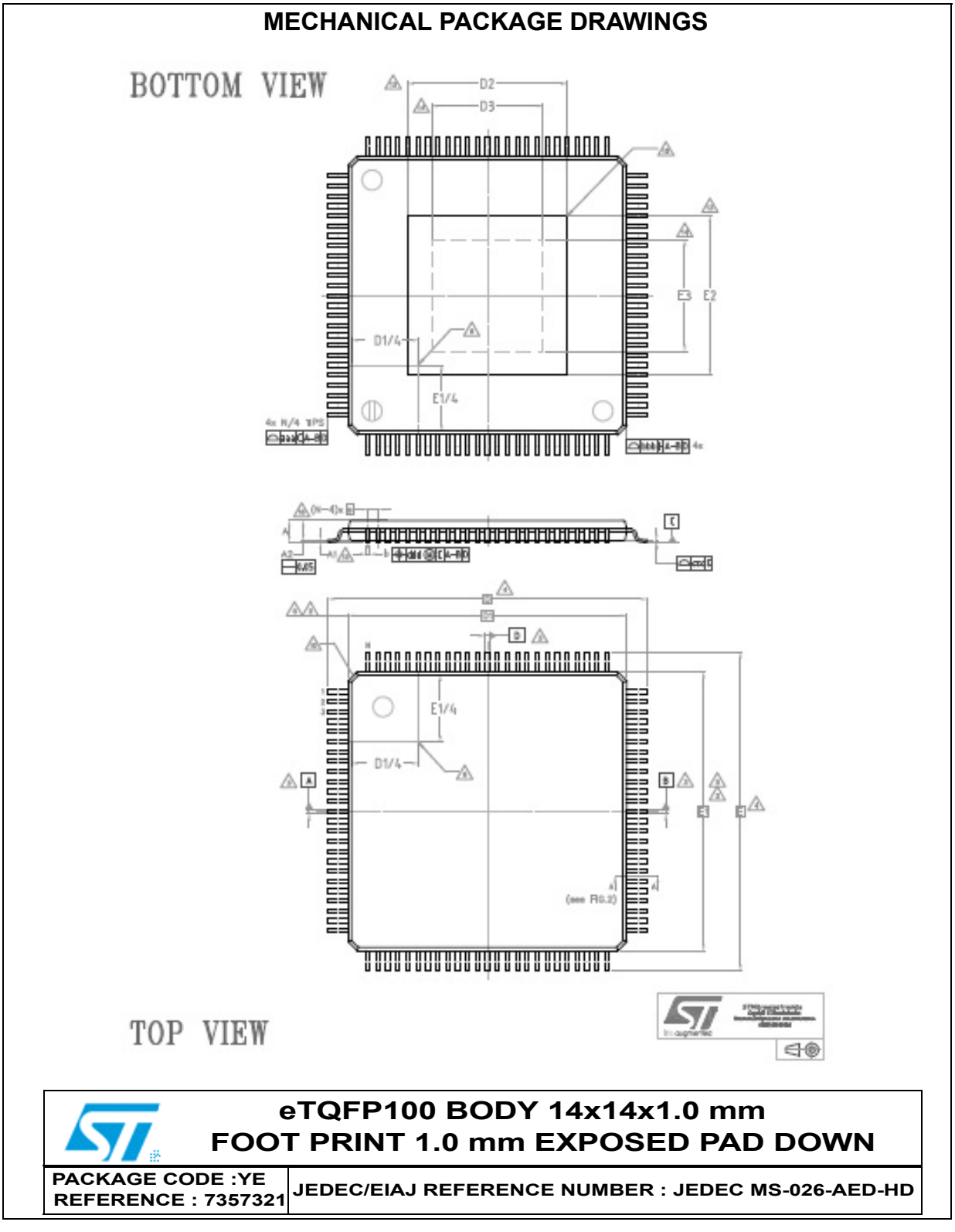


Table 52. eTQFP100 – STMicroelectronics package mechanical data

Symbol	Dimensions					
	Millimeters			Inches[1]		
	Min	Typ	Max	Min	Typ	Max
q	0°	3.5°	7°	0°	3.5°	7°
q1	0°	—	—	0°	—	—
q2	10°	12°	14°	10°	12°	14°
q3	10°	12°	14°	10°	12°	14°
A[2]	—	—	1.20	—	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2[2]	0.95	1.00	1.05	0.037	0.039	0.041
b[3] [4]	0.17	0.22	0.27	0.007	0.009	0.011
b1[4]	0.175	0.20	0.23	0.007	0.008	0.009
c[4]	0.09	—	0.20	0.004	—	0.008
c1[4]	0.09	—	0.16	0.004	—	0.006
D[5]	16.00 BSC			0.629 BSC		
D1[6] [7]	14.00 BSC			0.551 BSC		
D2[8]	—	—	5.67	—	—	0.223
D3[9]	4.00	—	—	0.157	—	—
e	0.50 BSC			0.019 BSC		
E[5]	16.00 BSC			0.629 BSC		
E1[6] [7]	14.00 BSC			0.551 BSC		
E2[8]	—	—	5.67	—	—	0.223
E3[9]	4.00	—	—	0.157	—	—
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
N[10]	100			3.937		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	—	0.003	—	—
S	0.20	—	—	0.008	—	—
aaa[11]	0.15			0.006		
bbb[11]	0.20			0.008		
ccc[11]	0.05			0.002		
ddd[11]	0.07			0.003		

1. Values in inches are converted from millimeters (mm) and rounded to three decimal digits.
2. The optional exposed pad is generally coincident with the top or bottom side of the package and not allowed to protrude beyond that surface.

3. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
4. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
5. To be determined at seating datum plane C.
6. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
7. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
8. Dimensions D2 and E2 show the maximum exposed metal area on the package surface where the exposed pad is located (if present). It includes all metal protrusions from exposed pad itself. Type of exposed pad is variable depending on leadframe pad design (T1, T2, T3). End user should verify D2 and E2 dimensions according to specific device application.
9. Dimensions D3 and E3 show the minimum solderable area, defined as the portion of exposed pad which is guaranteed to be free from resin flashes/bleeds, bordered by internal edge of inner groove.
10. “N” is the number of terminal positions for the specified body size.
11. Tolerance

4.4 Thermal characteristics

Table 53 and *Table 54* describe the thermal characteristics of the device.

Table 53. Thermal characteristics for eTQFP80(1)

Symbol		C	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-ambient, natural convection(2)	Four layer board—2s2p	29.6	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-moving-air, ambient(2)	At 200 ft./min., four layer board—2s2p	23.5	°C/W
$R_{\theta JB}$	CC	D	Junction-to-board(3)	Ring cold plate	9.6	°C/W
$R_{\theta JCtop}$	CC	D	Junction-to-case top(4)	Cold plate	13.2	°C/W
$R_{\theta JCbotttom}$	CC	D	Junction-to-case bottom(5)	Cold plate	1.0	°C/W
Ψ_{JT}	CC	D	Junction-to-package top(6)	Natural convection	0.4	°C/W

1. The values are based on simulation; actual data may vary in the given range. The specified characteristics are subject to change per final device design and characterization. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
3. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
5. Thermal resistance between the die and the solder pad on the bottom of the package. Interface resistance is ignored.
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

Table 54. Thermal characteristics for eTQFP100[1]

Symbol		C	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-ambient, natural convection[2]	Four layer board—2s2p	27.9	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-moving-air, ambient[2]	At 200 ft./min., four layer board—2s2p	22.8	°C/W
$R_{\theta JB}$	CC	D	Junction-to-board[3]	Ring cold plate	11.3	°C/W
$R_{\theta JCtop}$	CC	D	Junction-to-case top[4]	Cold plate	13.0	°C/W
$R_{\theta JCbotttom}$	CC	D	Junction-to-case bottom[5]	Cold plate	1.0	°C/W
Ψ_{JT}	CC	D	Junction-to-package top[6]	Natural convection	0.4	°C/W

1. The values are based on simulation; actual data may vary in the given range. The specified characteristics are subject to change per final device design and characterization. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
3. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
5. Thermal resistance between the die and the solder pad on the bottom of the package. Interface resistance is ignored.
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

4.4.1 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

Equation 1 $T_J = T_A + (R_{\theta JA} * P_D)$

where:

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The thermal resistance values used are based on the JEDEC JESD51 series of standards to provide consistent values for estimations and comparisons. The difference between the values determined for the single-layer (1s) board compared to a four-layer board that has two signal layers, a power and a ground plane (2s2p), demonstrate that the effective thermal resistance is not a constant. The thermal resistance depends on the:

- Construction of the application board (number of planes)
- Effective size of the board which cools the component
- Quality of the thermal and electrical connections to the planes
- Power dissipated by adjacent components

Connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes reduces the thermal performance. Thinner planes also reduce the thermal performance. When the clearance between the vias leave the planes virtually disconnected, the thermal performance is also greatly reduced.

As a general rule, the value obtained on a single-layer board is within the normal range for the tightly packed printed circuit board. The value obtained on a board with the internal planes is usually within the normal range if the application board has:

- One oz. (35 micron nominal thickness) internal planes
- Components are well separated
- Overall power dissipation on the board is less than 0.02 W/cm^2

The thermal performance of any component depends on the power dissipation of the surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

Equation 2 $T_J = T_B + (R_{\theta JB} * P_D)$

where:

T_B = board temperature for the package perimeter (°C)

$R_{\theta JB}$ = junction-to-board thermal resistance (°C/W) per JESD51-8

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air does not factor into the calculation, the junction temperature is predictable if the application board is similar to the thermal test condition, with the component soldered to a board with internal planes.

The thermal resistance is expressed as the sum of a junction-to-case thermal resistance plus a case-to-ambient thermal resistance:

Equation 3 $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

$R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and is not affected by other factors. The thermal environment can be controlled to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for packages with heat sinks where 90% of the heat flow is through the case to heat sink to ambient. For most packages, a better model is required.

A more accurate two-resistor thermal model can be constructed from the junction-to-board thermal resistance and the junction-to-case thermal resistance. The junction-to-case thermal resistance describes when using a heat sink or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used to generate simple estimations and for computational fluid dynamics (CFD) thermal models. More accurate compact Flotherm models can be generated upon request.

To determine the junction temperature of the device in the application on a prototype board, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature by measuring the temperature at the top center of the package case using the following equation:

Equation 4 $T_J = T_T + (\Psi_{JT} \times P_D)$

where:

T_T = thermocouple temperature on top of the package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured in compliance with the JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. Position the thermocouple so that the thermocouple junction rests on the package. Place a small amount of epoxy on the thermocouple junction and approximately 1 mm of wire extending from the junction. Place the thermocouple wire flat against the package case to avoid measurement errors caused by the cooling effects of the thermocouple wire.

When board temperature is perfectly defined below the device, it is possible to use the thermal characterization parameter (Ψ_{JPB}) to determine the junction temperature by measuring the temperature at the bottom center of the package case (exposed pad) using the following equation:

Equation 5 $T_J = T_B + (\Psi_{JPB} \times P_D)$

where:

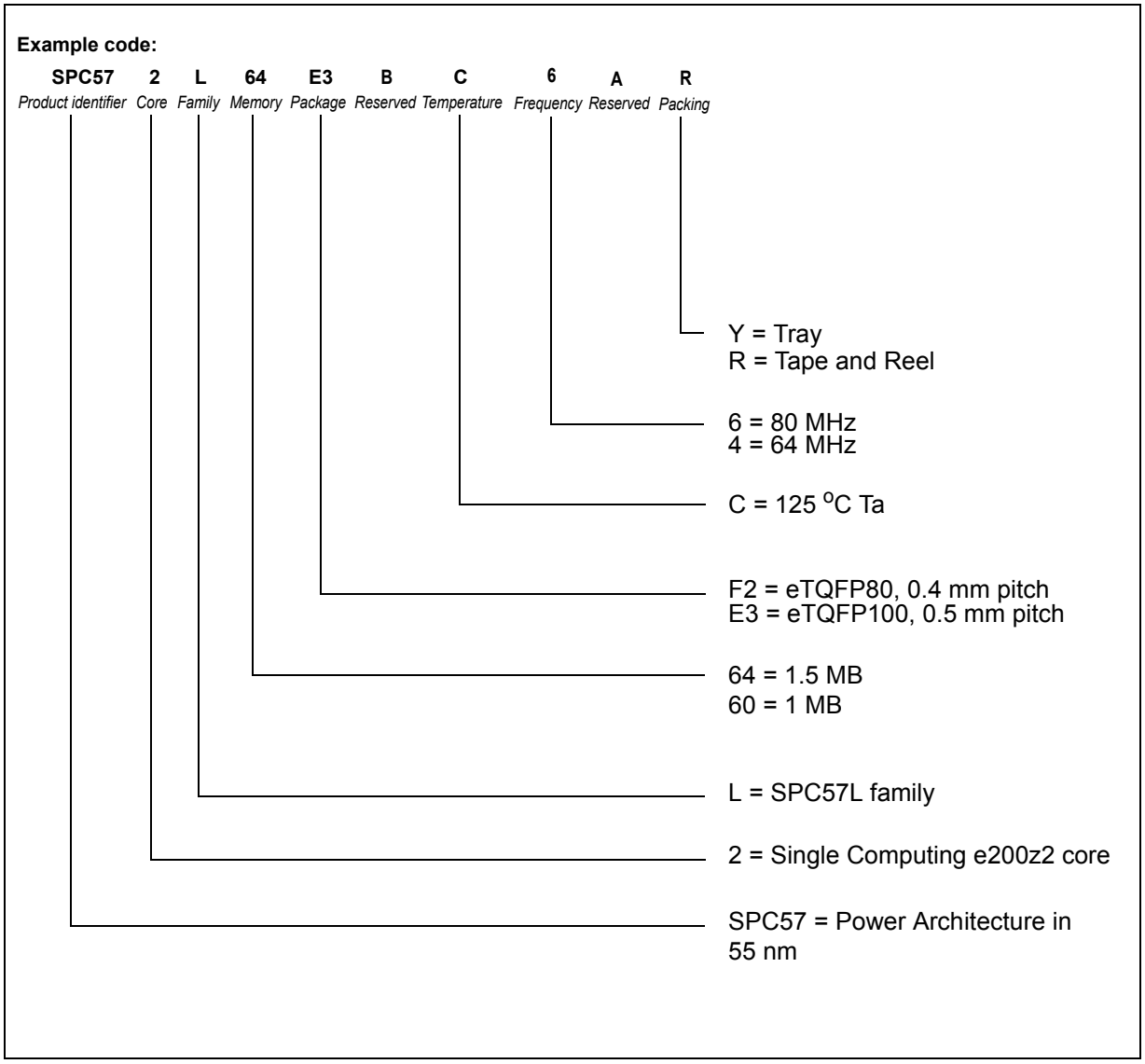
T_T = thermocouple temperature on bottom of the package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

5 Ordering information

Figure 40. Product code structure



1. Order on 1 MB part numbers can be entered upon ST's acceptance conditioned by volumes. Please contact your ST sales office to ask for the availability of a particular commercial product.
2. Features (e.g. flash, RAM or peripherals) not included in the commercial product cannot be used. ST cannot be called to take any liability for features used outside the commercial product.

6 Revision history

Table 55 summarizes revisions to this document.

Table 55. Document revision history

Date	Revision	Changes
18-Jul- 2012	1	Initial release.
03-Apr-2013	2	Formatting and editorial changes throughout document. *Table 2: SPC572Lx device feature summary*: Changed title (was *SPC5726SPC572L64 device feature summary*) *Figure 2 (Periphery allocation)*: Removed BAR module from diagram. *Section 1.5, Features overview*: Added detail to PIT descriptions (2 bullets). Added *Saturation Instructions Extension...* feature item. *Figure 4 (100-pin QFP configuration (top view))*: Changed pin 65 to “ESR1” *Table 3 (Power supply and reference pins)*: For row V_{DD_LV}: added pin 68 for 100 pin and 80 pin packages. *Section 2.2.1, Power supply and reference voltage pins*: Added 2 sentences starting from “The Supply Pins Table contains...” Table 5 (Port pins description): From PC[10] to PC[15] - changed *VDD_HV_IO_FLEX* to *VDD_HV_IO_ETH* *Table 7 (Absolute maximum ratings)*: Added footnote *VDD_HV_IO refers to...* *Section 2.2.1, Power supply and reference voltage pins*: Added 2 sentences starting from *The Supply Pins Table contains...* *Table 8 (ESD ratings,)*: Added classification column *Table 9 (Device operating conditions)*: Removed rows $V_{DD\_HV\_ADR\_D}$ and $V_{DD\_HV\_ADR\_S}$ For row $V_{DD\_HV\_ADR}$: divided Value Min column data into “C” (3.0) and “P” (4.0) values and added the word *reference* to the Parameter description column Changed row $V_{SS\_HV\_ADR}$ symbol (was $V_{SS\_HV\_ADR\_D}$) Changed VDD_HV_ADV Value Min column data for *P* characteristic to 4.0 (was 4.2) *Table 9 (Device operating conditions)*: For row $V_{DD\_HV\_ADR}$: inverted the *C* and *P* Parameter Classification values. *Table 10 (DC electrical specifications)*: Removed the following rows: $V_{DD\_HV\_IO}$, $V_{DD\_HV\_IO\_JTAG}$, $V_{DD\_HV\_IO\_ETH}$, $V_{DD\_HV\_ADV}$, $V_{DD\_HV\_ADR}$, $V_{DD\_HV\_ADR}$ – $V_{DD\_HV\_ADV}$ *Table 12 (I/O input DC electrical characteristics)*: In row V_{IHTTL} condition changed to 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V. In row V_{ILTTL} condition changed to 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V. In row V_{HYSTTL} condition changed to 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V. In row V_{IHCMOS_H} condition changed to 2.7 V < $V_{DD\_HV\_IO}$ < 3.0 V and 4.0 V < $V_{DD\_HV\_IO}$ < 4.5 V. In row V_{IHCMOS} condition changed to 2.7 V < $V_{DD\_HV\_IO}$ < 3.0 V and 4.0 V < $V_{DD\_HV\_IO}$ < 4.5 V. In row V_{ILCMOS_H} condition changed to 2.7 V < $V_{DD\_HV\_IO}$ < 3.0 V and 4.0 V < $V_{DD\_HV\_IO}$ < 4.5 V. In row $V_{HYSCMOS}$ condition changed to 2.7 V < $V_{DD\_HV\_IO}$ < 3.0 V and 4.0 V < $V_{DD\_HV\_IO}$ < 4.5 V.

Table 55. Document revision history (continued)

Date	Revision	Changes
03-Apr-2013	2 (cont.)	*Table 13 (I/O pull-up/pull-down DC electrical characteristics)*: In row $\|I_{WPU}\|$ changed to *Weak pull-up current absolute value* In row $\|I_{WPU}\|$ (P) condition changed to $V_{IN} < V_{IH} = 0.69*V_{DD\_HV\_IO}$, $4.5\ V < V_{DD\_HV\_IO} < 5.5\ V$. In row $\|I_{WPU}\|$ (P) minimum changed to 23 µA; maximum value deleted. In row $\|I_{WPD}\|$ (P) minimum deleted; maximum value changed to 130 µA. In row $\|I_{WPD}\|$ (P) condition changed to $V_{IN} > V_{IH} = 0.69*V_{DDE}$, $4.5\ V < V_{DD} < 5.5\ V$. Deleted: $\|I_{WPU}\|$ (T) at $V_{IN} = 0\ V$, $3.0\ V < V_{DD\_HV\_IO} < 4.0\ V$. Added $\|I_{WPU}\|$ (T) at $V_{IN} > V_{IL} = 0.49*V_{DDE}$, $4.5\ V < V_{DD} < 5.5\ V$. Added $\|I_{WPU}\|$ (T) at $V_{IN} > V_{IL} = 1.1\ V$ (TTL), $4.5\ V < V_{DD} < 5.5\ V$. Added R_{WPU} (Weak pull-up resistance). Deleted: $\|I_{WPD}\|$ (T) at $V_{IN} = V_{DD\_HV\_IO}$, $3.0\ V < V_{DD\_HV\_IO} < 4.0\ V$. Added $\|I_{WPD}\|$ (T) at $V_{IN} < V_{IL} = 0.49*V_{DDE}$, $4.5\ V < V_{DD} < 5.5\ V$. Added $\|I_{WPD}\|$ (T) at $V_{IN} < V_{IL} = 0.9\ V$ (TTL), $4.5\ V < V_{DD} < 5.5\ V$. Added R_{WPD} (Weak pull-down resistance). *Table 14 (WEAK configuration output buffer electrical characteristics)*: Added footnote 4. Specification changes: In row R_{OH_W} condition changed to $4.5\ V < V_{DD\_HV\_IO} < 5.9\ V$, Push pull, $I_{OH} < 0.5\ mA$. In row R_{OL_W} condition changed to $4.5\ V < V_{DD\_HV\_IO} < 5.9\ V$, Push pull, $I_{OH} < 0.5\ mA$. In row t_{TR_W} condition $C_L = 25\ pF$, $4.0\ V < V_{DD\_HV\_IO} < 5.9\ V$ changed to $C_L = 25\ pF$, $4.5\ V < V_{DD\_HV\_IO} < 5.9\ V$ In row t_{TR_W} condition $C_L = 50\ pF$, $4.0\ V < V_{DD\_HV\_IO} < 5.9\ V$ changed to $C_L = 50\ pF$, $4.5\ V < V_{DD\_HV\_IO} < 5.9\ V$ In row t_{TR_W} condition $C_L = 200\ pF$, $4.0\ V < V_{DD\_HV\_IO} < 5.9\ V$ changed to $C_L = 200\ pF$, $4.5\ V < V_{DD\_HV\_IO} < 5.9\ V$ *Table 15 (MEDIUM configuration output buffer electrical characteristics)*: Added footnote 4. In R_{OH_M} condition changed to $4.5\ V < V_{DD\_HV\_IO} < 5.9\ V$, Push pull, $I_{OH} < 2\ mA$. In R_{OL_M} condition changed to $4.5\ V < V_{DD\_HV\_IO} < 5.9\ V$, Push pull, $I_{OH} < 2\ mA$. In t_{TR_M} condition changed to $C_L = 25\ pF$, $4.5\ V < V_{DD\_HV\_IO} < 5.9\ V$. In t_{TR_M} condition changed to $C_L = 50\ pF$, $4.5\ V < V_{DD\_HV\_IO} < 5.9\ V$. In t_{TR_M} condition changed to $C_L = 200\ pF$, $4.5\ V < V_{DD\_HV\_IO} < 5.9\ V$. *Table 16 (STRONG configuration output buffer electrical characteristics)*: Added footnote 4. In R_{OH_S} condition changed to $4.5\ V < V_{DD\_HV\_IO} < 5.9\ V$, Push pull, $I_{OH} < 8\ mA$. IN R_{OL_S} condition changed to $4.5\ V < V_{DD\_HV\_IO} < 5.9\ V$, Push pull, $I_{OH} < 8\ mA$. In t_{TR_S} condition changed to $C_L = 50\ pF$, $4.5\ V < V_{DD\_HV\_IO} < 5.9\ V$. In t_{TR_S} condition changed to $C_L = 200\ pF$, $4.5\ V < V_{DD\_HV\_IO} < 5.9\ V$. In t_{TR_S} condition $C_L = 50\ pF$, $4.5\ V < V_{DD\_HV\_IO} < 5.9\ V$. *Table 17 (VERY STRONG configuration output buffer electrical characteristics)*: Removed footnote: *For specification per Electrical Physical Layer Specification 3.0.1...* *Section 3.9, I/O pad current specification*: Changed Note *In order to ensure ... remain below 10%.* changed to *...below 50%.* *Table 19 (Reset electrical characteristics)* Added footnote to row I_{OL_R}: *I_{OL_R} applies to both PORST and ESR0...* In row I_{OL_R} condition changed to *Device under power-on reset, $3.0\ V < V_{DD\_HV\_IO} < 5.5\ V$, $V_{OL} > 1.0\ V$.* In row I_{OL_R} minimum for conditions *Device under power-on reset, $3.0\ V < V_{DD\_HV\_IO} < 5.5\ V$, $V_{OL} > 1.0\ V$* changed to12 mA. *Table 23 (Internal RC oscillator electrical specifications)*: In row t_{start_T} Parameter Classification changed to *D* (was *T*).

Table 55. Document revision history (continued)

Date	Revision	Changes
03-Apr-2013	2 (cont.)	*Table 25 (SARn ADC electrical specification)*: Row $V_{DD\_HV\_ADR\_S}$ removed. In row V_{IN} Max Value cell changed to $V_{DD\_HV\_ADR}$ (was $V_{DD\_HV\_ADR\_S}$) In row TUE_{12} updated conditions In row TUE_{10} changed Characteristic for both conditions to *T* and updated conditions In row V_{ALTREF} changed the Parameter Classification to *C* (was P*)*. Added phrase *For parameters classified as T and D*. to footnote *TUE and DNL...* *Table 26 (SDn ADC electrical specification)* In row f_{IN} - changed Parameter Classification for both conditions to *D* (was *P*) Removed rows – $V_{DD\_HV\_ADV}$, $V_{SS\_HV\_ADR\_D}$, $V_{DD\_HV\_ADR\_D}$ For V_{IN_PK2PK} (Input range peak to peak $V_{IN\_PK2PK} = V_{INP} – V_{INM}$) corrected GAIN condition for Single ended – $V_{INM} = 0.5*V_{DD\_HV\_ADR\_D}$ GAIN = 2,4,8,16. In δ_{GROUP} condition OSR = 75, changed Max Value to 596. Added footnote *V_{INM} is the input voltage applied to the negative terminal of the SDADC.* For rows $SNR_{DIFF150}$, $SNR_{DIFF333}$ and SNR_{SE150} added footnote *SNR degradated by 3dB, in the range 3.6 V< $V_{DD\_HV\_ADV}$ < 5.5 V.* *Table 27 (Temperature sensor electrical characteristics)*: In row I_{TEMP_SENS} changed description to *VDD_HV_ADV power supply current*. *Section 3.15.2, Main voltage regulator electrical characteristics*: Changed HV and BV supply voltage descriptions. *Table 31 (Voltage regulator electrical characteristics)*: Updated all values. *Figure 19 (Voltage monitor threshold definition)*: Reworked diagram *Table 32 (Voltage monitor electrical characteristics)*: Refomatted table and updated all content. *Table 34 (Functional terminals state during power-up and reset)*: in TERMINAL *ERROR* row removed Comments. *Section 3.16, Flash memory electrical characteristics*: Added content relating to Flash read wait states and added *Table 35 (RWSC settings)*. *Table 36 (Flash memory program and erase specifications (pending silicon characterization))*: Updated footnotes, parameter classifications, Initial Max 25 °C values, Initial max parameter classifications and Typical end of life values. Added rows $t_{pprogrameep}$ and $t_{qprogrameep}$ In Rows $t_{16kprogrameep}$ and $t_{16keraseeep}$ changed partition information to *partition 1*. *Table 41 (DSPI CMOS master classic timing (full duplex and output only) – MTFE = 0, CPHA = 0 or 1)* Changed footnote *Maximum frequency is 100 MHz* to *Maximum frequency is 80 MHz.* *Table 42 (DSPI CMOS master modified timing (full duplex and output only) – MTFE = 1, CPHA = 0 or 1)* Changed footnote *Maximum frequency is 100 MHz* to *Maximum frequency is 80 MHz.* *Table 49 (DSPI LVDS slave timing – full duplex – modified transfer format (MTFE = 0/1)):* Changed footnote *Maximum frequency is 100 MHz* to *Maximum frequency is 80 MHz.* *Table 49 (UART frequency support)*: Added row clock frequency 100. *Section 4.2: eTQFP80 case drawing* Added mechanical drawings. *Section 4.3: eTQFP100 case drawing* Added mechanical drawings. *Table 53 (Thermal characteristics for eTQFP80)*:

Table 55. Document revision history (continued)

Date	Revision	Changes
03-Apr-2013	2 (cont.)	Updated table, added $R_{\theta JA}$ Min and Max values *Table 54 (Thermal characteristics for eTQFP100)*: Updated table, added $R_{\theta JA}$ Min and Max values
18-May-2015	3	Following are the changes in this version of the Datasheet: Formatting and editorial changes throughout document. *Table 2 (SPC572Lx device feature summary)*: Replaced SIPI/LAST Interprocessor bus with Zipwire (SIPI/LAST) Interprocessor bus. Updated the description of SENT bus. *Figure 1 (Block diagram)*: Replaced LFAST & SIPI with Zipwire (LFAST & SIPI). *Section 1.5, Features overview* Reworded the PIT bullet points. Replaced “two channel multiplexer” with “two channel multiplexers” Removed “Port pins description” table since the table is included in the JPC5726M_IO_Signal_Table.xlsx sheet. *Section 3.1, Introduction* Added $V_{DD\_HV\_PMC}$ to the note section. *Table 7 (Absolute maximum ratings)*: In row V_{DD_LV} added footnotes: Allowed 1.375 – 1.45 V for 10 hours... 1.32 – 1.375 V range allowed periodically for supply... In footnote: 1.32 – 1.375 V range allowed periodically... changed 1.275 V to 1.288 V Removed $V_{DD\_HV\_FLA}$ and $V_{DD\_HV\_IO\_JTAG}$ rows. Removed T_J row. For I_{MAXD}, replaced minimum and maximum values of “-10” and “10” with “-11” and “11”. Updated t_{XRAY}. Added a note to $V_{DD\_HV\_ADV}$. *Table 9 (Radiated emissions testing specification)*: Added “36 dBµV” in all the rows of column “BISS radiated emissions limit”. *Table 10 (Conducted emissions testing specifications)*: Added “BISS limit” column. *Table 8 (ESD ratings,)*: Classification parameter for ESD for Human Body Model is now *T*.

Table 55. Document revision history (continued)

Date	Revision	Changes
18-May-2015	3 (cont.)	*Table 9 (Device operating conditions)*: Changed VRAMP to V_{RAMP_LV}, changed parameter to “slew rate on core power supply pins”. Added V_{RAMP_HV} specification, parameter “Slew rate on HV power supply pins”, max value 100 V/ms. Updated the classification of f_{SYS} to “C”. Updated the $V_{DD\_HV\_IO\_MAIN}$ classification, minimum, and maximum values. Updated the $V_{DD\_HV\_IO\_JTAG}$ classification, minimum, and maximum values. Added V_{IN} symbol. Updated all the columns of the $V_{DD\_HV\_ADV}$ symbol. Replaced note below the table “Reduced output/input capabilities below 4.2 V. See performance ...” with “Reduced output/input capabilities below 4.2 V. See performance operating values in I/O pad electrical characteristics. Not all functionality are guaranteed below 4.2V. Please check ...” *Table 10 (DC electrical specifications)*: Updated the maximum values of I_{DD} from “100” to “145”. Changed the classification of I_{DDPE} from “P” to “C”. Updated the condition of I_{DDAPP} and the maximum value is updated to 125 mA. Updated the parameter, conditions, and maximum values of I_{DDAR}. Added another row to it. Changed the classification of I_{SPIKE} from “C” to “T”. Changed the classification of dI from “C” to “T”. Replaced “20 us” with “< 20 us” in the conditions column of dI. Changed the classification of I_{SR} from “C” to “D”. Updated the parameter column of I_{SR}. Deleted I_{INACT_D}, I_{IC}, and T_A (T_L to T_H). Replaced the maximum value of “90” with “60” for I_{SPIKE} Replaced the maximum value of “120” with “165” for I_{DDPE}. Added $V_{REF\_BG\_T}$, $V_{REF\_BG\_TC}$, and $V_{REF\_BG\_LR}$ symbols. *Table 11 (I/O pad specification descriptions)*: In row *Very Strong Configuration*, removed reference to *FlexRay*. *Table 12 (I/O input DC electrical characteristics)*: For V_{HYSTTL} replaced “0.3” with “0.275” for minimum value. For V_{ILAUT} replaced “2.2” with “2.1” for maximum value. For V_{HYSAUT} replaced “0.5” with “0.4” for minimum value. Updated the I_{LKG}. Updated the conditions of I_{LKG_MED}. Added “GPIO input pins” to the conditions column of C_{IN}. Updated Note 6 below the table. For V_{DRFTTT}, $V_{DRFTAUT}$, and $V_{DRFTCMOS}$ replaced “C” with “T” in characteristics column. Updated note in maximum value of V_{IHAUT}. *Table 13 (I/O pull-up/pull-down DC electrical characteristics)*: V_{DDE} replaced by $V_{DD\_HV\_IO}$. Updated I_{WPU} rows. Updated I_{WPD} rows. Added R_{WPU} parameter. Added conditions to R_{WPD} parameter.

Table 55. Document revision history (continued)

Date	Revision	Changes
18-May-2015	3 (cont.)	*Table 14 (WEAK configuration output buffer electrical characteristics)*: "4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V" replaced by "4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V" in R_{OH_W} and R_{OL_W} rows. Minimum values of R_{OH_W} and R_{OL_W} changed from "560" to "520" Replaced "$V_{DD\_HV\_IO\_FLEX}$" with "$V_{DD\_HV\_IO\_ETH}$" in note below the table. *Table 15 (MEDIUM configuration output buffer electrical characteristics)*: Added note to the conditions column. "4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V" replaced by "4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V" in R_{OH_M} and R_{OL_M}rows. Replaced "$V_{DD\_HV\_IO\_FLEX}$" with "$V_{DD\_HV\_IO\_ETH}$" in note below the table. Minimum values of R_{OH_M} and R_{OL_M} changed from "140" to "120" *Table 16 (STRONG configuration output buffer electrical characteristics)*: Added note to the conditions column. "4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V" replaced by "4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V" in R_{OH_S} and R_{OL_S} rows. Replaced "$V_{DD\_HV\_IO\_FLEX}$" with "$V_{DD\_HV\_IO\_ETH}$" in note below the table. Minimum values of R_{OH_S} and R_{OL_S} changed from "35" to "30" Updated the minimum values of t_{TR_S} *Table 17 (VERY STRONG configuration output buffer electrical characteristics)*: Added note to the conditions column. Updated R_{OH_V} and R_{OL_V} rows. Removed footnotes: • *Refer to FlexRay section for...* • *20–80% transition time...* Updated the minimum values of t_{TR_V} Removed "EBI output driver electrical characteristics" table. *Table 18 (I/O consumption)*: Added a footnote to the table. Removed footnote: Data based on simulation results... Updated all the condition rows of the table. *Table 19 (Reset electrical characteristics)*: Replaced minimum value of "300" with "275" in the V_{HYS} row. Replaced "0.9 V" with "1.0 V" in the in the condition column of I_{OL_R} row. Replaced minimum value of "11" with "12" in the I_{OL_R} row. Updated I_{WPU} and I_{WPD} rows. *Table 20 (PLL0 electrical characteristics)*: Added $f_{PLL0PHI1}$ and $f_{PLL0FREE}$ symbols. Replaced maximum value of "100" with "80" in the $f_{PLL0PHI0}$ row. In footnote: *PLL0IN clock retrieved...* the second sentence now reads *Input characteristics are granted when using XOSC.* In f_{PLL0IN} added a second note to parameter column. Updated maximum value of $f_{PLL0LOCK}$.

Table 55. Document revision history (continued)

Date	Revision	Changes
18-May-2015	3 (cont.)	*Table 21 (External oscillator electrical specifications)*: Updated the minimum and maximum values of f_{XTAL}. Updated V_{IHEXT}, V_{ILEXT}, g_{m}, and I_{XTAL}. Added V_{HYS}. *Table 22 (Selectable load capacitance)*: Updated the table. *Table 23 (Internal RC oscillator electrical specifications)*: Removed I_{AVDD5}, and I_{DVDD12} rows. Updated parameter column of δf_{var_SW}. *Table 24 (ADC pin specification)*: Removed I_{LK_IN} symbol. Added $V_{REF\_BG\_T}$, $V_{REF\_BG\_TC}$, and $V_{REF\_BG\_LR}$ symbols. Updated conditions column of I_{BG} symbol. Removed the table footnote “Leakage current is a....” Added ΣI_{ADR} Updated I_{LK_INUD}, I_{LK_INUSD}, I_{LK_INREF}, and I_{LK_INOUT}. Replaced maximum value of “6.5” with “8.5” for C_S. *Table 25 (SARn ADC electrical specification)*: Updated conditions, minimum, and maximum columns of V_{ALTREF}. Updated parameter, conditions, and maximum columns of $I_{ADCREFH}$. Replaced the maximum value of “1” with “+8” in $I_{ADCREFH}$ symbol (power down mode). Replaced “I_{ADCVDD}” with “I_{ADV_S}” and updated its conditions and maximum columns. Updated minimum and maximum columns of DNL. *Table 26 (SDn ADC electrical specification)*: In the f_{ADCD_M} symbol replaced “S/D clock 3” with “S/D modulator Input clock”. Added minimum value of “4”. Updated the maximum values of $\lvert\delta_{GAIN}\rvert$ Replaced the unit values of “dB” with “dBFS” in the $SNR_{DIFF150}$, $SNR_{DIFF333}$, and SNR_{SE150} symbols. Replaced the unit values of “dB” with “dBc” in SFDR symbol. Added CMRR symbol and replaced the minimum value of “20” with “54”. Added R_{Caaf} and $F_{rolloff}$ symbols. Updated the maximum values of I_{ADV_D} and ΣI_{ADR_D}. Removed ΣI_{ADR_D}. Replaced maximum value of “$2*\delta_{GROUP}$” with “δ_{GROUP}” for $t_{LATENCY}$. Replaced maximum value of “15” with “16” for GAIN. Added I_{ADCS/D_REFH}. Updated the minimum, typical and maximum values of Z_{IN}. *Table 27 (Temperature sensor electrical characteristics)*: Added rows: • *temperature monitoring range* • *temperature sensitivity (T_{SENS})* • *temperature accuracy (T_{ACC})*

Table 55. Document revision history (continued)

Date	Revision	Changes
18-May-2015	3 (cont.)	*Table 28 (LVDS pad startup and receiver electrical characteristics)*: Replaced “C” with “T” in the characteristics column of I_{LVDS_BIAS} and I_{LVDS_RX}. *Table 29 (LFAST transmitter electrical characteristics)*, and *Table 30 (MSC/DSPI LVDS transmitter electrical characteristics)*: Replaced “C” with “T” in the characteristics column of I_{LVDS_TX}. *Table 39 (Nexus debug port timing)*: Replaced “P” with “D” in the characteristics column of t_{EVTIPW} and tEVTOPW. *Figure 18 (Voltage regulator capacitance connection)*: Updated the figure. *Table 31 (Voltage regulator electrical characteristics)*: Replaced $R_{DECREGn}$ with R_{REG}. Updated the conditions column of C_{DECBV} and C_{DECHV}. Changed the classification of $I_{MREGINT}$ from “P” to “D”. Added “- at 27 ^{o}C , no load” to note 6. Added “with full load” to note 7. *Table 36 (Flash memory program and erase specifications (pending silicon characterization))*: For tESUS, replaced lifetime max value of “20” WITH “30”. For tpsus, replaced lifetime max value of “10” WITH “15”. *Table 40 (DSPI channel frequency support)*: Removed “Full duplex” from LVDS (Master mode). *Table 41 (DSPI CMOS master classic timing (full duplex and output only) – MTFE = 0, CPHA = 0 or 1)*: Updated the minimum values of t_{CSC}, t_{PCSC}, and t_{PASC} and maximum values of t_{SUO}. *Table 42 (DSPI CMOS master modified timing (full duplex and output only) – MTFE = 1, CPHA = 0 or 1)*: Updated the minimum values of t_{CSC}, t_{PCSC}, and t_{PASC} and maximum values of t_{SUO}. Removed section “DSPI LVDS Master Mode — Modified Timing.” *Table 44 (DSPI CMOS master timing – output only – timed serial bus mode TSB = 1 or ITSB = 1, CPOL = 0 or 1, continuous SCK clock)*: Updated the minimum values of t_{CSV} and maximum values of t_{SUO}. *Table 45 (DSPI CMOS Slave timing - Modified Transfer Format (MTFE = 0/1))*: Updated the minimum and maximum values of t_{DIS}. Replaced the maximum value of “50” with “55” in $t_{SUO\ (medium)}$. *Table 48 (RMII transmit signal timing)*: Replaced the maximum value of “14” with “16” for R6.

Table 55. Document revision history (continued)

Date	Revision	Changes
18-May-2015	3 (cont.)	*Section 3.17.5, GPIO delay timing*: Added this section. Replaced “four” with “three” in the table footnotes in *Table 51 (eTQFP80 – STMicroelectronics package mechanical data)* and *Table 52 (eTQFP100 – STMicroelectronics package mechanical data)*. *Table 51 (eTQFP80 – STMicroelectronics package mechanical data)*: Second note removed from E2 parameter and added to E3 parameter. *Table 53 (Thermal characteristics for eTQFP80)*: Updated the table and its values. *Table 54 (Thermal characteristics for eTQFP100)*: Updated the table and its values. *Table 60 (Order codes (ST))* Updated the table.
15-Jun-2017	4	Following are the changes in this version of the Datasheet: Replaced eLQFP100 with eTQFP100 throughout the document. Removed all requirement tagging from the document. Replaced RPNs: SPC572L64F2B, SPC572L64E3B with SPC572Lx. Replaced SPC572LxB with SPC572Lx. Replaced bullet point “On-chip voltage...” with “Single 5V +/-10%....” on the cover page. *Table 1 (Device summary)*: – Updated the table. *Table 2 (SPC572Lx device feature summary)*: – Updated the notes of “External power supplies” *Section 3.4: Electromagnetic Compatibility (EMC)*: – Updated the section. *Table 9 (Device operating conditions)*: – Updated the values of parameter $V_{DD\_LV.}$ – Updated notes in the table. Removed section: “Temperature profile.” *Table 26 (SDn ADC electrical specification)*: – Updated the values for R_{BIAS} parameter. – Added parameters $Z_{DIFF,}$ Z_{CM}, and $\Delta V_{INTCM.}$ *Table 31 (Voltage regulator electrical characteristics)*: – Added parameter C_{DECFLA} *Table 32 (Voltage monitor electrical characteristics)*: – Added parameter V_{LVD108} *Section 4.3: eTQFP100 case drawing*: – Updated the *Figure 39: eTQFP100 – STMicroelectronics package mechanical drawing*. – Updated the *Table 52 (eTQFP100 – STMicroelectronics package mechanical data)*. *Section 5: Ordering information*: – Removed table: Order codes (ST). Added *Figure 40: Product code structure*.

Table 55. Document revision history (continued)

Date	Revision	Changes
06-Jul-2017	5	Removed “ST Restricted” watermark

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