

PCN Number: MC110816 Chgnot.doc rev 13 1/14

Product/Process Change Notification (PCN)

Customer: Digi-Key

Date: 11/08/2016

Customer Part # and/or Lot# affected: A6260KLJTR-T and A6260SLJTR-T

Originator: Mark Caggiano

Phone: 603-626-2538

<u>Dur</u>	ation of Change:	Permanent X	Temporary	(explain)
<u>Sum</u>	mary description of change : Part Change:	Process Cl	hange: X	Other:
1	Allegro currently manufactures the A6260K	I ITR-T and $\Delta 626$	50SI ITR-T or	the 6" wafer

- Allegro currently manufactures the A6260KLJTR-T and A6260SLJTR-T on the 6" wafer fab ABCD4 technology line at Polar Semiconductor LLC (PSL), Bloomington, MN, USA. The 6" ABCD4 wafer fab line will be closing. Allegro will change manufacturing to the 8" ABCD4 technology wafer fab line at Polar Semiconductor LLC (PSL), Bloomington, MN, USA
- The A6260KLJTR-T and A6260SLJTR-T will change the final test location from Allegro MicroSystems, LLC Worcester, MA USA to Allegro MicroSystems (Thailand) Co., Ltd. (AMTC).

What is the part or process changing from (provide details)?

- 1. Allegro currently manufactures the A6260KLJTR-T and A6260SLJTR-T on the 6" wafer fab ABCD4 technology line at Polar Semiconductor LLC (PSL), Bloomington, MN, USA, The 6" ABCD4 wafer fab line will be closing.
- 2. The A6260KLJTR-T and A6260SLJTR-T final test location is Allegro MicroSystems, LLC, Worcester, MA USA.

What is the part or process changing to (describe the anticipated impact of this change on form, fit and/or function)?

- 1. The A6260KLJTR-T and A6260SLJTR-T will change manufacturing to the 8 inch wafer fab ABCD4 technology line at Polar Semiconductor LLC (PSL), Bloomington, MN, USA..
- 2. The A6260KLJTR-T and A6260SLJTR-T will change final test locations to Allegro MicroSystems (Thailand) Co., Ltd. (AMTC).

Allegro will be expanding its manufacturing capabilities with the addition of a new, whollyowned integrated circuit test facility located in Saraburi, Thailand. The same make and model test equipment will be utilized and test site transfer buy off data will be on file for each device before production begins.



Note: Validation of equivalence within a specific application is at the discretion of the Customer

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Is a PPAP update required?	Yes	No 🔀
T	Yes X	No (explain)
Is reliability testing required? (If Yes, refer to attached plan)		





Reliability Qualification Results

Device: 6260 (9326) Assy Lot #: 1548731UAAA Number of Leads: 8 Fab Location: PSL Package: LJ (eSOIC) Assembly Location: Unisem Lead Finish: 100% Sn Tracking Number: 3316

<u>Reason for Qualification:</u> 6260 (9326) – [6" to 8" Fab Tansfer] - Automotive, High Brightness LED, Current Regulator

Reliability Qualification Results									
6260 (9326) - STR#3316						Requirements			
Stress Test	Abv.	Test #	Test Method	Test Conditions	s.s.	Results			
Preconditioning	PC	A1	JESD22-A113 / J-STD-020	85°C/60% RH, 168 hrs, Peak Reflow=260°C; MSL3, (HAST, AC, TC)	231	0 Rejects			
HAST	HAST	A2	JESD22-A110	Ta=130°C, 85% RH, 2 ATM, 0, 96 hrs	77	0 Rejects			
Autoclave	AC	A3	JESD22-A102	Ta=121°C, 100% RH, 15 PSIG, 0, 96 hrs		0 Rejects			
Temperature Cycle	тс	A4	JESD22-A104	Ta = -65°C to +175°C, 0, 500, 1000 Cycles		0 Rejects			
Wire Bond Pull	WBP	C2	Mil-Std-883 Method 2011	Temp conditions and sample size are defined in the test method. (after TC)		0 Rejects; Cpk>1.67			
High Temperature Operating Life	HTOL	B1	JESD22-A108	Ta=125°C, 0, 1000 hrs	77	0 Rejects			
Early Life Failure Rate	ELFR	B2	AEC-Q100-008 / JESD22-A108	Ta=125°C, 0, 48 hrs	800	0 Rejects			
Electrostatic Discharge Human Body Model			ined in	Classification H2, HBM = 2.0kV					
Electrostatic Discharge Charged Device Model	CDM	E3	AEC-Q100-011	Test Conditions, Sampling Size are defined in the Test Method		Classification C6, > 1kV			
Latch-Up	LU	E4	JESD78	Test Conditions, Sampling Size are defined in the Test Method		Class II, Level A			
Electrical Distributions	ED	E5	AEC Q100-009	Tri-Temp Electrical Distributions - 30 pcs. (1 Lot)		0 Rejects; Cpk>1.67			

This device qualification is considered to be passing all environmental stress evaluations per the *Allegro MicroSystems, LLC* 900019 specification and AEC-Q100.

Approved by:

Beb Domero

Bob Demers Product Safety and Reliability Allegro MicroSystems, LLC

Allegro MicroSystems, LLC

Proprietary

Expected completion date for internal qualification: Complete

Expected PPAP availability date: N/A

Target implementation date: May 2017



Estimated date of first shipment: June 2017

Expected sample availability date: Available Upon Request



Please note: It is our intention to inform our customer of changes as early as possible. Under Allegro's procedure for product/process change notification, Allegro strives, based on its technical judgment, to provide notification of significant changes that may affect form, fit or function. However, as Allegro cannot ensure evaluation of product/process changes for each and every application; the customer retains responsibility to validate the impact of a change on its application suitability. If samples are needed for validation of a change, requests may be made via the contact information provided herein. Please contact your Account Manager or local Sales contact for any questions. We would kindly request your consideration so we can meet our target date for implementation. Unless both parties agree to extend the implementation date, this change will be implemented as scheduled.

Customer comments/Conditions of Acceptance:

Approved by: Date: cc: Allegro Sales/Marketing/Quality

Title: