



BUK9C10-55BIT

N-channel TrenchPLUS logic level FET

25 August 2014

Product data sheet

1. General description

Logic level N-channel MOSFET in a D2PAK-7 package using TrenchPLUS MOSFET technology. The device includes TrenchPLUS current sensing and integrated diodes for temperature sensing. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

2. Features and benefits

- AEC-Q101 Compliant
- Enables temperature monitoring due to integrated temperature sensor
- Enables current sense measurement due to integrated current senseFET
- Suitable for thermally demanding environments due to 175 °C rating

3. Applications

- 12 V Automotive systems
- Motors, lamps and solenoid control
- Powertrain, chassis and body applications

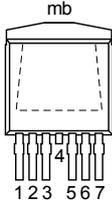
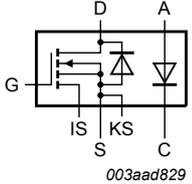
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
R _{DSon}	drain-source on-state resistance	V _{GS} = 5 V; I _D = 10 A; T _j = 25 °C; Fig. 16 ; Fig. 17	-	8.2	10	mΩ
		V _{GS} = 10 V; I _D = 10 A; T _j = 25 °C; Fig. 16 ; Fig. 17	-	7.5	9	mΩ
I _D /I _{sense}	ratio of drain current to sense current	-55 °C < T _j < 175 °C; V _{GS} = 5 V; Fig. 18	10000	11000	12000	A/A
S _{F(TSD)}	temperature sense diode temperature coefficient	I _F = 250 μA; -55 °C ≤ T _j ≤ 175 °C; Fig. 19	-5.7	-6	-6.3	mV/K
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 25 mA; V _{GS} = 0 V; T _j = 25 °C	55	-	-	V
V _{F(TSD)}	temperature sense diode forward voltage	I _F = 250 μA; T _j = 25 °C; Fig. 19	2.855	2.9	2.945	V

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>D2PAK-7 (SOT427)</p>	 <p>003aad829</p>
2	IS	current sense		
3	A	anode		
4	D[1]	drain		
5	C	cathode		
6	KS	Kelvin source		
7	S	source		
mb	D	mounting base		

[1] It is not possible to connect to pin 4 of the SOT427 package

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9C10-55BIT	D2PAK-7	Plastic single-ended surface-mounted package (D2PAK-7); 7 leads (one lead cropped)	SOT427

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9C10-55BIT	28083 576

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	55	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$; $25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	55	V
V_{GS}	gate-source voltage		-15	15	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	194	W
I_D	drain current	$V_{GS} = 5\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2; Fig. 3	[1]	75	A
		$V_{GS} = 5\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 2		65	A

Symbol	Parameter	Conditions	Min	Max	Unit
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\ \mu\text{s}$; Fig. 3	-	401	A
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
$V_{isol(FET-TSD)}$	FET to temperature sense diode isolation voltage		-	100	V
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 75\text{ A}$; $V_{sup} \leq 55\text{ V}$; $V_{GS} = 5\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped; Fig. 4	[2][3][4]	-	215 mJ
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ °C}$	[1]	-	75 A
I_{SM}	peak source current	pulsed; $t_p \leq 10\ \mu\text{s}$; $T_{mb} = 25\text{ °C}$		-	401 A
Electrostatic discharge					
V_{ESD}	electrostatic discharge voltage	HBM; C = 100 pF; R = 1.5 kΩ; all pins		-	0.1 kV
		HBM; C = 100 pF; R = 1.5 kΩ; pin 4 to pin 7		-	4 kV

- [1] Current is limited by package
- [2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [3] Refer to application note AN10273 for further information.
- [4] Repetitive rating defined in avalanche rating figure.

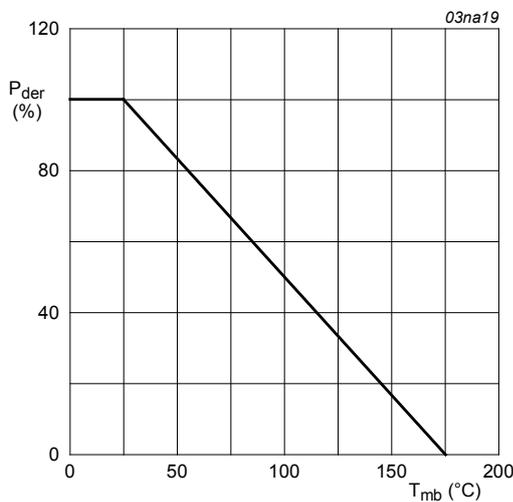
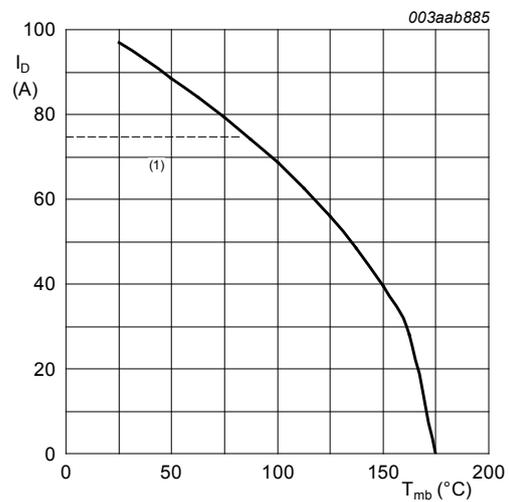


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25\text{°C})}} \times 100\%$$



(1) Capped at 75A due to package

Fig. 2. Continuous drain current as a function of mounting base temperature

$$V_{GS} \geq 5V$$

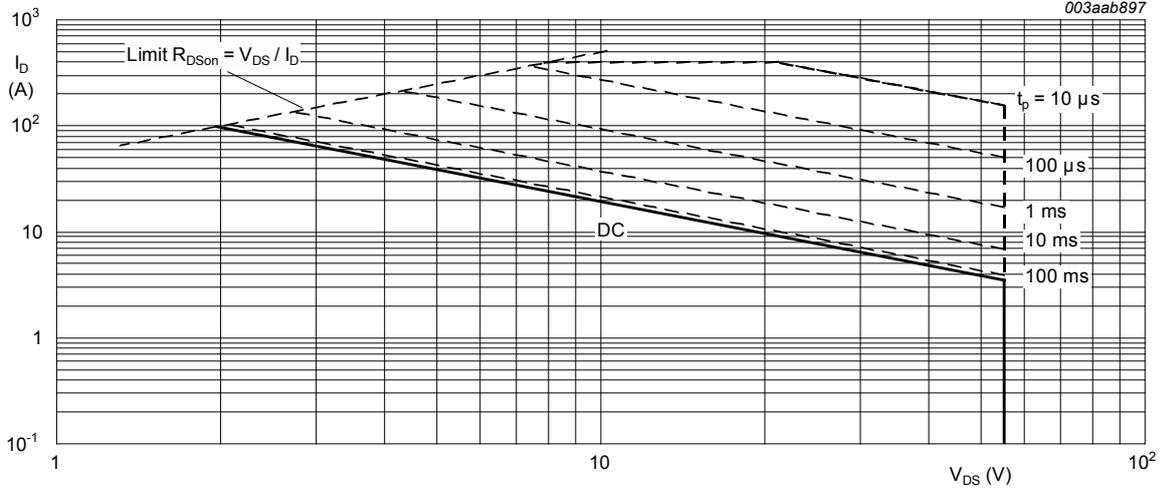


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^{\circ}\text{C}$; I_{DM} is a single pulse

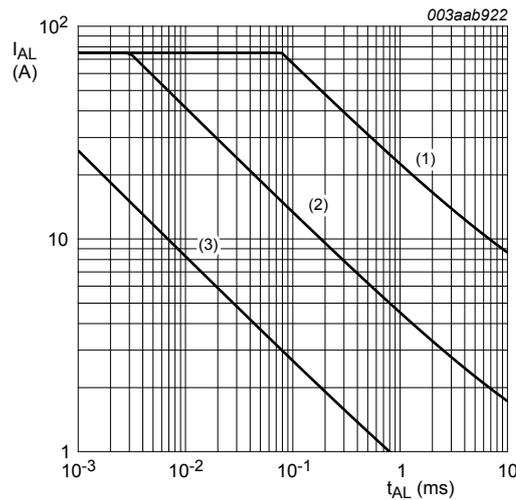


Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

(1) $T_{j (limit)} = 25^{\circ}\text{C}$; (2) $T_{j (limit)} = 125^{\circ}\text{C}$; (3) Repetitive Avalanche

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	0.46	0.78	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on printed circuit board; Fig. 6 ; Fig. 7 ; Fig. 8 ; Fig. 9	-	61.4	-	K/W

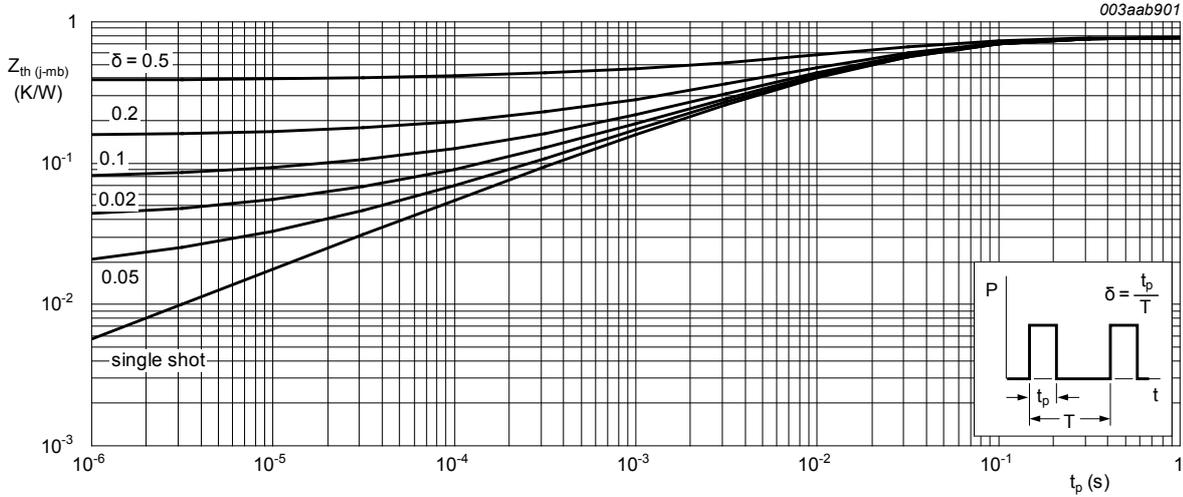
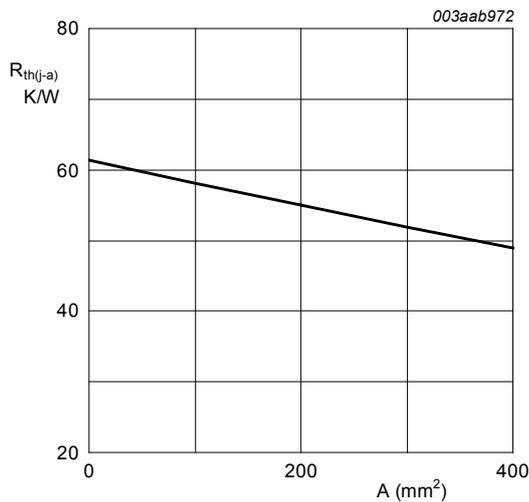


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration



Zero airflow

Fig. 6. Thermal resistance from junction to ambient as a function of printed-circuit board (PCB) heat sink area

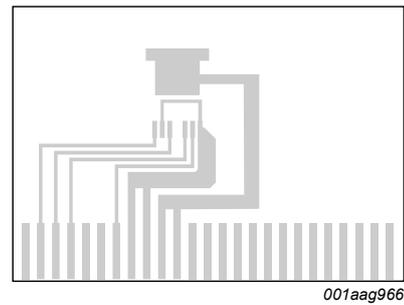


Fig. 7. PCB used for thermal tests; zero heat sink area

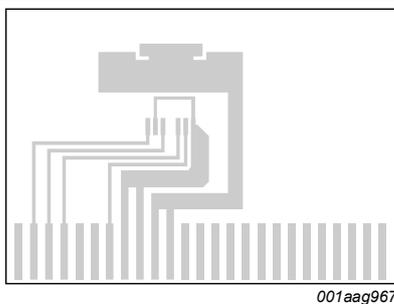


Fig. 8. PCB used for thermal tests; heat sink area 200 mm²

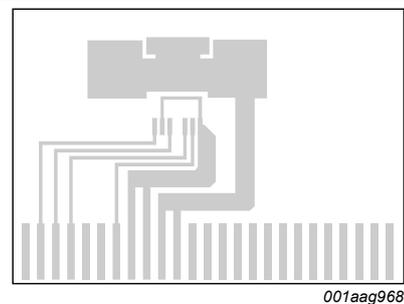


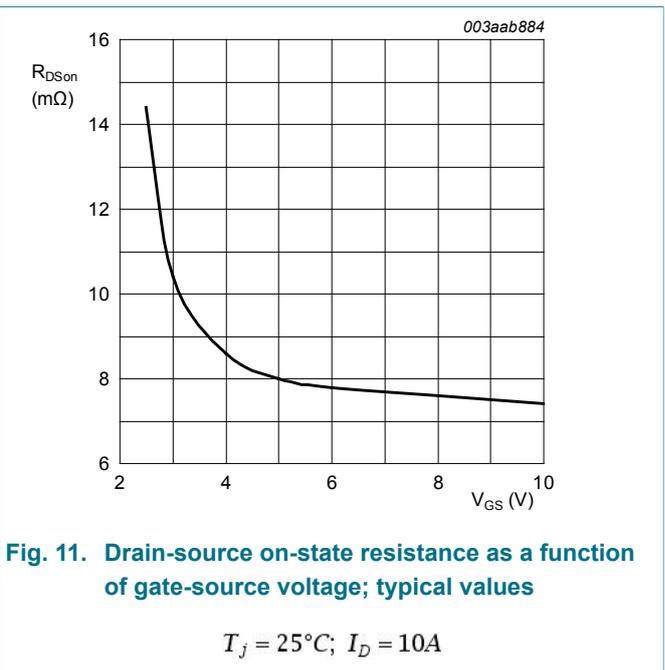
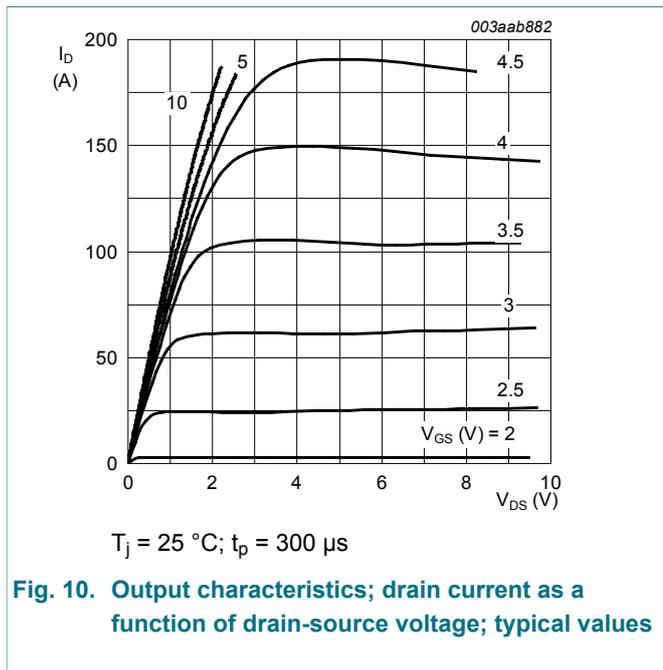
Fig. 9. PCB used for thermal tests; heat sink area 400 mm²

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	50	-	-	V
		$I_D = 25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	55	-	-	V
		$I_D = 250 \text{ } \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	47	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 14 ; Fig. 15	1.1	1.5	2	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ\text{C};$ Fig. 14	0.5	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ Fig. 14	-	-	2.3	V
I_{DSS}	drain leakage current	$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.02	1	μA
		$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ\text{C}$	-	-	125	μA
I_{GSS}	gate leakage current	$V_{DS} = 0 \text{ V}; V_{GS} = -15 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
		$V_{DS} = 0 \text{ V}; V_{GS} = 15 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 16 ; Fig. 17	-	8.4	15	m Ω
		$V_{GS} = 5 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 16 ; Fig. 17	-	8.2	10	m Ω
		$V_{GS} = 5 \text{ V}; I_D = 10 \text{ A}; T_j = 175 \text{ }^\circ\text{C};$ Fig. 16 ; Fig. 17	-	-	20	m Ω
		$V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 16 ; Fig. 17	-	7.5	9	m Ω
I_D/I_{sense}	ratio of drain current to sense current	$V_{GS} = 5 \text{ V}; -55 \text{ }^\circ\text{C} < T_j < 175 \text{ }^\circ\text{C};$ Fig. 18	10000	11000	12000	A/A
$S_{F(TSD)}$	temperature sense diode temperature coefficient	$I_F = 250 \text{ } \mu\text{A}; -55 \text{ }^\circ\text{C} \leq T_j \leq 175 \text{ }^\circ\text{C};$ Fig. 19	-5.7	-6	-6.3	mV/K
$V_{F(TSD)}$	temperature sense diode forward voltage	$I_F = 250 \text{ } \mu\text{A}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 19	2.855	2.9	2.945	V
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 10 \text{ A}; V_{DS} = 44 \text{ V}; V_{GS} = 5 \text{ V};$ Fig. 20	-	51	-	nC
Q_{GS}	gate-source charge		-	8	-	nC
Q_{GD}	gate-drain charge		-	17	-	nC
C_{iss}	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$	-	3500	4667	pF
C_{oss}	output capacitance	$T_j = 25 \text{ }^\circ\text{C};$ Fig. 21	-	526.7	635	pF

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{rSS}	reverse transfer capacitance		-	246.2	348	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30\text{ V}; R_L = 3\ \Omega; V_{GS} = 5\text{ V}; R_{G(ext)} = 10\ \Omega$	-	80	-	ns
t_r	rise time		-	32	-	ns
$t_{d(off)}$	turn-off delay time		-	100	-	ns
t_f	fall time		-	170	-	ns
L_D	internal drain inductance	from pin to center of die	-	0.85	-	nH
L_S	internal source inductance	from source lead to source bonding pad	-	1.9	-	nH
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 10\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C}; \text{Fig. 22}$	-	0.85	1.2	V
t_{rr}	reverse recovery time	$I_S = 5\text{ A}; dI_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = -10\text{ V}; V_{DS} = 30\text{ V}$	-	65.5	-	ns
Q_r	recovered charge		-	122	-	nC



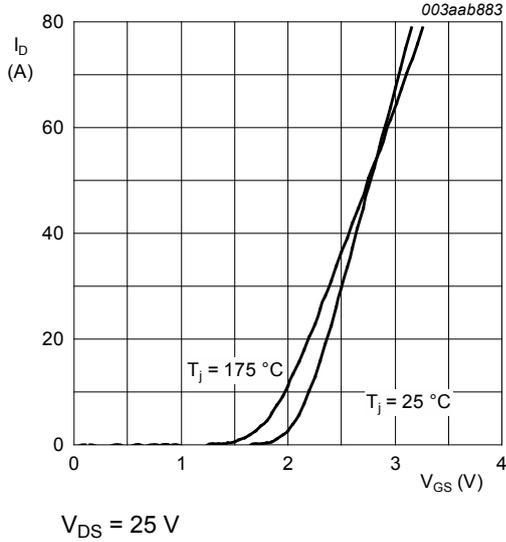


Fig. 12. Transfer characteristics; drain current as a function of gate-source voltage; typical values

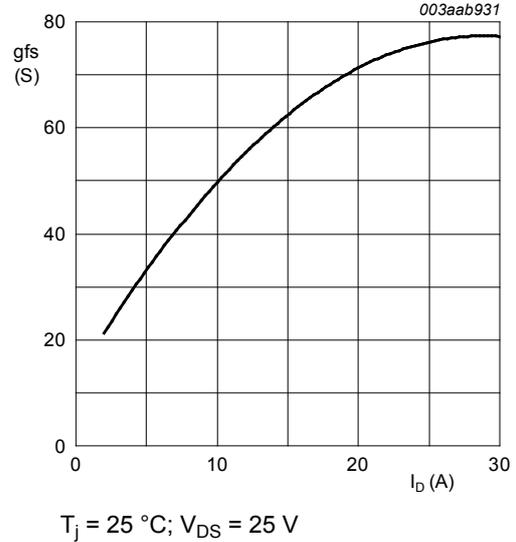


Fig. 13. Forward transconductance as a function of drain current; typical values

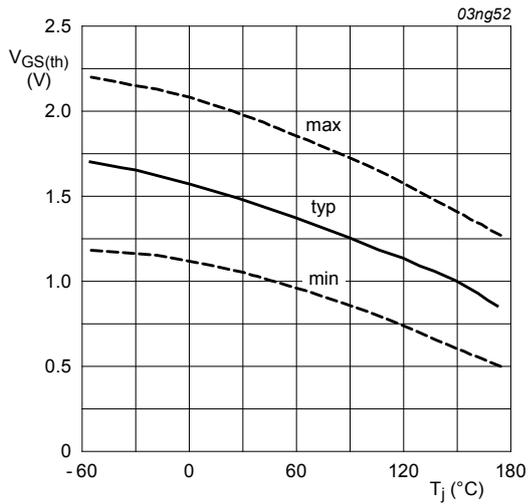


Fig. 14. Gate-source threshold voltage as a function of junction temperature

$$I_D = 1\text{ mA}; V_{DS} = V_{GS}$$

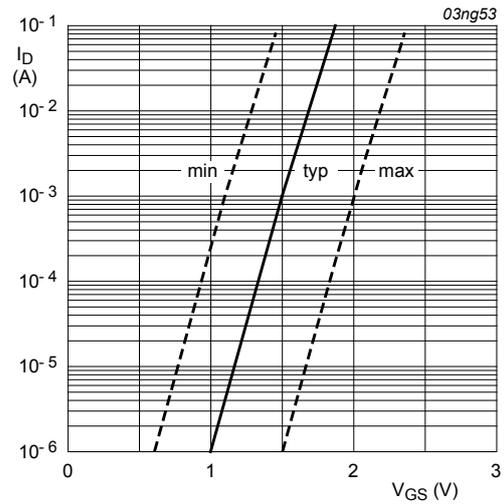


Fig. 15. Sub-threshold drain current as a function of gate-source voltage

$$T_j = 25\text{ }^\circ\text{C}; V_{DS} = V_{GS}$$

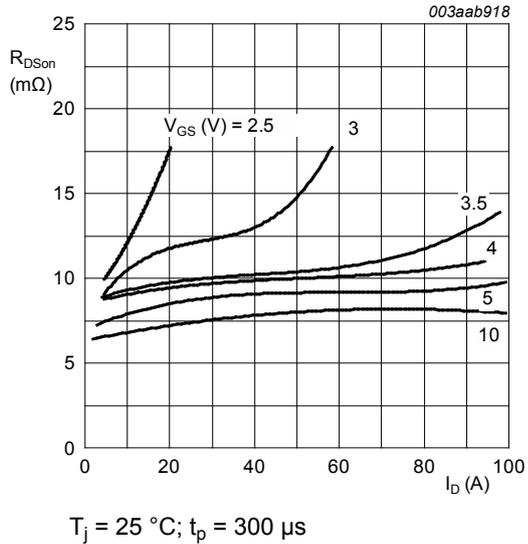


Fig. 16. Drain-source on-state resistance as a function of drain current; typical values

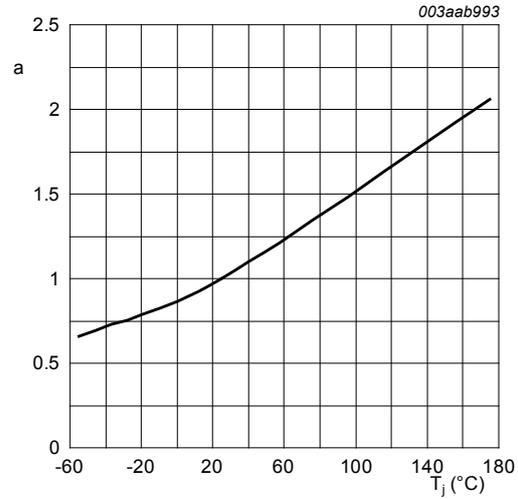


Fig. 17. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

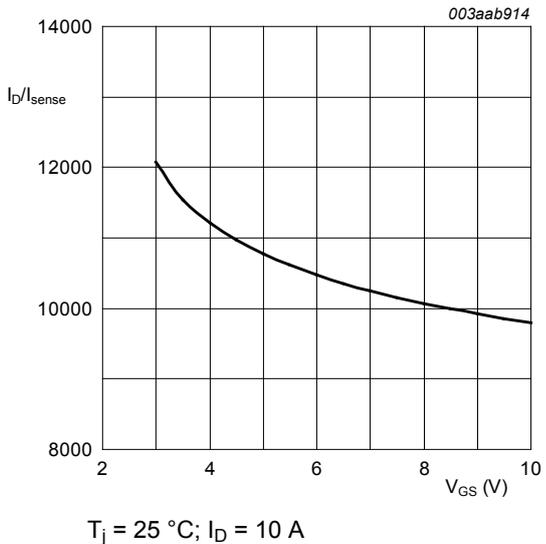


Fig. 18. Ratio of drain current to sense current as a function of gate-source voltage; typical values

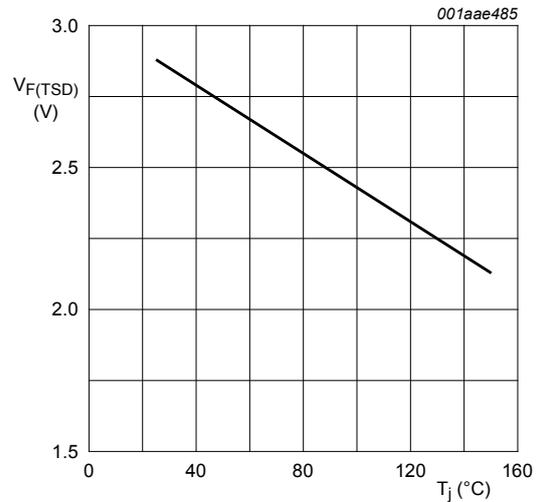
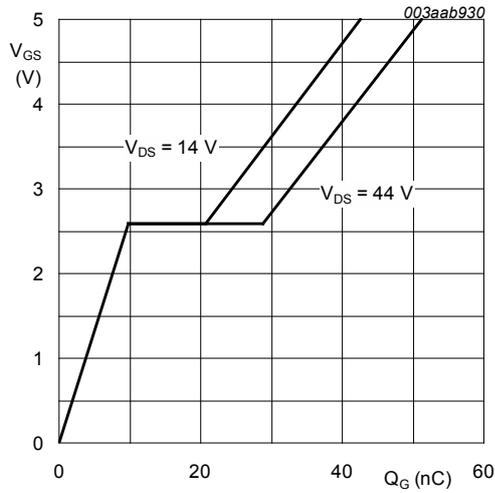


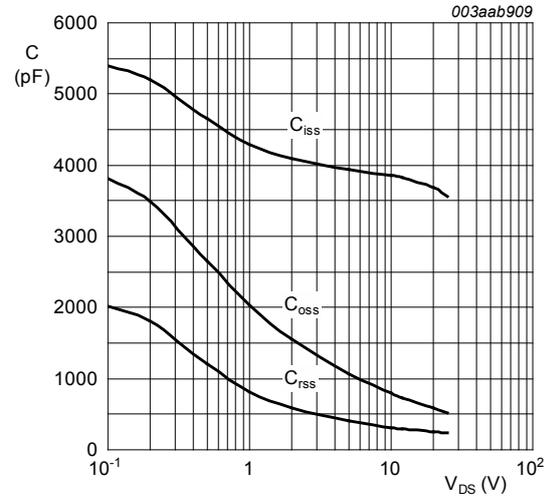
Fig. 19. Temperature sense diode forward voltage as a function of junction temperature; typical values

$$I_F = 250\text{ }\mu\text{A}$$



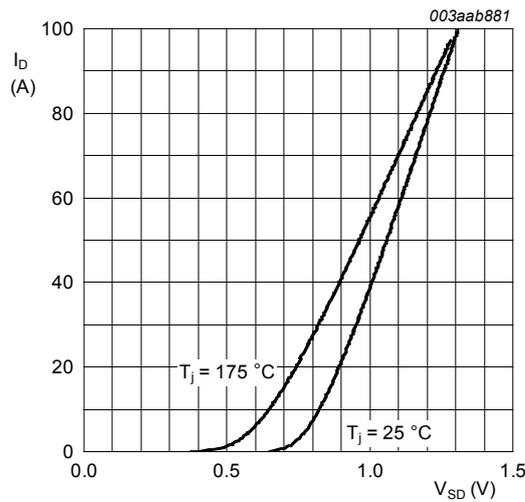
$T_j = 25\text{ °C}; I_D = 10\text{ A}$

Fig. 20. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

Fig. 21. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

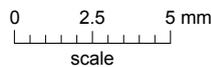
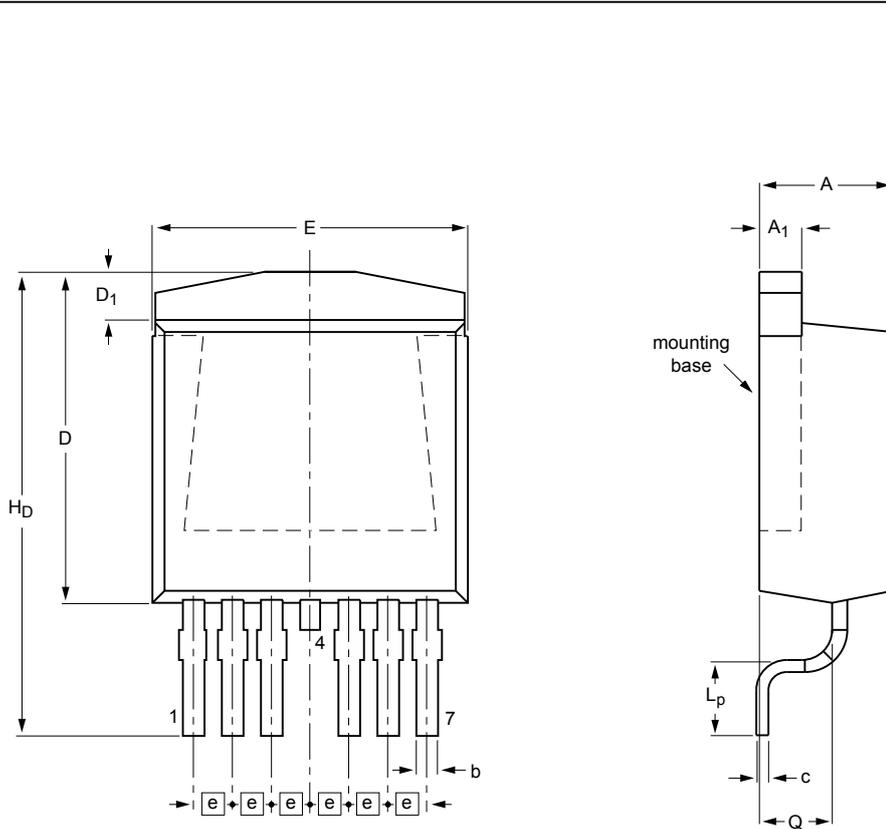


$V_{GS} = 0\text{ V}$

Fig. 22. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

11. Package outline

Plastic single-ended surface-mounted package (D2PAK-7); 7 leads (one lead cropped) SOT427



Dimensions (mm are the original dimensions)

Unit ⁽¹⁾	A	A ₁	b	c	D	D ₁	E	e	L _p	H _D	Q
max	4.5	1.40	0.85	0.64	11	1.6	10.3	1.27	2.90	15.8	2.6
nom											
min	4.1	1.27	0.60	0.46		1.2	9.7		2.10	14.8	2.2

sot427_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT427						-06-03-16- 12-10-16

Fig. 23. Package outline D2PAK-7 (SOT427)

12. Legal information

12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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13. Contents

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For sales office addresses, please send an email to: salesaddresses@nexperia.com
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