



BGU8063

low-noise high-linearity amplifier

Rev. 3.1 — 10 February 2021

Product data sheet

1 General description

The BGU8063 also known as the BTS3001H, is a high-linearity bypass amplifier for wireless infrastructure applications, equipped with fast shutdown to support TDD systems. The LNA has a high input and output return loss and is designed to operate between 2.5 GHz and 5 GHz. It is housed in a 3 mm x 3 mm x 0.85 mm with 10 terminals, in a plastic thin small outline package. The LNA is ESD protected on all terminals.

2 Features and benefits

- Low noise performance: $NF = 1.4$ dB
- High-linearity performance: $IP3_o = 34$ dBm
- High-input return loss > 10 dB
- High-output return loss > 10 dB
- Unconditionally stable up to 20 GHz
- Small 10-terminal leadless package 3 mm x 3 mm x 0.85 mm
- ESD protection on all terminals
- Moisture sensitivity level 1
- Fast shut down to support TDD systems
- +5 V single supply

3 Applications

- Wireless infrastructure
- Low noise and high-linearity applications
- LTE, W-CDMA, CDMA, GSM
- General-purpose wireless applications
- TDD or FDD systems
- Suitable for small cells



4 Quick reference data

Table 1. Quick reference data

$f = 2500\text{ MHz}$; $V_{CC} = 5\text{ V}$; $T_{amb} = 25\text{ °C}$; input and output $50\ \Omega$; unless otherwise specified. All RF parameters are measured on an application board with the circuit as shown in [Figure 29](#) and components listed in [Table 9](#) implemented. This board is optimized for $f = 2500\text{ MHz}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}	supply current	LNA enable; bypass off	-	75	90	mA
		LNA disable; bypass on	-	3	5	mA
G_{ass}	associated gain	LNA enable; bypass off	17	18.5	20	dB
		LNA disable; bypass on	-2.2	-1.8	-	dB
NF	noise figure	LNA enable; bypass off	^[1] -	1.4	2.2	dB
$P_{L(1dB)}$	output power at 1 dB gain compression	LNA enable; bypass off	17.5	19	-	dBm
$IP3_O$	output third-order intercept point	2-tone; tone spacing = 1 MHz; $P_L = 5\text{ dBm}$ per tone				
		LNA enable; bypass off	31	34	-	dBm
		LNA disable; bypass on	-	43	-	dBm

[1] Connector and Printed-Circuit Board (PCB) losses have been de-embedded.

5 Ordering information

Table 2. Ordering information

Type number	orderable part number	Package		Version
		Name	Description	
BGU8063	BGU8063J	HVSON10	plastic thermal enhanced very thin small outline package; no leads; 10 terminals; body 3 mm x 3 mm x 0.85 mm	SOT650-1

6 Block diagram

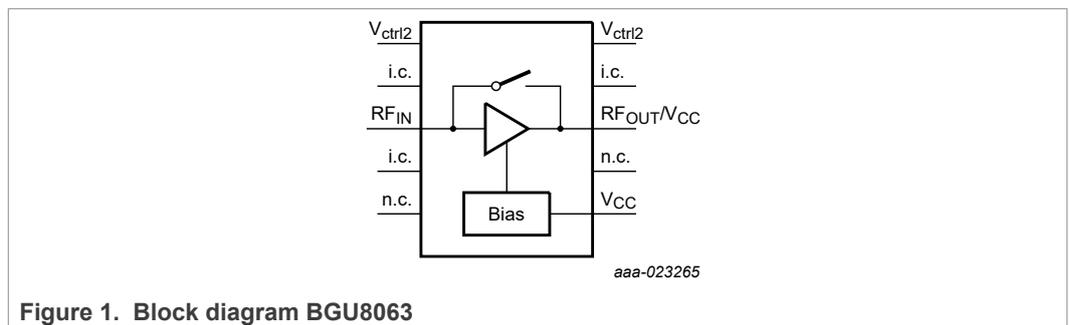


Figure 1. Block diagram BGU8063

7 Pinning information

7.1 Pinning

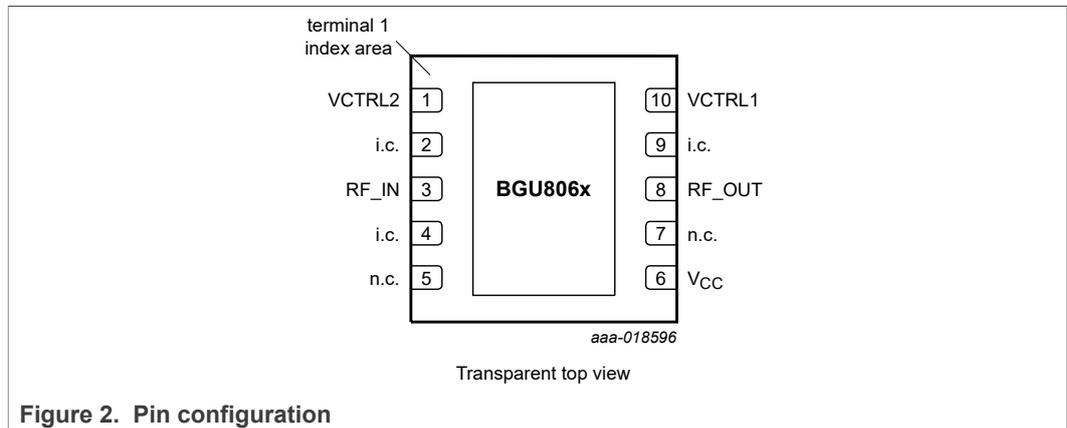


Figure 2. Pin configuration

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
VCTRL2	1	voltage control 2
i.c.	2, 4, 9	internally connected, can be grounded or left open in the application
RF_IN	3	RF input
n.c.	5	not connected
VCC	6	supply voltage
n.c.	7	not connected
RF_OUT	8	RF output
VCTRL1	10	voltage control 1
GND	exposed die pad	ground

8 Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-	6	V
$V_{i(CTRL1)}$	input voltage on pin CTRL1		-	3.6	V
$V_{i(CTRL2)}$	input voltage on pin CTRL2		-	3.6	V
$P_{i(RF)CW}$	continuous waveform RF input power		-	20	dBm
T_{stg}	storage temperature		-40	150	°C
T_j	junction temperature		-	150	°C
P	power dissipation	$T_{case} \leq 125$ °C	[1] -	510	mW
V_{ESD}	electrostatic discharge voltage	Human Body Model (HBM) according to ANSI/ESDA/JEDEC standard JS-001-2010	-	2	kV
		Charged Device Model (CDM); according to JEDEC standard 22-C101B	-	1	kV

[1] Case is ground solder pad.

9 Recommended operating conditions

Table 5. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.75	5	5.25	V
Z_0	characteristic impedance		-	50	-	Ω

10 Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-case)}$	thermal resistance from junction to case		[1] [2] 55	K/W

[1] Case is ground solder pad.

[2] Thermal resistance measured using infrared measurement technique, device mounted on application board and placed in still air.

11 Functional description

Table 7. Control truth table

$V_{CC} = 5$ V; $T_{amb} = 25$ °C.

Control signal setting [1]		Mode of operation	
CTRL1	CTRL2	LNA	bypass
LOW	HIGH	disable	on
HIGH	HIGH	disable	on
LOW	LOW	enable	off
HIGH	LOW	disable	off

[1] A logic LOW is the result of an input voltage on that specific pin between -0.3 V and 0.7 V

A logic HIGH is the result of an input voltage on the specific pin between 1.2 V and 3.6 V

12 Characteristics

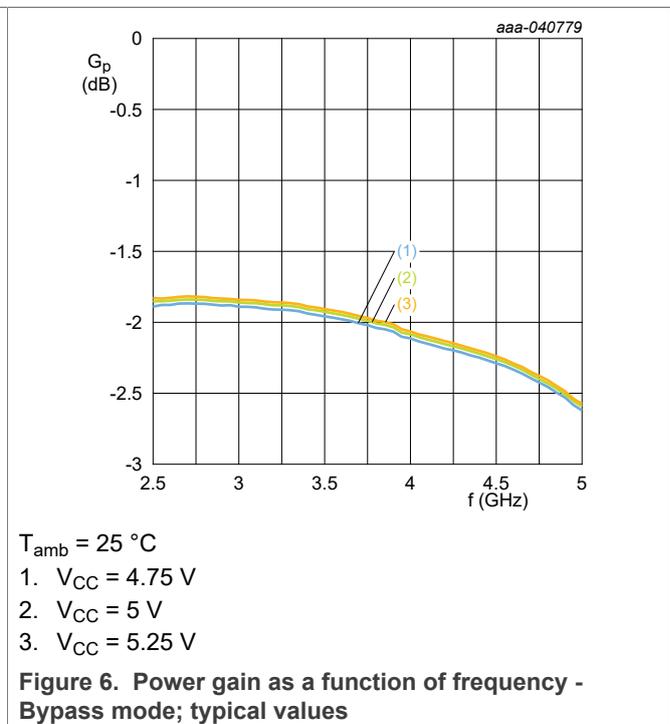
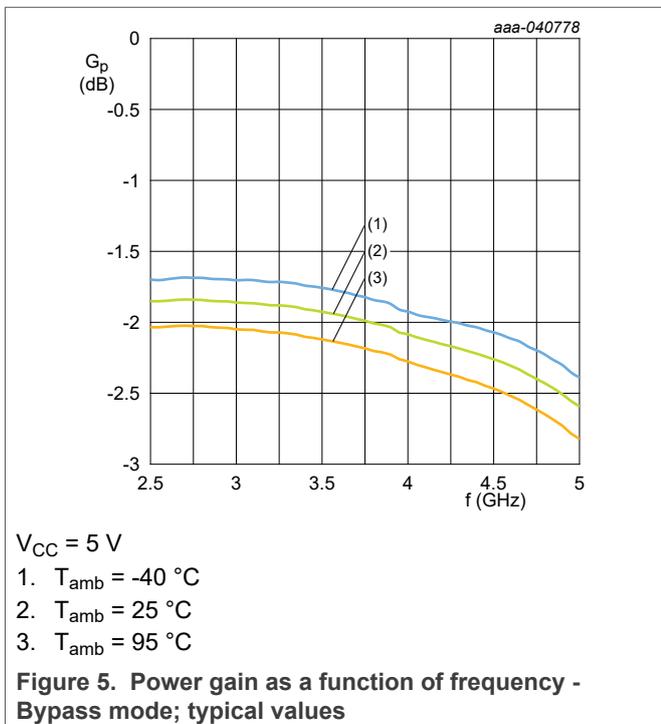
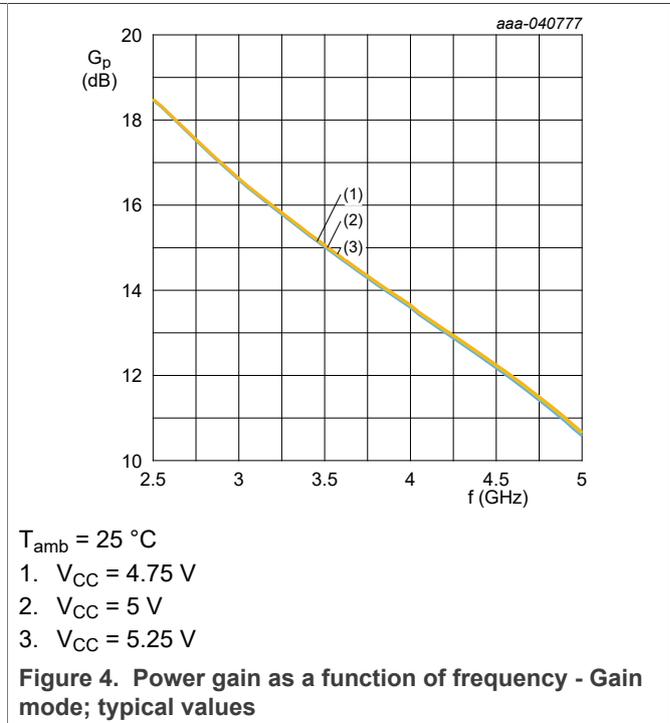
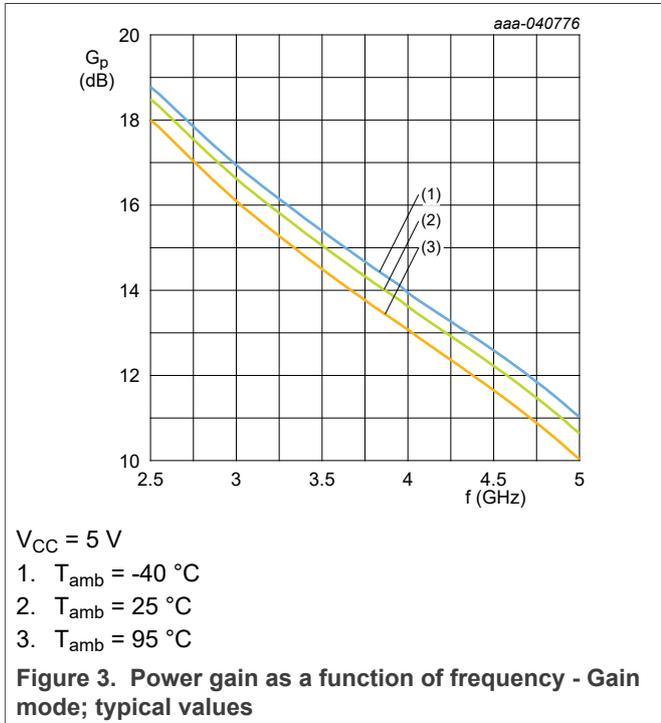
Table 8. Characteristics

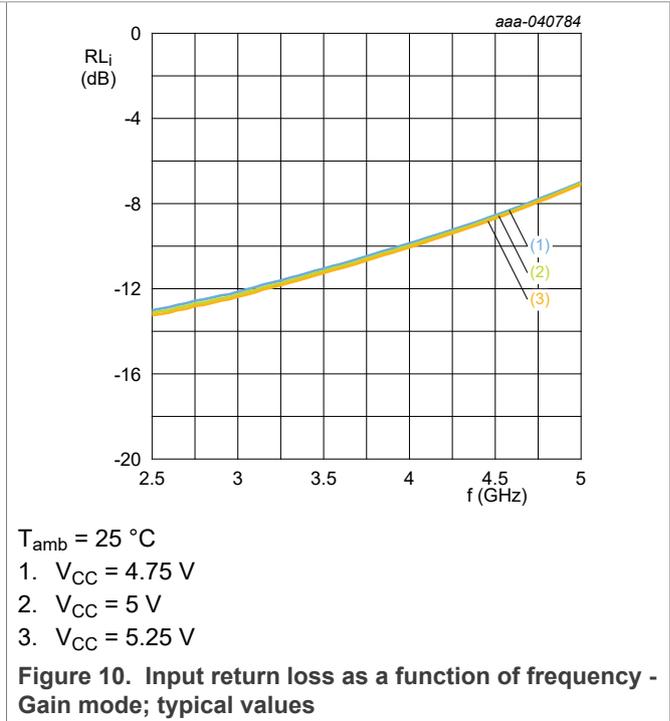
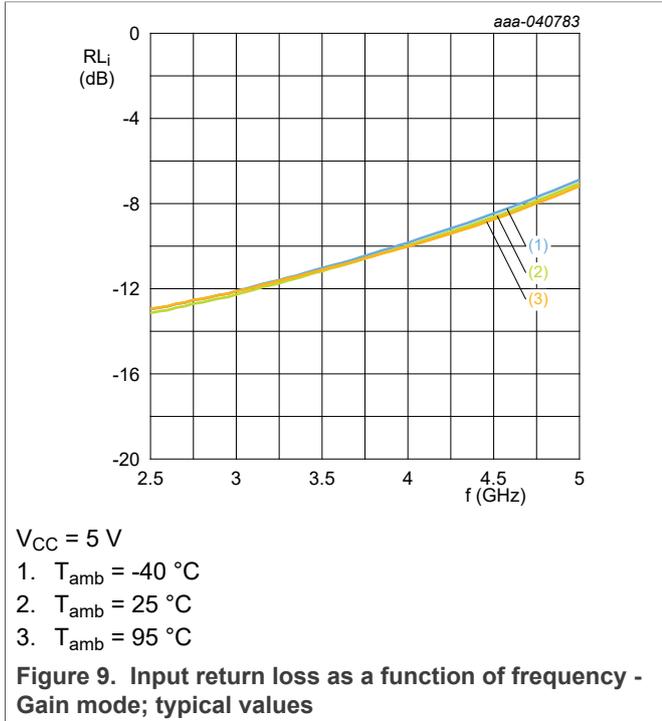
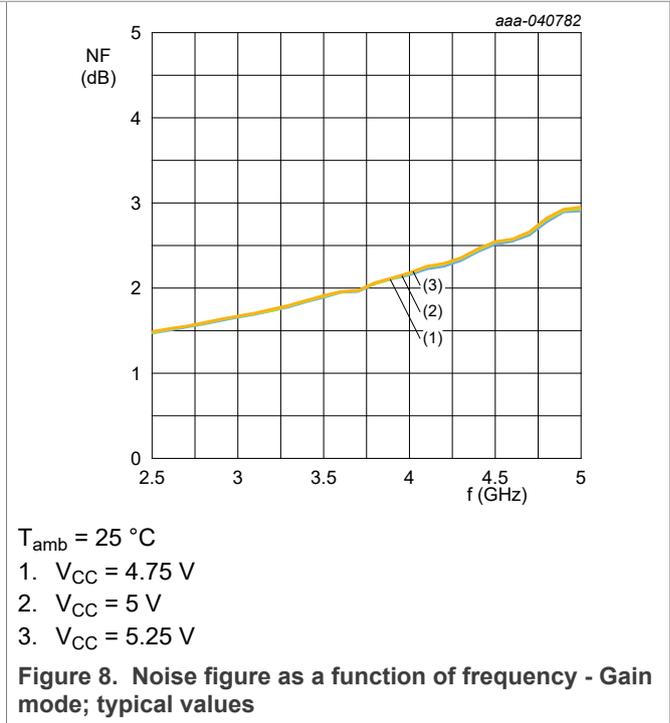
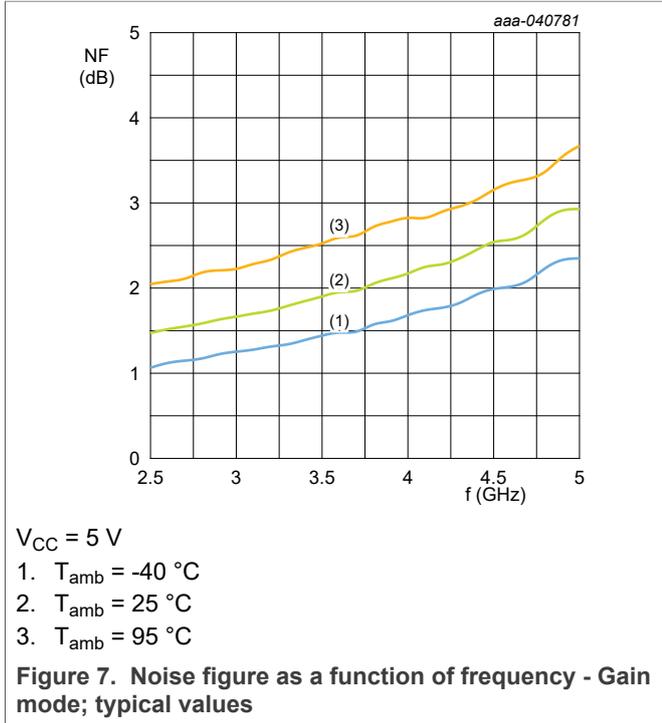
$f = 2500$ MHz; $V_{CC} = 5$ V; $T_{amb} = 25$ °C; input and output 50Ω ; unless otherwise specified. All RF parameters are measured on an application board with the circuit as shown in [Figure 29](#) and components listed in [Table 9](#) implemented. This board is optimized for $f = 2500$ MHz.

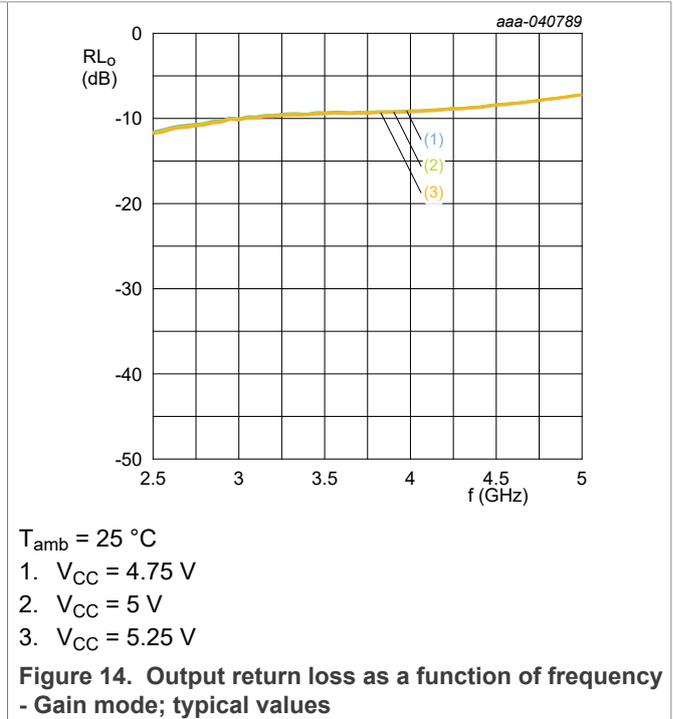
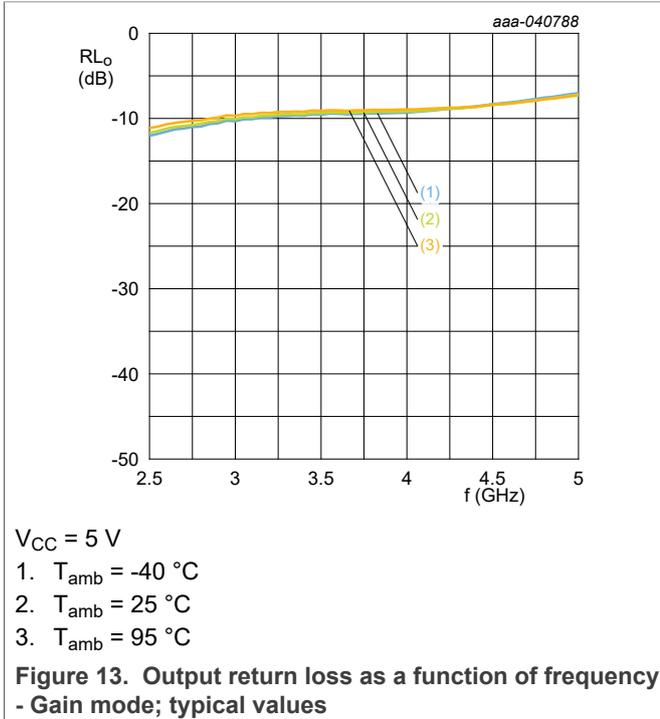
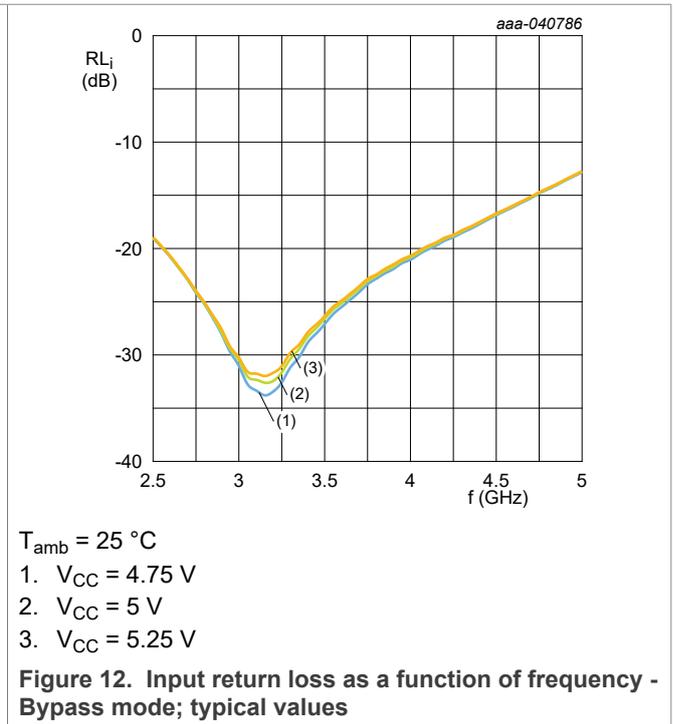
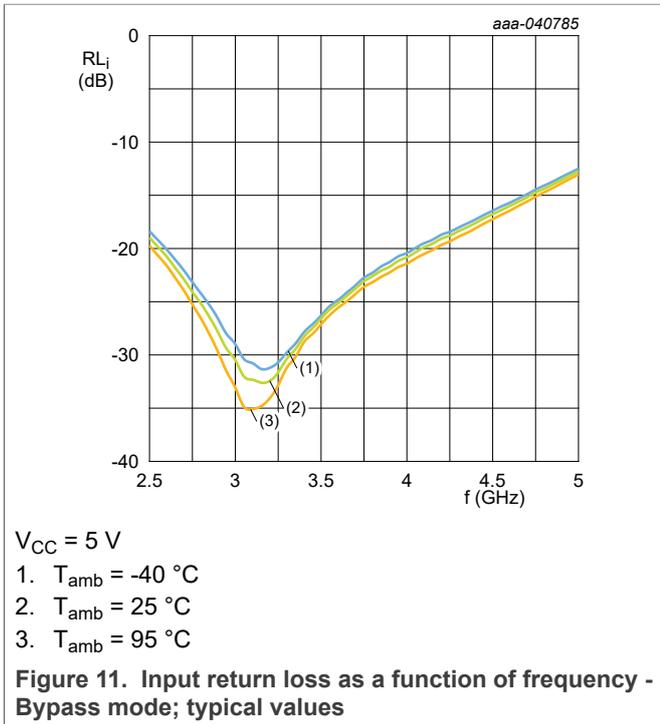
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		LNA disable; bypass on	-	3	5	mA
G_{ass}	associated gain	LNA enable; bypass off	17	18.5	20	dB
		LNA disable; bypass on	-2.2	-1.8	-	dB
G_{flat}	gain flatness	within 100 MHz bandwidth; LNA enable; bypass off				
		$2500 \text{ MHz} \leq f \leq 4000 \text{ MHz}$	-	0.4	-	dB
		$3000 \text{ MHz} \leq f \leq 3500 \text{ MHz}$	-	0.3	-	dB
NF	noise figure	LNA enable; bypass off	^[1] -	1.4	2.2	dB
ΔG	gain variation	$2500 \text{ MHz} \leq f \leq 4000 \text{ MHz}$	-	4.9	-	dB
$P_{L(1dB)}$	output power at 1 dB gain compression	LNA enable; bypass off	17.5	19	-	dBm
IP_{3O}	output third-order intercept point	2-tone; tone spacing = 1 MHz; $P_L = 5$ dBm per tone				
		LNA enable; bypass off	31	34	-	dBm
		LNA disable; bypass on	-	43	-	dBm
RL_{in}	input return loss	LNA enable; bypass off	-	-10	-	dB
		LNA disable; bypass on	-	-20	-	dB
RL_{out}	output return loss	LNA enable; bypass off	-	-10	-	dB
		LNA disable; bypass on	-	-20	-	dB
ISL	isolation	LNA disable; bypass off	-	30	-	dB
		LNA enable; bypass off	-	25	-	dB
$t_{s(pon)}$	power-on settling time	$P_i = -20$ dBm	-	0.5	-	μ s
$t_{s(poff)}$	power-off settling time	$P_i = -20$ dBm	-	0.1	-	μ s
K	Rollett stability factor	both ON-state and OFF-state up to $f = 20$ GHz	1	-	-	-

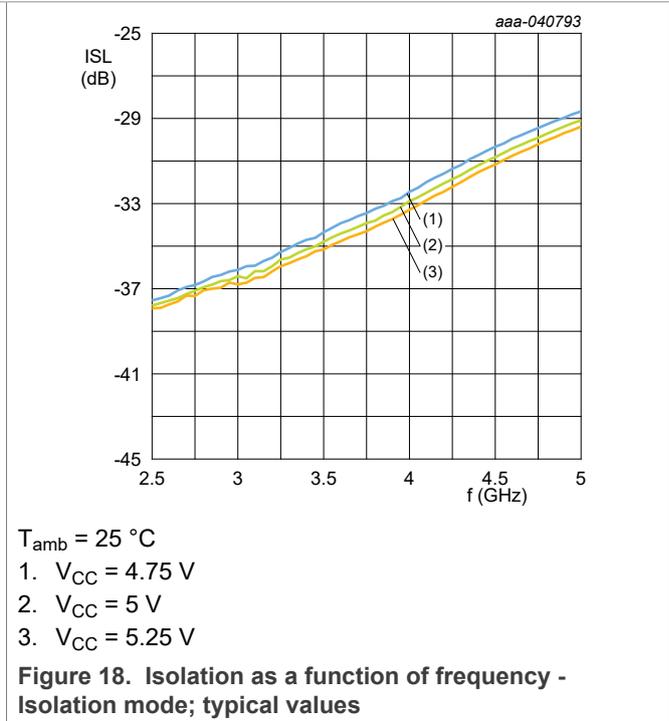
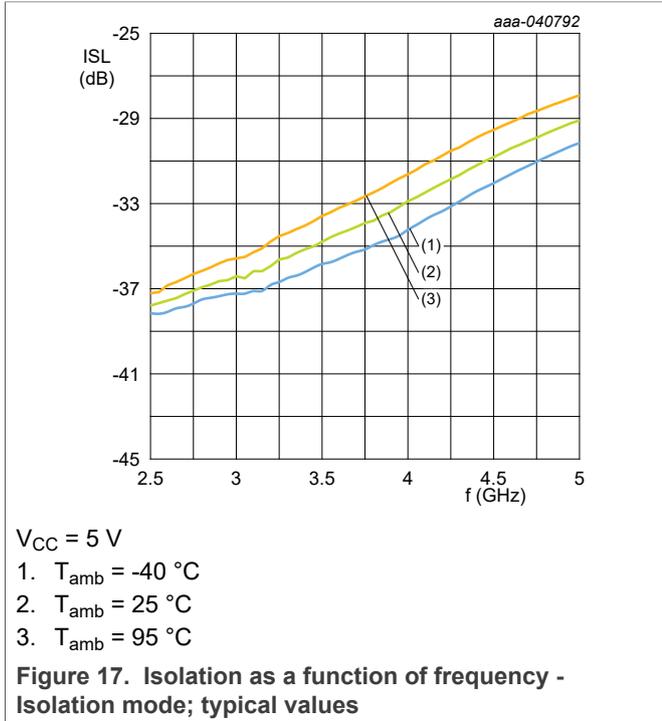
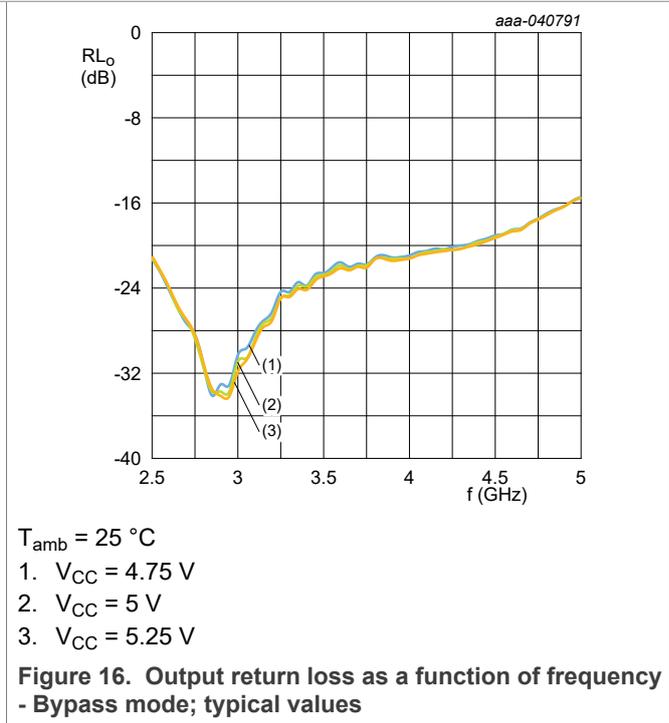
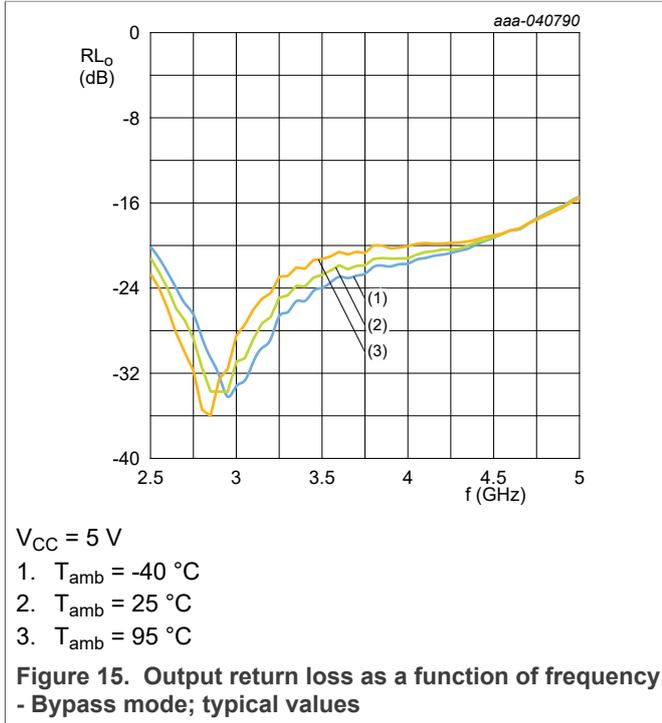
[1] Connector and Printed-Circuit Board (PCB) losses have been de-embedded.

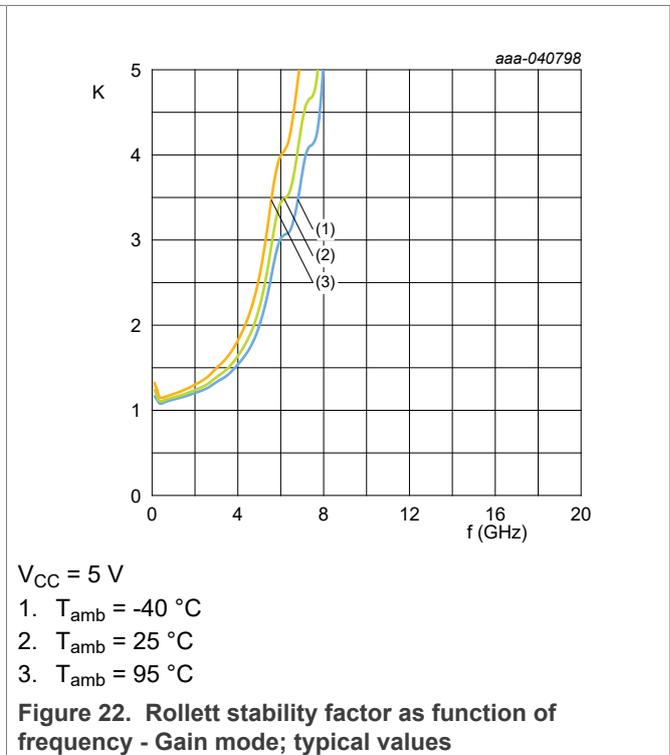
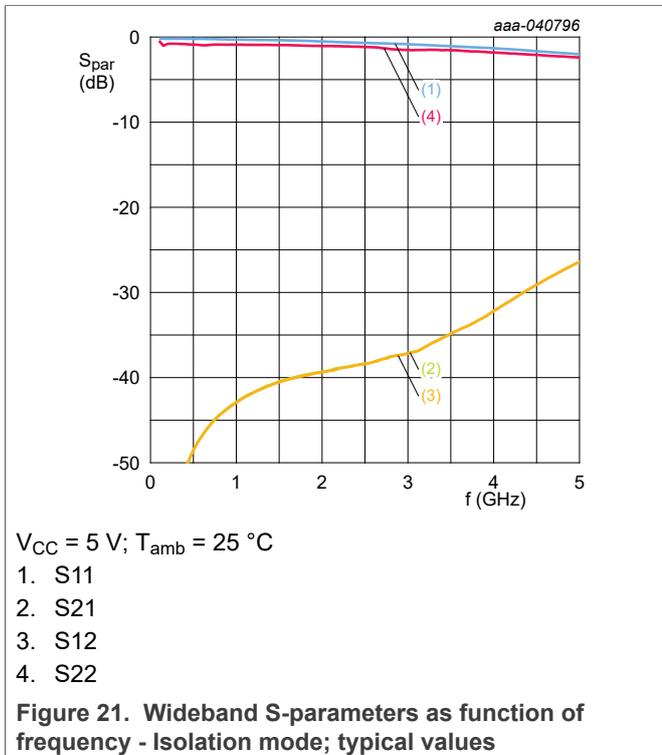
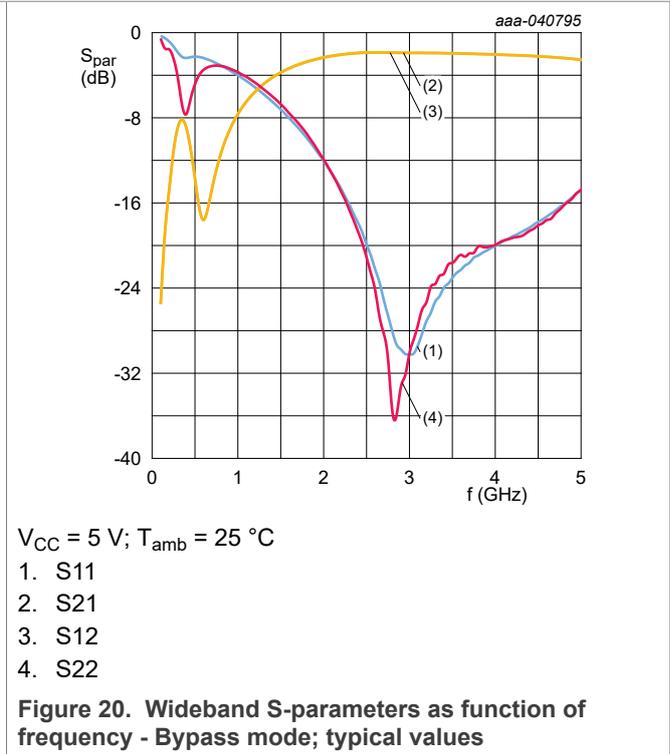
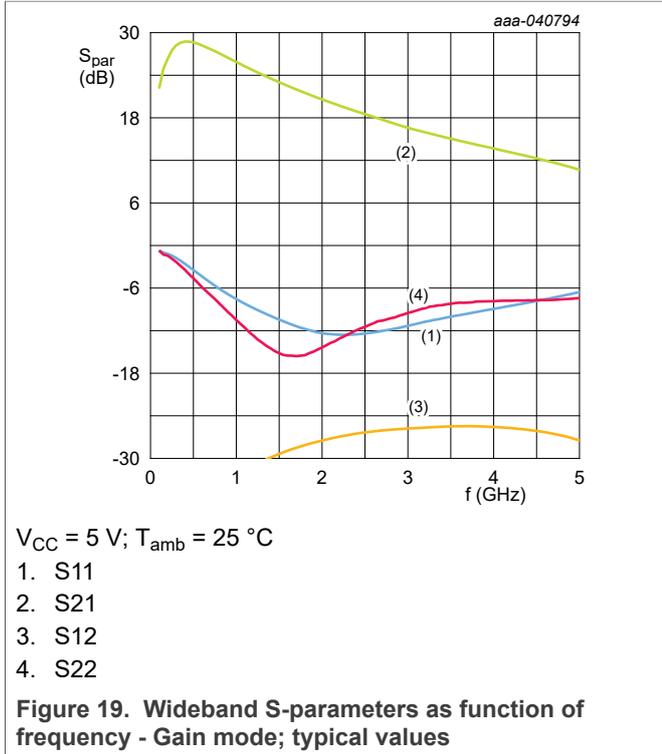
13 Graphics

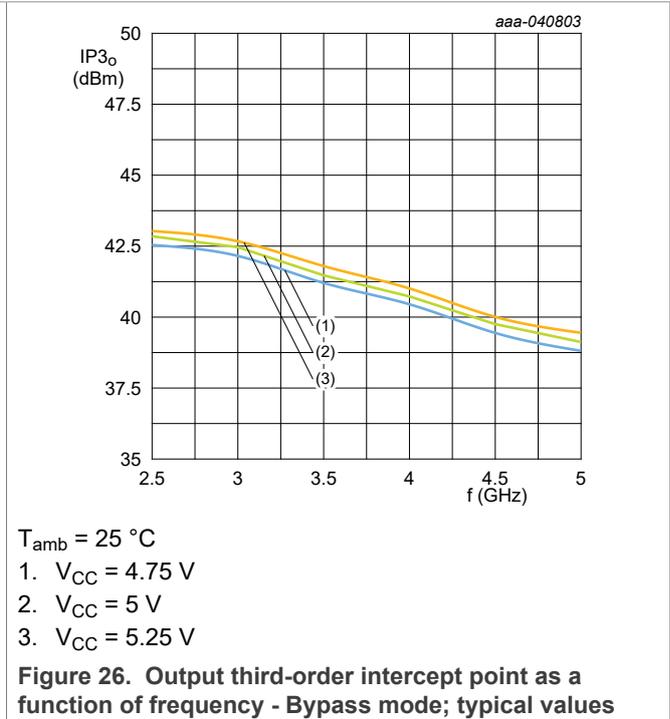
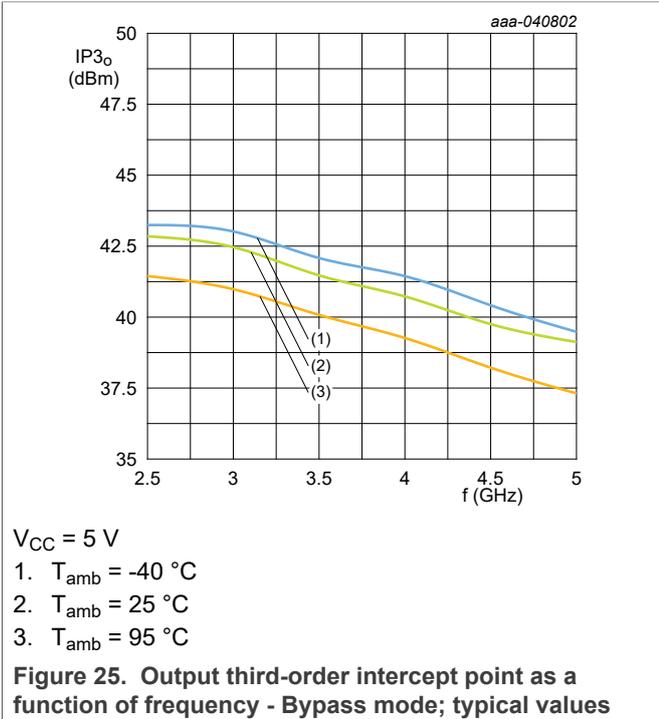
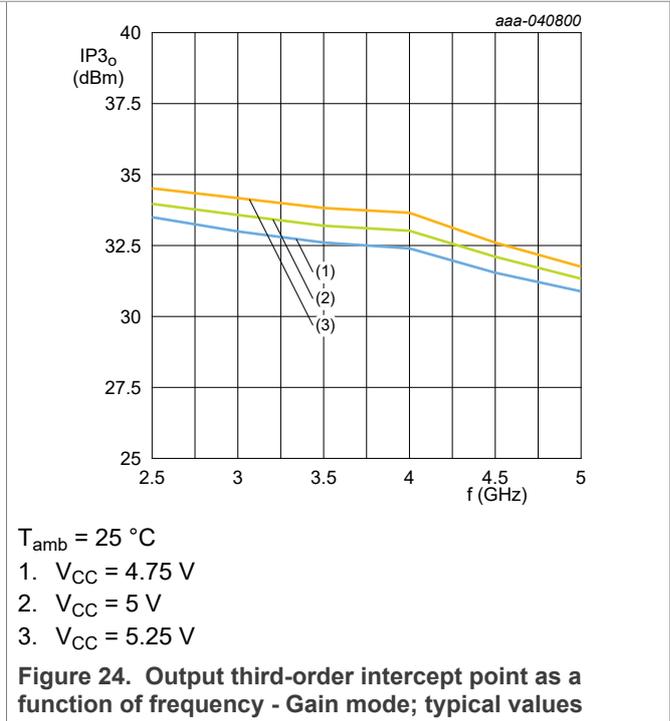
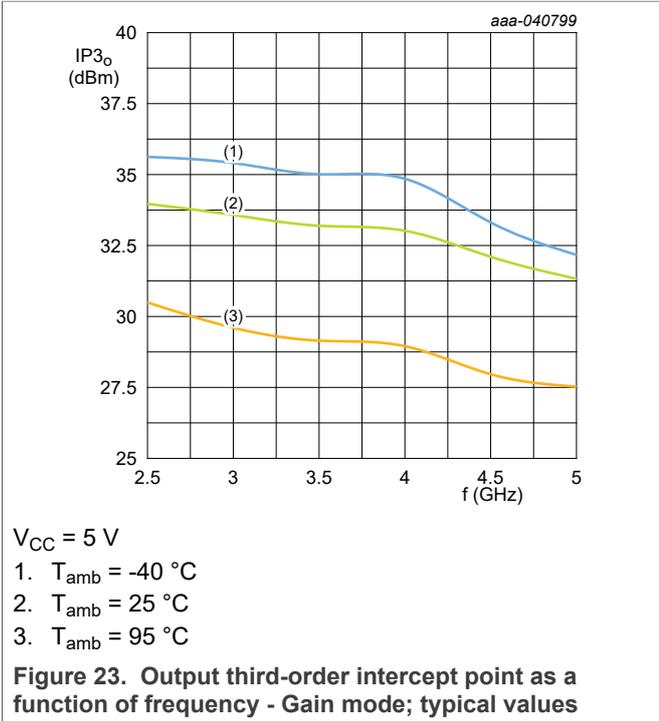


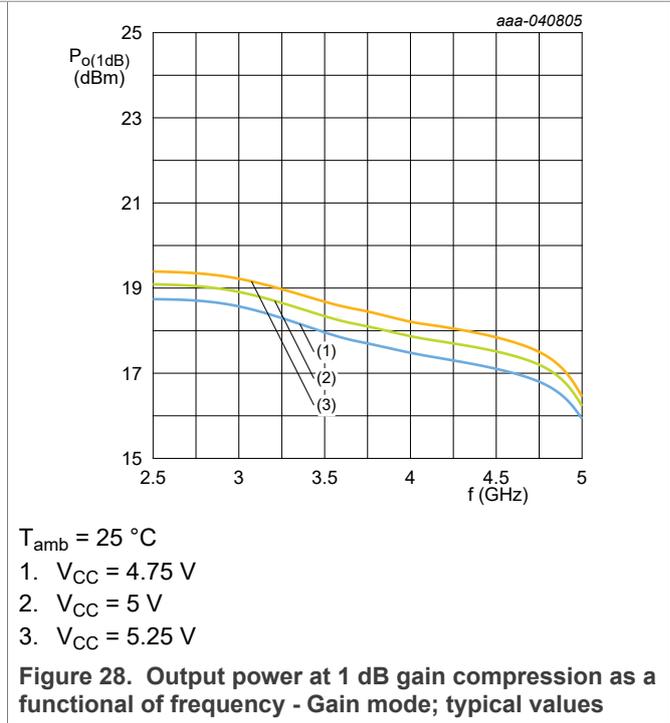
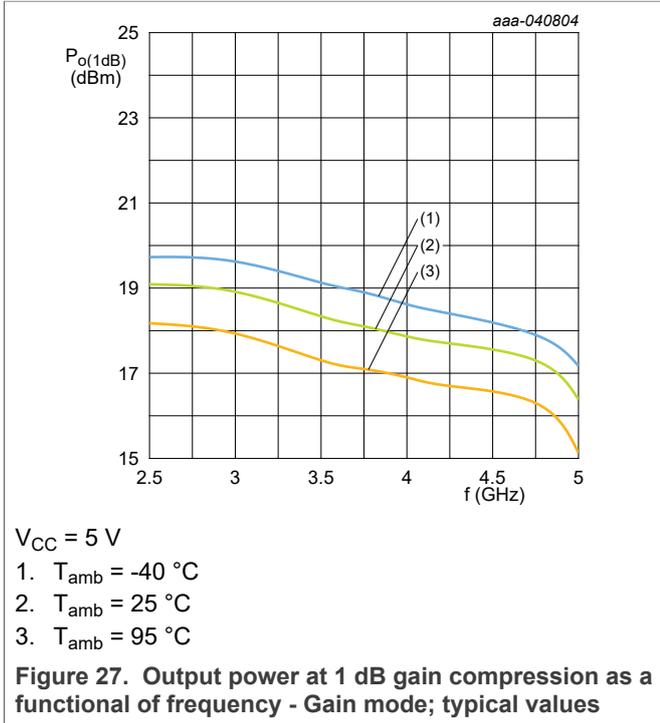












14 Application information

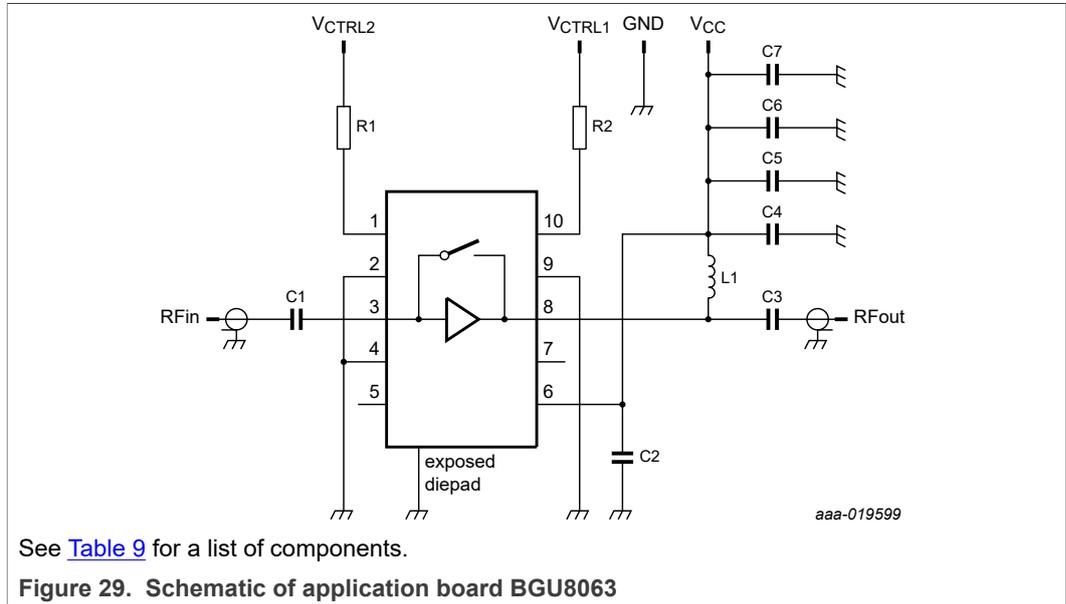


Table 9. List of components

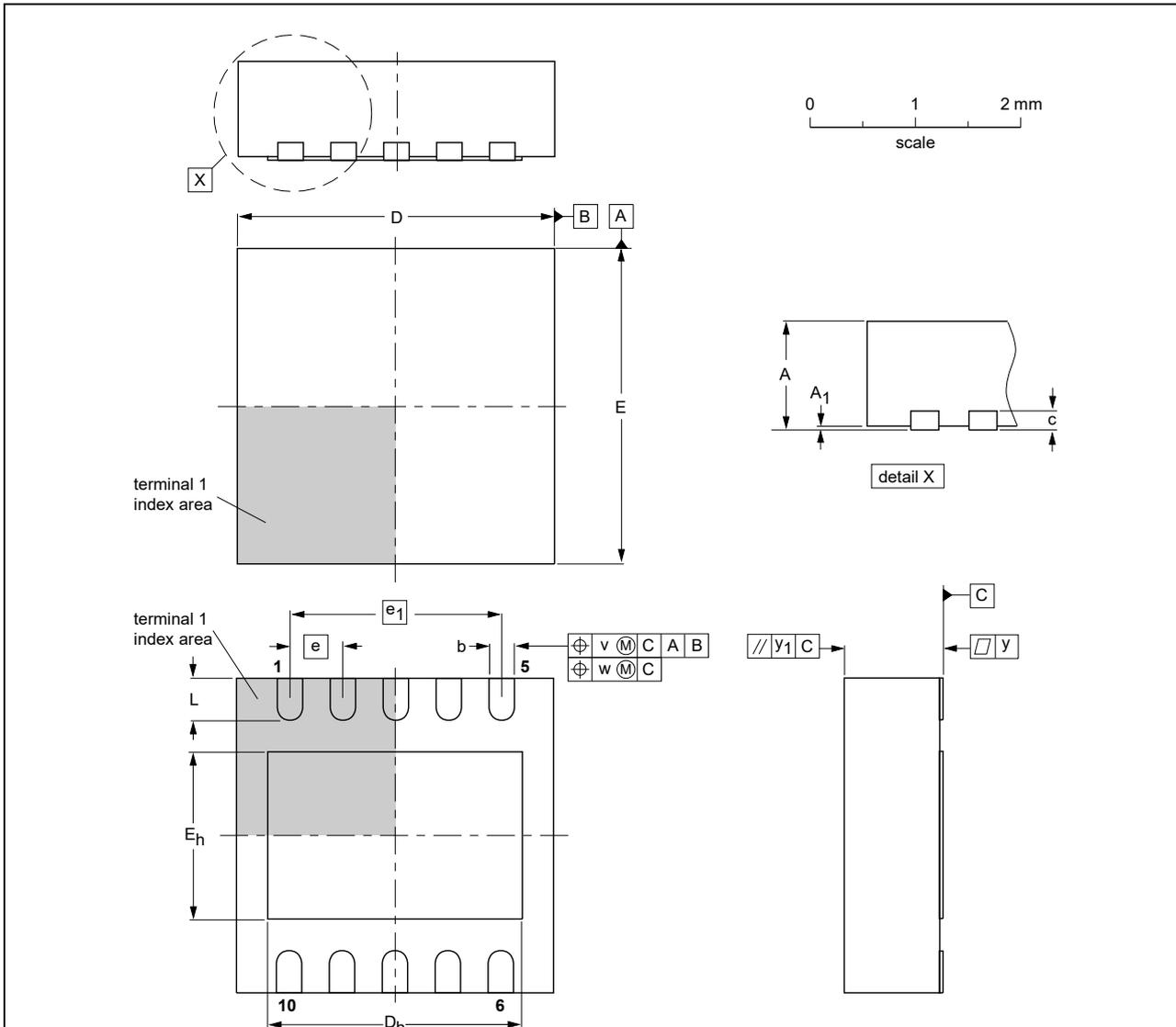
See [Figure 29](#) for schematics.

Component	Description	Value	Remarks
C1	capacitor	100 nF	
C2, C3	capacitor	100 pF	
C4	capacitor	1 nF	
C5	capacitor	-	optional
C6	capacitor	10 nF	
C7	capacitor	1 μ F	
L1	inductor	15 nH	
R1, R2	resistor	1 k Ω	

15 Package outline

HVSON10: plastic thermal enhanced very thin small outline package; no leads;
10 terminals; body 3 x 3 x 0.85 mm

SOT650-1



DIMENSIONS (mm are the original dimensions)

UNIT	A ⁽¹⁾ max.	A ₁	b	c	D ⁽¹⁾	D _h	E ⁽¹⁾	E _h	e	e ₁	L	v	w	y	y ₁
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	2.55 2.15	3.1 2.9	1.75 1.45	0.5	2	0.55 0.30	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT650-1	---	MO-229	---		01-01-22- 02-02-08

Figure 30. Package outline SOT650-1 (HVSON10)

15.1 Footprint and solder information

NXP recommends by default to apply the soldering and footprint guidelines as are released in POD SOT650-1

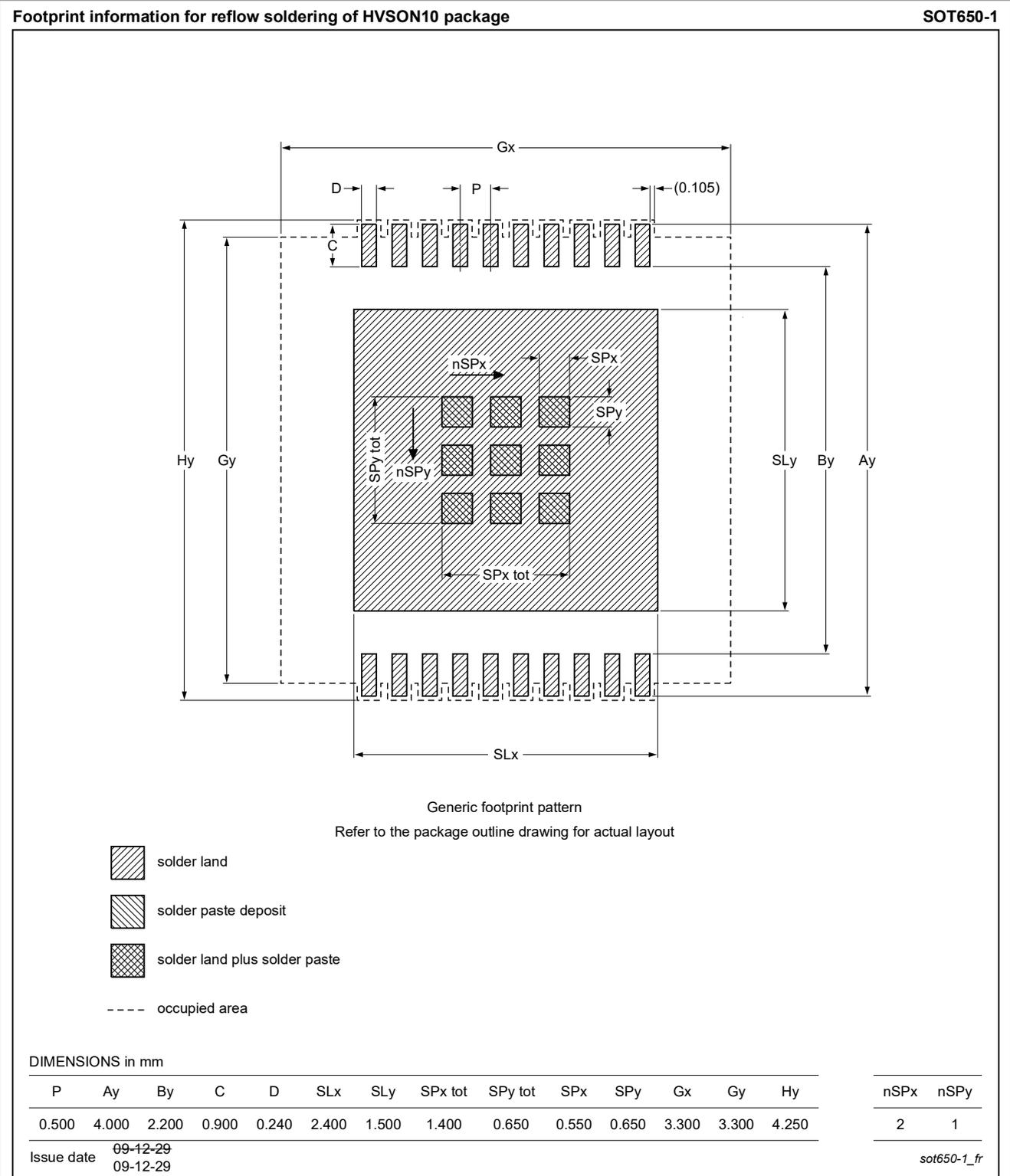


Figure 31. Footprint information

16 Abbreviations

Table 10. Abbreviations

Acronym	Description
CDMA	code division multiple-access
ESD	electroStatic discharge
FDD	frequency-division duplexing
GSM	global system for mobile communication
LNA	low noise amplifier
LTE	long-term evolution
TDD	time-division duplexing
W-CDMA	wideband code division multiple-access

17 Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BGU8063 v.3.1	20210210	Product data sheet	CIN	BGU8063 v.3
modification	<ul style="list-style-type: none"> corrected typo wrong product name was mentioned BGU3063 instead of BGU8063 			
BGU8063 v.3	20210127	Product data sheet	CIN	BGU8063 v.2
modification	<ul style="list-style-type: none"> changed frequency range in all graphics from 4 GHz to 5 GHz changed location of truth table from the Characteristics topic to the Functional description topic added solder footprint information added orderable part number to the Ordering information 			
BGU8063 v.2	20170127	Product data sheet	-	BGU8063 v.1
modification	<ul style="list-style-type: none"> changed status to Product data sheet 			
BGU8063v.1	20170112	Preliminary data sheet	-	-

18 Legal information

18.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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