LM3242 6-MHz, 750-mA Miniature Adjustable Step-Down DC-DC Converter With Auto Bypass for RF Power Amplifiers

1 Features

- 2.7-V to 5.5-V Input Voltage Operating From Single Li-Ion Cell
- 6-MHz (typical) PWM Switching Frequency
- 0.4-V to 3.6-V Adjustable Output Voltage
- 750-mA Maximum Load Capability (up to 1 A in Bypass)
- High Efficiency (95% typical at 3.9 V_{IN}, 3.3 V_{OUT} at 500 mA)
- Automatic ECO/PWM/BP Mode Change
- Current Overload Protection
- Thermal Overload Protection
- Soft-Start Function
- Small Chip Inductor in 0805 (2012) case size

2 Applications

- Battery-Powered 3G/4G RF PAs
- Battery-Powered RF Devices
- Hand-Held Radios
- RF PC Cards

3 Description

The LM3242 is a DC-DC converter optimized for powering RF power amplifiers (PAs) from a single lithium-ion cell; however, it may be used in many other applications. It steps down an input voltage from 2.7 V to 5.5 V to an adjustable output voltage from 0.4 V to 3.6 V. Output voltage is set using a VCON analog input for controlling power levels and efficiency of the RF PA.

The LM3242 offers five modes of operation. In PWM mode the device operates at a fixed frequency of 6 MHz (typical) which minimizes RF interference when driving medium-to-heavy loads. At light load, the device enters into ECO mode automatically and operates with reduced switching frequency. In ECO mode, the quiescent current is reduced and extends the battery life. Shutdown mode turns the device off and reduces battery consumption to 0.1 µA (typical). In low-battery condition Bypass mode reduces the voltage dropout to less than 50 mV (typical). The part also features a Sleep mode.

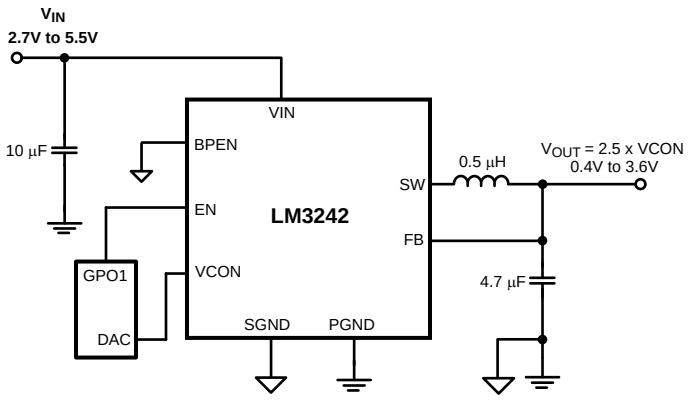
The LM3242 is available in a 9-bump lead-free DSBGA package. A high switching frequency (6 MHz) allows use of only three tiny surface-mount components: one inductor and two ceramic capacitors.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (MAX)
LM3242	DSBGA (9)	1.51 mm × 1.385 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (March 2013) to Revision E — **Page**

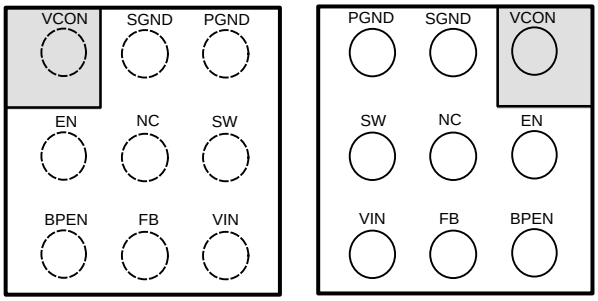
- Added *Device Information* and *Pin Configuration and Functions* sections, *ESD Ratings* table, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections ... 1

Changes from Revision C (March 2013) to Revision D — **Page**

- Changed layout of National Data Sheet to TI format ... 25

5 Pin Configuration and Functions

YFQ Package
9-Pin DSBGA
Top View (left); Bottom View (right)



Pin Functions

PIN		TYPE	DESCRIPTION
NUMBER	NAME		
A1	VCON	A/I	Voltage control analog input. VCON controls V_{OUT} in PWM and ECO modes. VCON may also be used to force bypass condition by setting VCON > V_{IN}/2.5.
A2	SGND	G	Signal ground for analog and control circuitry.
A3	PGND	G	Power ground for the power MOSFETs and gate drive circuitry
B1	EN	D/I	Enable Input. Set this digital input high for normal operation. For shutdown, set low. Do not leave EN pin floating.
B2	NC	—	Do not connect to PGND directly — Internally connected to SGND.
B3	SW	P/O	Switching node connection to the internal PFET switch and NFET synchronous rectifier. Connect to an inductor with a saturation current rating that exceeds the maximum Switch Peak Current Limit specification of the LM3242.
C1	BPEN	D/I	Bypass Enable input. Set this digital input high to force bypass operation. For normal operation with automatic bypass, set low or connect to ground. Do not leave this pin floating.
C2	FB	A	Feedback analog input and bypass FET output. Connect to the output at the output filter capacitor.
C3	VIN	P/I	Voltage supply input for SMPS converter.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
VIN to SGND	−0.2	6	V
PGND to SGND	−0.2	0.2	V
EN, VCON, BPEN	(SGND − 0.2)	(V_{IN} + 0.2) w/ 6 V	V
SW, FB	(PGND – 0.2)	(V_{IN} + 0.2)	V
Continuous power dissipation(2)	Internally limited		
Maximum lead temperature (soldering, 10 sec)		260	°C
Junction temperature, T_{J-MAX}		150	°C
Storage temperature, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 150°C (typical) and disengages at T_J = 125°C (typical).

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1250	
		Machine model	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	NOM	MAX	UNIT
Input voltage	2.7		5.5	V
Recommended load current	0		750	mA
PWM mode	0		750	mA
Bypass mode	0		1000	mA
Junction temperature, T_J	−30		125	°C
Ambient temperature, T_A(2)	−30		90	°C

(1) All voltages are with respect to the potential at the GND pins.
(2) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be de-rated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (R_{\theta JA} \times P_{D-MAX})$.

6.4 Thermal Information

THERMAL METRIC(1)		LM3242 YFQ (DSBGA) 9 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	85	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

All typical limits in are for $T_A = T_J = 25°C$; all minimum and maximum limits apply over the full operating ambient temperature range ($-30°C \le T_A = T_J \le +90°C$). Unless otherwise noted, all specifications apply to the *Typical Application* with V_{IN} = EN = 3.6 V, and BPEN = NC = 0 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{FB,MIN}$	Feedback voltage at minimum setting	PWM mode, VCON = 0.16 V(1)	0.38	0.4	0.42	V
$V_{FB,MAX}$	Feedback voltage at maximum setting	PWM mode, VCON = 1.44 V, V_{IN} = 4 V	3.55	3.6	3.65	V
I_{SHDN}	Shutdown supply current	EN = SW = VCON = FB = BPEN = NC = 0 V(2)		0.1	1	µA
I_Q_PWM	PWM mode quiescent current	PWM mode, No switching VCON = 0.13 V, FB = 1 V(3)		650	795	µA
I_Q_SLEEP	Low-power SLEEP mode	EN = VIN, BPEN = NC = 0 V, SW = TriState VCON < 0.08 V(3)		60	80	µA
I_Q_ECO	ECO mode Quiescent current	ECO mode, No switching VCON = 0.8 V, FB = 2.05 V(3)		60	80	µA
$R_{DSON\ (P)}$	Pin-pin resistance for PFET	$V_{IN} = V_{GS}$ = 3.6 V, I_{SW} = 200 mA		170	260	mΩ
$R_{DSON\ (N)}$	Pin-pin resistance for NFET	VIN = V_{GS} = 3.6 V, I_{SW} = −200 mA		110	200	mΩ
$R_{DSON\ (BP)}$	Pin-Pin resistance for BPFET	$V_{IN} = V_{GS}$ = 3.1 V, I_{SW} = −200 mA		80	110	mΩ
$I_{LIM\ P}$	PFET switch peak current limit	See(4)	1300	1450	1600	mA
$I_{LIM\ BP}$	BPFET switch peak current limit	$V_{FB} = V_{IN}$ − 1 V(4)	310	400		mA
F_{OSC}	Internal oscillator frequency		5.7	6	6.3	MHz
V_{IH}	EN, BPEN logic high input threshold		1.2			V
V_{IL}	EN, BPEN logic low input threshold				0.4	V
Gain	VCON to V_{OUT} gain	0.16 V ≤ VCON ≤ 1.44 V(5)		2.5		V/V
I_{VCON}	VCON pin leakage current	VCON = 1 V			±1	µA
$V_{BP,NEG}$	Auto bypass detection negative threshold	VCON = 1.2 V ($V_{OUT-SET}$ = 3 V) V_{IN} = 3.2 V, R_L = 6 Ω, I_{OUT} = 500 mA(6)	165	200	235	mV
$V_{BP,POS}$	Auto bypass detection positive threshold	VCON = 1.2 V ($V_{OUT-SET}$ = 3 V) V_{IN} = 3.25 V, R_L = 6 Ω, I_{OUT} = 500 mA(7)	215	250	285	mV
$I_{BP,SLEW}$	Auto bypass I_{OUT} slew current	BPEN = High, Forced bypass		1600		mA

(1) All 0.4-V V_{OUT} specifications are at steady-state only.
(2) Shutdown current includes leakage current of PFET.
(3) I_Q specified here is when the part is not switching under test mode conditions. For operating quiescent current at no load, refer to *Typical Characteristics*.
(4) Current limit is built-in, fixed, and not adjustable.
(5) Care must be taken to keep the VCON pin voltage less than the VIN pin voltage as this can place the part into a manufacturing test mode.
(6) Entering Bypass mode V_{IN} is compared to the programmed output voltage (2.5 × VCON). When V_{IN} − (2.5 × VCON) falls below $V_{BP,NEG}$ longer than $T_{BP,NEG}$, the Bypass FET turns on, and the switching FET turns on.
(7) Bypass mode is exited when V_{IN} − (2.5 × VCON) exceeds $V_{BP,POS}$ longer than $T_{BP,POS}$, and PWM mode resumes. The hysteresis for the bypass detection threshold $V_{BP,POS} – V_{BP,NEG}$ is always positive and will be approximately 50 mV.

6.6 System Characteristics

The following spec table entries are ensured by design providing the component values in the *Typical Application* are used. *These parameters are not ensured by production testing.* Minimum and Maximum values apply over the full operating ambient temperature range (−30°C ≤ T_A ≤ +90°C) and over the V_{IN} range = 2.7 V to 5.5 V unless otherwise specified. L = 0.5 µH, DCR = 50 mΩ, C_{IN} = 10 µF, 6.3 V, 0603 (1608), C_{OUT} = 4.7 µF, 6.3 V, 0402.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
D	Maximum duty cycle		100%			
R_{BP}	Bypass mode resistance(1)	V_{IN} = V_{GS} = 3.1 V, I_{OUT} = –500 mA VCON > 1.16 V		75		mΩ
I_{OUT}	Maximum output current capability	2.7 V ≤ V_{IN} ≤ 5.5 V 2.5 × VCON ≤ V_{IN} − 285 mV	750			mA
		2.7 V ≤ V_{IN} ≤ 5.5 V 2.5 × VCON ≥ V_{IN} – 165 mV, Bypass mode	1000			
C_{VCON}	VCON input capacitance	VCON = 1 V, Test frequency = 100 KHz		< 1		pF
V_{OUT} Linearity	VCON range 0.16 V to 1.44 V	0 mA ≤ I_{OUT} ≤ 750 mA(2)	−3%		3%	
			−50		50	mV
η	Efficiency	V_{IN} = 3.6 V, V_{OUT} = 0.8 V I_{OUT} = 10 mA, ECO mode		75%		
		V_{IN} = 3.6 V, V_{OUT} = 1.8 V I_{OUT} = 200 mA, PWM mode		90%		
		V_{IN} = 3.9 V, V_{OUT} = 3.3 V I_{OUT} = 500 mA, PWM mode		95%		
LINE $_{TR}$	Line transient response	V_{IN} = 3.6 V to 4.2 V, T_R = T_F = 10 µs, I_{OUT} = 100 mA, V_{OUT} = 0.8V		50		mVpk
LOAD $_{TR}$	Load transient response	V_{IN} = 3.1 V/3.6 V/4.5 V, V_{OUT} = 0.8 V, I_{OUT} = 50 mA to 150 mA T_R = T_F = 0.1 µs		50		mVpk

(1) Total resistance in Bypass mode. Total includes the Bypass FET resistance in parallel with the PWM switch path resistance (PFET resistance and series inductor parasistic resistance.)
(2) Linearity limits are ±3% or ±50 mV, whichever is larger. V_{OUT} is monotonic in nature with respect to VCON input.

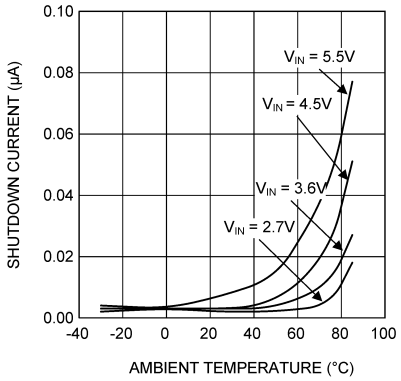
6.7 Timing Requirements

		MIN	NOM	MAX	UNIT
T_{VCON_TR}	V_{OUT} rise time, VCON change to 90% V_{IN} = 3.7 V, V_{OUT} = 1.4 V to 3.4 V 0.1 µs < VCON_T_R < 1 µs, R_L = 12 Ω		9		µs
	V_{OUT} fall time VCON change to 10% V_{IN} = 3.7 V, V_{OUT} = 3.4 V to 1.4 V 0.1 µs < VCON_T_F < 1 µs, R_L = 12 Ω		9		µs
T_{ON}	Turnon time (time for output to reach 95% final value after Enable low-to-high transition) EN = Low-to-High, V_{IN} = 4.2 V, V_{OUT} = 3.4 V I_{OUT} = < 1 mA, C_{OUT} = 4.7 µF			50(1)	µs
$T_{BP,\ NEG}$	Auto bypass detect negative threshold delay time(2)		10		µs
$T_{BP,\ POS}$	Auto bypass detect positive threshold delay time(3)		0.1		µs

(1) This parameter is not production-limit tested.
(2) Entering Bypass mode V_{IN} is compared to the programmed output voltage (2.5 × VCON). When V_{IN} − (2.5 × VCON) falls below $V_{BP,NEG}$ longer than $T_{BP,NEG}$, the Bypass FET turns on, and the switching FET turns on.
(3) Bypass mode is exited when V_{IN} − (2.5 × VCON) exceeds $V_{BP,POS}$ longer than $T_{BP,POS}$, and PWM mode resumes. The hysteresis for the bypass detection threshold $V_{BP,POS}$ – $V_{BP,NEG}$ is always be positive and will be approximately 50 mV.

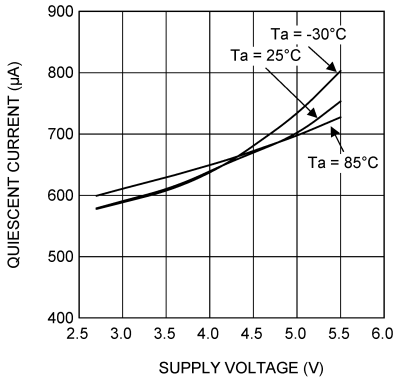
6.8 Typical Characteristics

V_{IN} = EN = 3.6 V, L = 0.5 µH, C_{IN} = 10 µF, C_{OUT} = 4.7 µF and T_A = 25°C, unless otherwise noted.



SW = VCON = EN = 0 V

Figure 1. Shutdown Current vs Temperature



FB = 1 V VCON = 0.13 V

Figure 2. Quiescent Current vs Supply Voltage (No Switching)

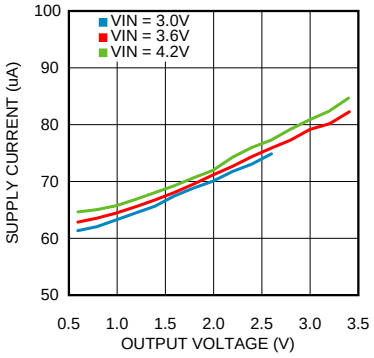
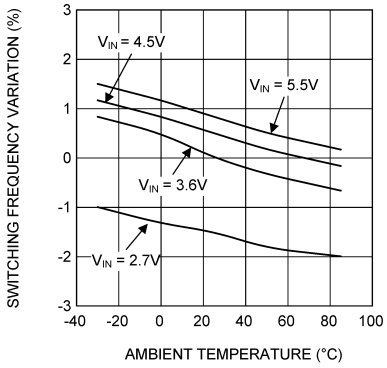
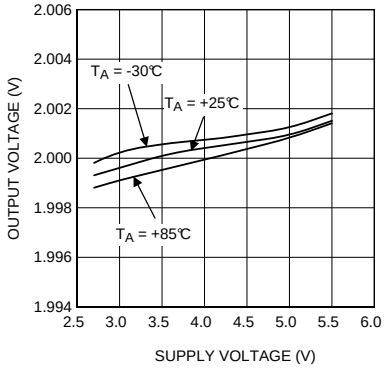


Figure 3. ECO Mode Supply Current vs Output Voltage (Closed Loop, Switching, No Load)



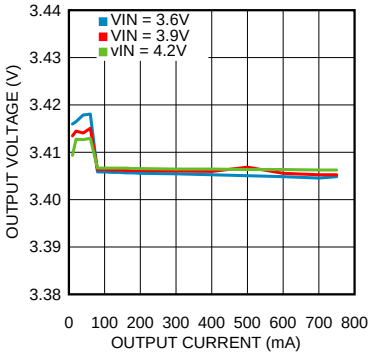
V_{OUT} = 2 V I_{OUT} = 200 mA

Figure 4. Switching Frequency vs Temperature



V_{OUT} = 2 V R_{LOAD}=10 Ω

Figure 5. Output Voltage vs Supply Voltage

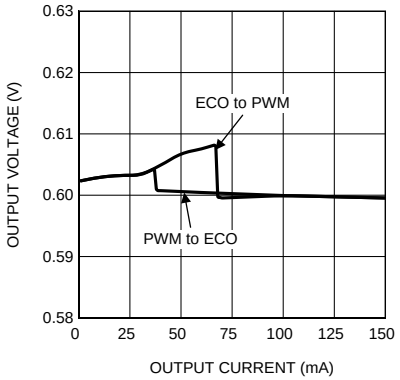


V_{OUT} = 3.4 V

Figure 6. Output Voltage vs Output Current

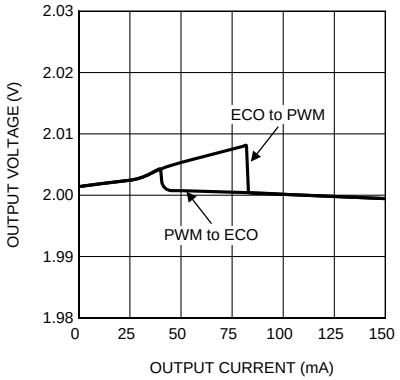
Typical Characteristics (continued)

V_{IN} = EN = 3.6 V, L = 0.5 µH, C_{IN} = 10 µF, C_{OUT} = 4.7 µF and T_A = 25°C, unless otherwise noted.



V_{OUT} = 0.6 V

Figure 7. Output Voltage vs Output Current



V_{OUT} = 2 V

Figure 8. Output Voltage vs Output Current

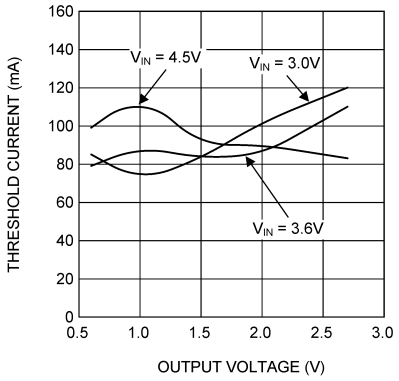


Figure 9. ECO-PWM Mode Threshold Current vs Output Voltage

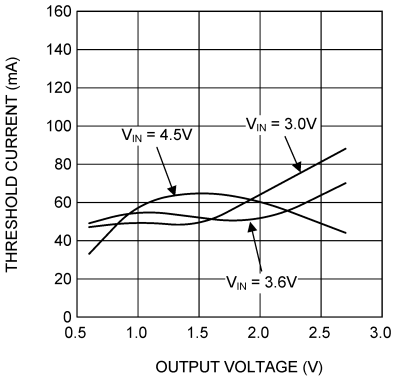
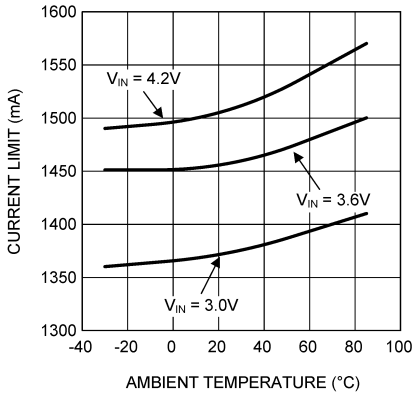
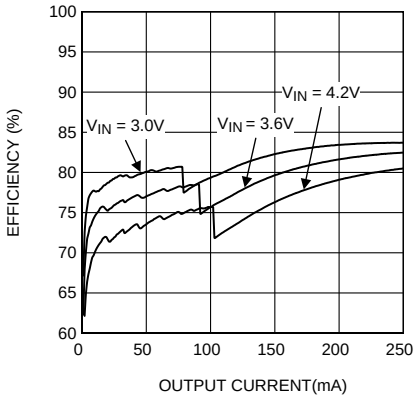


Figure 10. PWM-ECO Mode Threshold Current vs Output Voltage



V_{OUT} = 2 V

Figure 11. Closed-Loop Current Limit vs Temperature

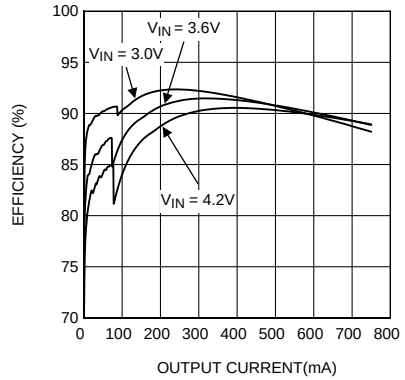


V_{OUT} = 0.8 V

Figure 12. Efficiency vs Output Current

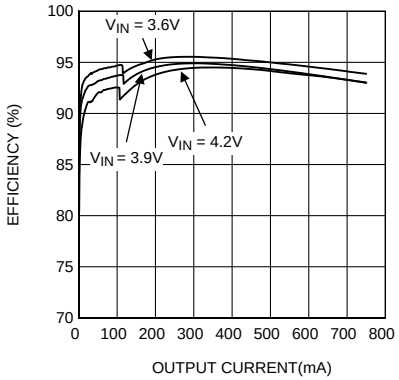
Typical Characteristics (continued)

V_{IN} = EN = 3.6 V, L = 0.5 µH, C_{IN} = 10 µF, C_{OUT} = 4.7 µF and T_A = 25°C, unless otherwise noted.



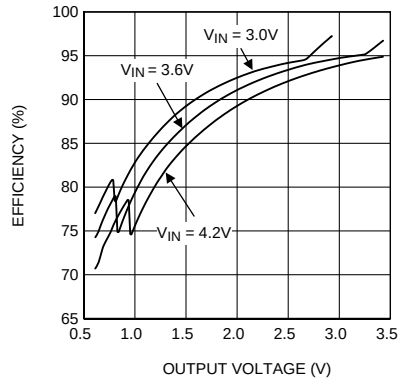
V_{OUT} = 2 V

Figure 13. Efficiency vs Output Current



V_{OUT} = 3.3 V

Figure 14. Efficiency vs Output Current



R_{LOAD} = 10 Ω

Figure 15. Efficiency vs Output Voltage

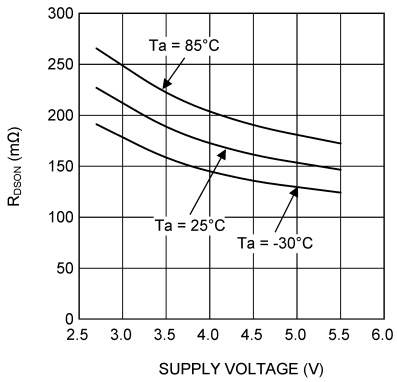


Figure 16. PFET R_{DSON} vs Supply Voltage

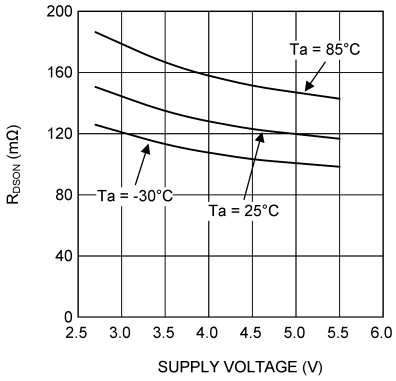


Figure 17. NFET R_{DSON} vs Supply Voltage

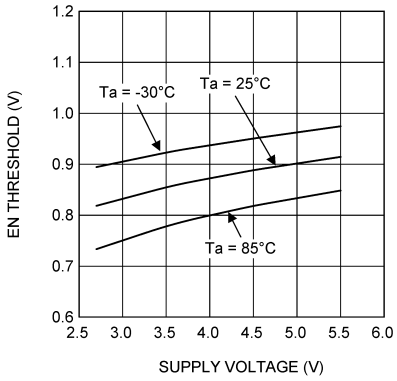


Figure 18. EN High Threshold vs Supply Voltage

Typical Characteristics (continued)

V_{IN} = EN = 3.6 V, L = 0.5 µH, C_{IN} = 10 µF, C_{OUT} = 4.7 µF and T_A = 25°C, unless otherwise noted.

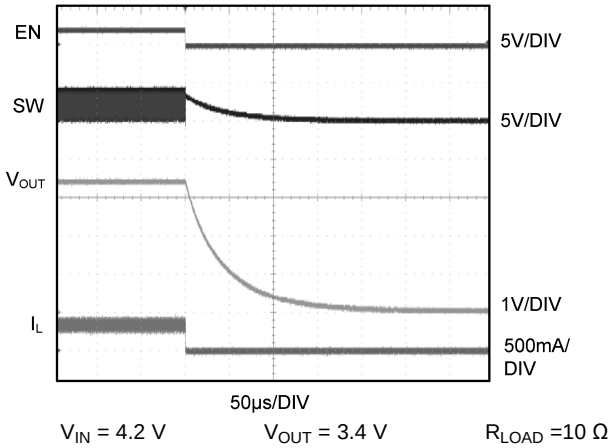


Figure 19. Shutdown

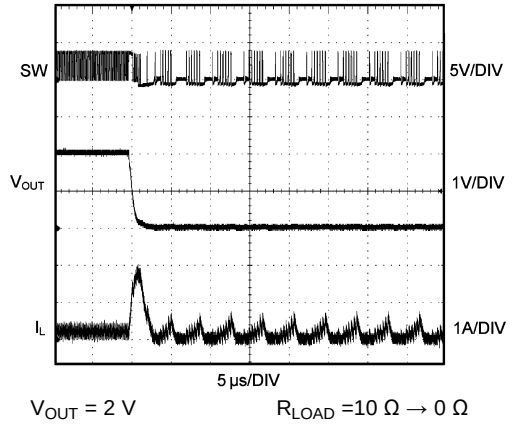


Figure 20. Timed Current Limit

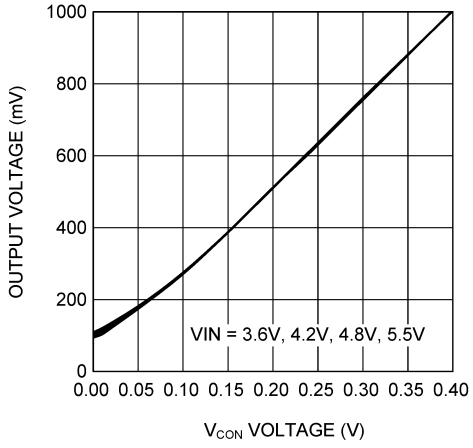


Figure 21. Low VCON Voltage vs Output Voltage

7 Detailed Description

7.1 Overview

The LM3242 is a simple, step-down DC-DC converter optimized for powering RF power amplifiers (PAs) in mobile phones, portable communicators, and similar battery-powered RF devices. It is designed to allow the RF PA to operate at maximum efficiency over a wide range of power levels from a single Li-Ion battery cell. It is based on a voltage-mode buck architecture, with synchronous rectification for high efficiency. The device is designed for a maximum load capability of 750 mA in PWM mode. Maximum load range may vary from this depending on input voltage, output voltage, and the inductor chosen.

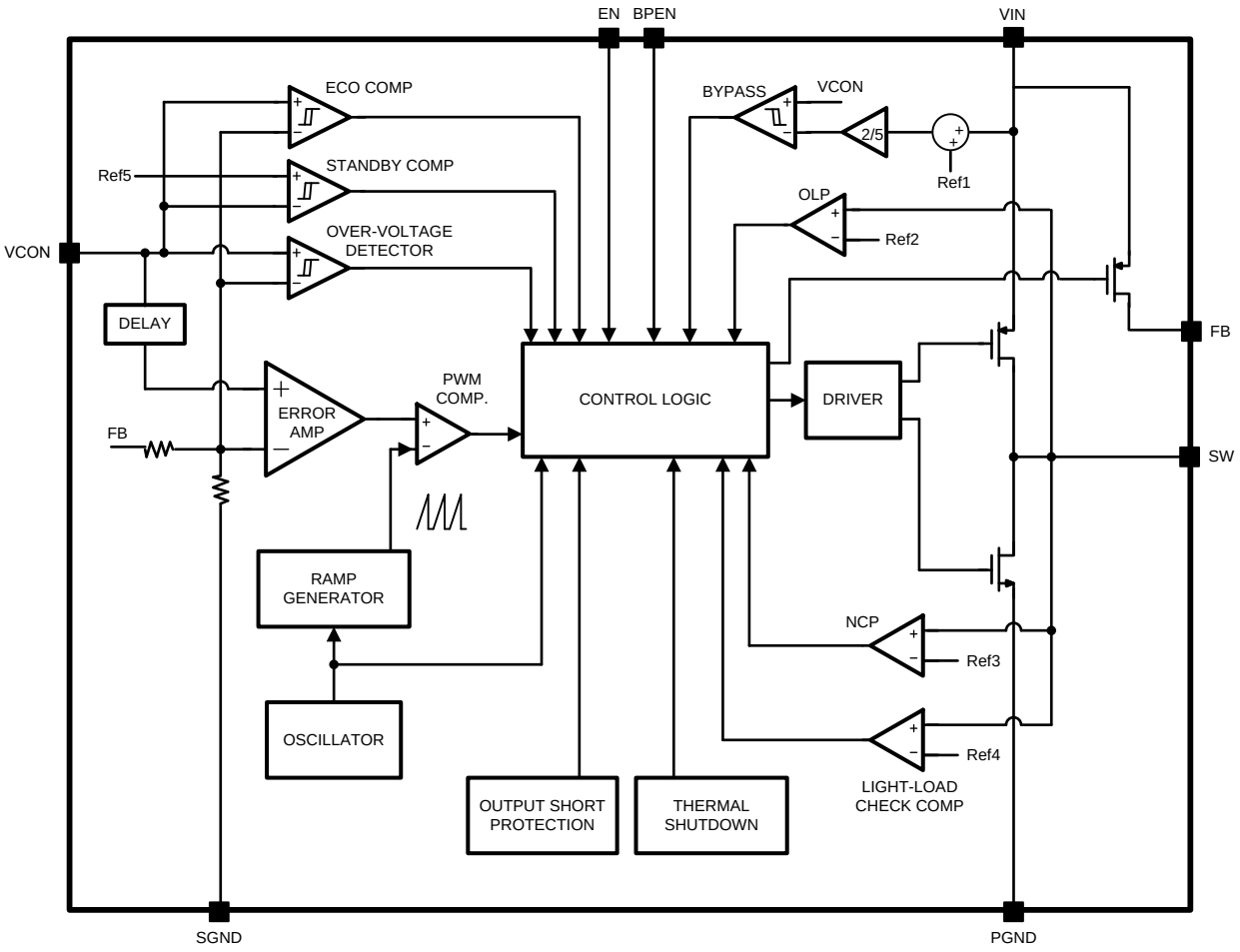
There are five modes of operation depending on the current required: PWM (Pulse Width Modulation), ECO (ECOnomy), BP (Bypass), Sleep, and Shutdown. (See Table 1.) The LM3242 operates in PWM mode at higher load current conditions. Lighter loads cause the device to automatically switch into ECO mode. Shutdown mode turns the device off and reduces battery consumption to 0.1 µA (typical).

DC PWM mode output voltage precision is ±2% for 3.6 V_{OUT}. Efficiency is typically around 95% (typical) for a 500-mA load with 3.3-V output, 3.9-V input. The output voltage is dynamically programmable from 0.4 V to 3.6 V by adjusting the voltage on the control pin (VCON) without the need for external feedback resistors. This ensures longer battery life by being able to change the PA supply voltage dynamically depending on its transmitting power.

Additional features include current overload protection and thermal overload shutdown.

The LM3242 is constructed using a chip-scale 9-bump DSBGA package. This package offers the smallest possible size, for space-critical applications such as cell phones, where board area is an important design consideration. Use of a high switching frequency (6 MHz, typical) reduces the size of external components. As shown in the Typical Application Circuit, only three external power components are required for implementation. Use of a DSBGA package requires special design considerations for implementation. (See *DSBGA Package Assembly and Use*.) Its fine bump-pitch requires careful board design and precision assembly equipment. Use of this package is best suited for opaque-case applications, where its edges are not subject to high-intensity ambient red or infrared light. Also, the system controller must set EN low during power-up and other low supply voltage conditions. (See *Shutdown Mode*.)

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Circuit Operation

Referring to the *Typical Application* and *Functional Block Diagram*, the LM3242 operates as follows. During the first part of each switching cycle, the control block in the LM3242 turns on the internal top-side PFET switch. This allows current to flow from the input through the inductor to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of around (V_{IN} − V_{OUT}) / L, by storing energy in a magnetic field. During the second part of each cycle, the controller turns the PFET switch off, blocking current flow from the input, and then turns the bottom-side NFET synchronous rectifier on. In response, the inductor's magnetic field collapses, generating a voltage that forces current from ground through the synchronous rectifier to the output filter capacitor and load. As the stored energy is transferred back into the circuit and depleted, the inductor current ramps down with a slope around V_{OUT} / L. The output filter capacitor stores charge when the inductor current is high, and releases it when low, smoothing the voltage across the load.

The output voltage is regulated by modulating the PFET switch on time to control the average current sent to the load. The effect is identical to sending a duty-cycle modulated rectangular wave formed by the switch and synchronous rectifier at SW to a low-pass filter formed by the inductor and output filter capacitor. The output voltage is equal to the average voltage at the SW pin.

Feature Description (continued)

7.3.2 Internal Synchronous Rectification

While in PWM mode, the LM3242 uses an internal NFET as a synchronous rectifier to reduce rectifier forward voltage drop and associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across an ordinary rectifier diode.

With medium and heavy loads, the NFET synchronous rectifier is turned on during the inductor current down slope in the second part of each cycle. The synchronous rectifier is turned off prior to the next cycle. The NFET is designed to conduct through its intrinsic body diode during transient intervals before it turns on, eliminating the need for an external diode.

7.3.3 Current Limiting

The current limit feature allows the LM3242 to protect itself and external components during overload conditions. In PWM mode, the cycle-by-cycle current limit is a 1450 mA (typical). If an excessive load pulls the output voltage down to less than 0.3V (typical), the NFET synchronous rectifier is disabled and the current limit is reduced to 530 mA (typical). Moreover, when the output voltage becomes less than 0.15V (typical), the switching frequency decreases to 3 MHz, thereby preventing excess current and thermal stress.

7.3.4 Dynamically Adjustable Output Voltage

The LM3242 features dynamically adjustable output voltage to eliminate the need for external feedback resistors. The output can be set from 0.4 V to 3.6 V by changing the voltage on the analog VCON pin. This feature is useful in PA applications where peak power is needed only when the handset is far away from the base station or when data is being transmitted. In other instances the transmitting power can be reduced. Hence the supply voltage to the PA can be reduced, promoting longer battery life. See *Setting The Output Voltage* in *Application and Implementation* for further details. The LM3242 moves into pulse-skipping mode when duty cycle is over approximately 92% or less than approximately 15% and the output voltage ripple increases slightly.

7.3.5 Thermal Overload Protection

The LM3242 has a thermal overload protection function that operates to protect itself from short-term misuse and overload conditions. When the junction temperature exceeds around 150°C, the device inhibits operation. Both the PFET and the NFET are turned off. When the temperature drops below 125°C, normal operation resumes. Prolonged operation in thermal overload conditions may damage the device and is considered bad practice.

7.3.6 Soft Start

The LM3242 has a soft-start circuit that limits in-rush current during start-up. During start-up the switch current limit is increased in steps. Soft start is activated if EN goes from low to high after V_{IN} reaches 2.7V.

7.4 Device Functional Modes

Table 1. Description Of Modes

MODE	EN	BPEN	VCON	I_{OUT}
Shutdown	0	X	X	X
Sleep	1	0	< 80 mV	X
Pulse Width Modulation (PWM)	1	0	> 130 mV, < (V_{IN} − 0.2 V)/2.5	> 100 mA
Economy (ECO)	1	0		< 50 mA
Bypass (BP)	1	0	> (V_{IN} − 0.2 V)/2.5	X
	1	1	X	X

7.4.1 PWM Mode Operation

While in PWM mode operation, the converter operates as a voltage-mode controller with input voltage feedforward. This allows the converter to achieve excellent load and line regulation. The DC gain of the power stage is proportional to the input voltage. To eliminate this dependence, feed forward inversely proportional to the input voltage is introduced. While in PWM mode, the output voltage is regulated by switching at a constant frequency and then modulating the energy per cycle to control power to the load. At the beginning of each clock cycle the PFET switch is turned on and the inductor current ramps up until the comparator trips and the control logic turns off the switch. The current limit comparator can also turn off the switch in case the current limit of the PFET is exceeded. Then the NFET switch is turned on and the inductor current ramps down. The next cycle is initiated by the clock turning off the NFET and turning on the PFET.

7.4.2 Bypass Mode Operation

The LM3242 contains an internal BPFET switch for bypassing the PWM DC-DC converter during Bypass mode. In Bypass mode, this BPFET is turned on to power the PA directly from the battery for maximum RF output power. When the part operates in the Bypass mode, the output voltage is the input voltage less the voltage drop across the resistance of the BPFET in parallel with the PFET + Switch Inductor. Bypass mode is more efficient than operating in PWM mode at 100% duty cycle because the combined resistance is significantly less than the series resistance of the PWM PFET and inductor. This translates into higher voltage available on the output in Bypass mode, for a given battery voltage. The part can be set to bypass mode by sending BPEN pin high. This is called Forced Bypass Mode and it remains in bypass mode until BPEN pin goes low. Alternatively the part can go into Bypass mode automatically. This is called Auto-Bypass mode or Automatic Bypass mode. The bypass switch turns on when the difference between the input voltage and programmed output voltage is less than 200 mV (typical) for longer than 10 µs (typical). The bypass switch turns off when the input voltage is higher than the programmed output voltage by 250 mV (typical) for longer than 0.1 µs (typical). This method is very system resource friendly in that the Bypass PFET is turned on automatically when the input voltage gets close to the output voltage, a typical scenario of a discharging battery. It is also turned off automatically when the input voltage rises, a typical scenario when connecting a charger. When V_{OUT} < 300 mV, BPEN is ignored.

7.4.3 ECO Mode Operation

At very light loads (50 mA to 100 mA), the LM3242 enters ECO mode operation with reduced switching frequency and supply current to maintain high efficiency. During ECO mode operation, the LM3242 positions the output voltage slightly higher (7 mV typical) than the normal output voltage during PWM mode operation, allowing additional headroom for voltage drop during a load transient from light to heavy load.

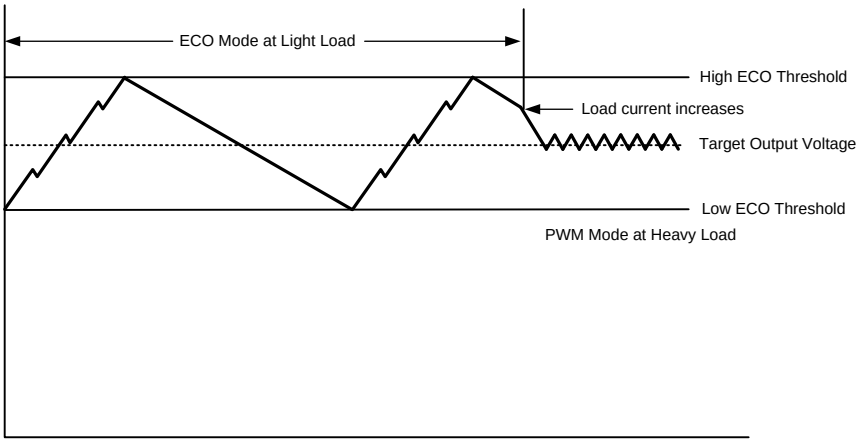


Figure 22. Operation In ECO Mode and Transfer to PWM Mode

7.4.4 Sleep Mode Operation

When VCON is less than 80 mV in 10 µs, the LM3242 goes into SLEEP mode — the SW pin is in Tri-state (floating), which operates like ECO mode with no switching. The LM3242 device returns to normal operation immediately when VCON ≥ 130 mV in PWM mode or ECO mode, depending on load detection.

7.4.5 Shutdown Mode

Setting the EN digital pin low (< 0.4 V) places the LM3242 in Shutdown mode (0.1 µA typical). During shutdown, the PFET switch, the NFET synchronous rectifier, reference voltage source, control and bias circuitry of the LM3242 are turned off. Setting EN high (> 1.2 V) enables normal operation. EN must be set low to turn off the LM3242 during power-up and undervoltage conditions when the power supply is less than the 2.7V minimum operating voltage. The LM3242 has an undervoltage lock-out (UVLO) comparator to turn the power device off in the case the input voltage or battery voltage is too low. The typical UVLO threshold is around 2 V for lock and 2.1 V for release.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Setting The Output Voltage

The LM3242 features a pin-controlled adjustable output voltage to eliminate the need for external feedback resistors. It can be programmed for an output voltage from 0.4 V to 3.6 V by setting the voltage on the VCON pin, as in Equation 1:

$$V_{OUT} = 2.5 \times VCON \quad (1)$$

When VCON is between 0.16 V and 1.44 V, the output voltage will follow proportionally by 2.5 times of VCON.

If VCON is less than 0.16 V (V_{OUT} = 0.4 V), the output voltage may not be well regulated. Refer to Figure 21 for more detail. This curve exhibits the characteristics of a typical part, and the performance cannot be ensured as there could be a part-to-part variation for output voltages less than 0.4 V. For V_{OUT} lower than 0.4 V, the converter might suffer from larger output ripple voltage and higher current limit operation.

8.1.2 FB

Typically the FB pin is connected to V_{OUT} for regulating the output voltage maximum of 3.6 V.

8.2 Typical Application

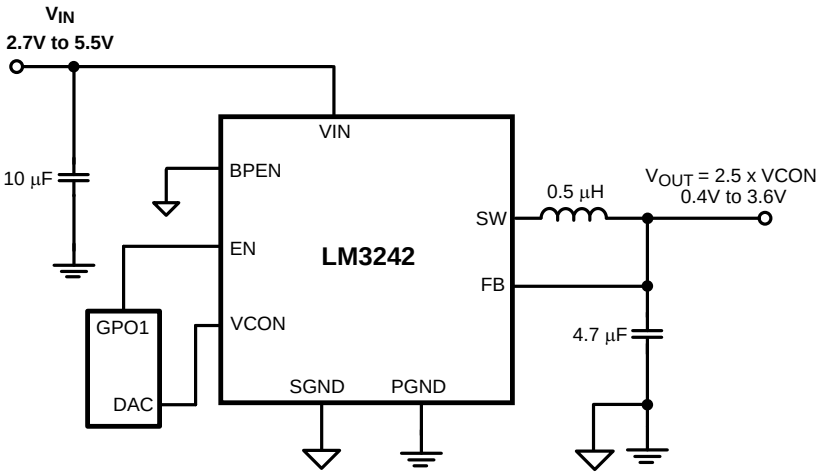


Figure 23. LM3242 Typical Application

Typical Application (continued)

8.2.1 Design Requirements

For typical step-down DC-DC applications, use the parameters listed in Table 2.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Minimum input voltage	2.7 V
Minimum output voltage	0.4 V
Output current	0 to 750 mA
Switching frequency	6 MHz (typical)

8.2.2 Detailed Design Procedure

8.2.2.1 Inductor Selection

There are two main considerations when choosing an inductor; the inductor must not saturate, and the inductor current ripple is small enough to achieve the desired output voltage ripple. Different manufacturers follow different saturation current rating specifications, so attention must be given to details. Saturation current ratings are typically specified at 25°C so ratings over the ambient temperature of application should be requested from manufacturer.

Minimum value of inductance to ensure good performance is 0.3 µH at bias current (I_{LIM} (typical)) over the ambient temperature range. Shielded inductors radiate less noise and are preferred. There are two methods to choose the inductor saturation current rating:

8.2.2.1.1 Method 1

The saturation current must be greater than the sum of the maximum load current and the worst-case average-to-peak inductor current. This can be written as:

$$I_{SAT} > I_{OUT\_MAX} + I_{RIPPLE}$$

where

$$I_{RIPPLE} = \left(\frac{V_{IN} - V_{OUT}}{2 \times L}\right) \times \left(\frac{V_{OUT}}{V_{IN}}\right) \times \left(\frac{1}{f}\right) \quad (2)$$

where

- I_{RIPPLE}: average-to-peak inductor current
- I_{OUT_MAX}: maximum load current (750 mA)
- V_{IN}: maximum input voltage in application
- L minimum inductor value including worst-case tolerances (30% drop can be considered for Method 1)
- F: minimum switching frequency (5.7 MHz)
- V_{OUT}: output voltage

8.2.2.1.2 Method 2

A more conservative and recommended approach is to choose an inductor that can handle the maximum current limit of 1600 mA.

The resistance of the inductor must be less than approximately 0.1 Ω for good efficiency. Table 3 lists suggested inductors and suppliers.

Table 3. Suggested Inductors

MODEL	SIZE (W × L × H) (mm)	VENDOR
MIPSZ2012D0R5	2 × 1.2 × 1	FDK
LQM21PNR54MG0	2 × 1.25 × 0.9	Murata
LQM2MPNR47NG0	2 × 1.6 × 0.9	Murata
CIG21LR47M	2 × 1.25 × 1	Samsung
CKP2012NR47M	2 × 1.25 × 1	Taiyo Yuden

8.2.2.2 Capacitor Selection

The LM3242 is designed for use with ceramic capacitors for its input and output filters. Use a 10-µF ceramic capacitor for input and a sum total of 4.7-µF ceramic capacitors for the output. They must maintain at least 50% capacitance at DC bias and temperature conditions. Ceramic capacitors types such as X5R, X7R, and B are recommended for both filters. These provide an optimal balance between small size, cost, reliability and performance for cell phones and similar applications. Table 4 lists some suggested part numbers and suppliers. DC bias characteristics of the capacitors must be considered when selecting the voltage rating and case size of the capacitor. If it is necessary to choose a 0603 (1608) size capacitor for V_{IN} and 0402 (1005) size capacitor for V_{OUT}, the operation of the LM3242 must be carefully evaluated on the system board. Use of a 2.2-µF capacitor in conjunction with multiple 0.47 µF or 1 µF capacitors in parallel may also be considered when connecting to power amplifier devices that require local decoupling.

Table 4. Suggested Capacitors and Their Suppliers

CAPACITANCE	MODEL	SIZE (W × L) (mm)	VENDOR
2.2 µF	GRM155R60J225M	1 × 0.5	Murata
2.2 µF	C1005X5R0J225M	1 × 0.5	TDK
2.2 µF	CL05A225MQ5NSNC	1 × 0.5	Samsung
4.7 µF	C1608JB0J475M	1.6 × 0.8	TDK
4.7 µF	C1005X5R0J475M	1 × 0.5	TDK
4.7 µF	CL05A475MQ5NRNC	1 × 0.5	Samsung
10 µF	C1608X5R0J106M	1.6 × 0.8	TDK
10 µF	GRM155R60J106M	1 × 0.5	Murata
10 µF	CL05A106MQ5NUNC	1 × 0.5	Samsung

The input filter capacitor supplies AC current drawn by the PFET switch of the LM3242 in the first part of each cycle and reduces the voltage ripple imposed on the input power source. The output filter capacitor absorbs the AC inductor current, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low Equivalent Series Resistance (ESR) to perform these functions. The ESR of the filter capacitors is generally a major factor in voltage ripple.

8.2.3 Application Curves

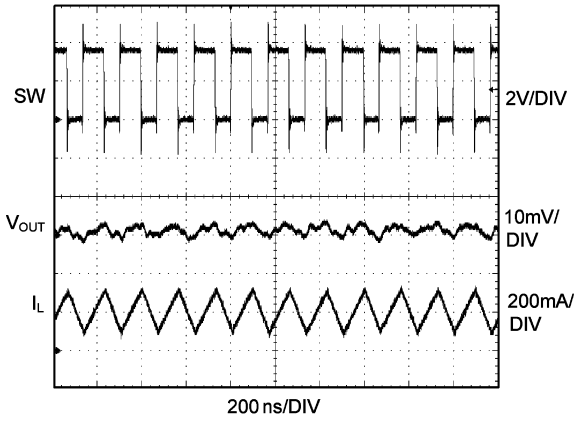


Figure 24. Output Voltage Ripple In PWM Mode

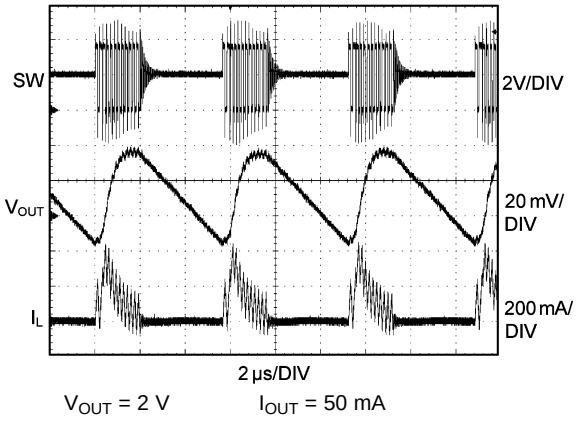


Figure 25. Output Voltage Ripple In ECO Mode

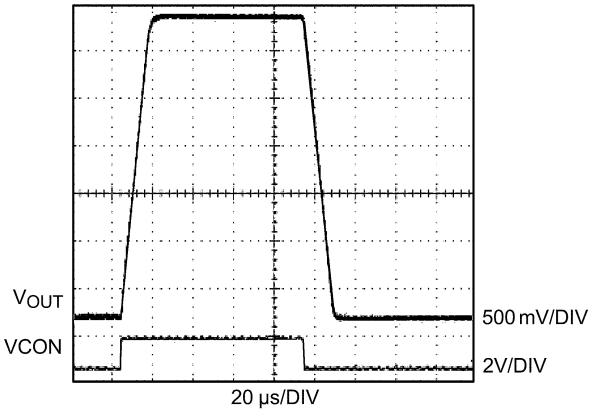


Figure 26. VCON Transient Response

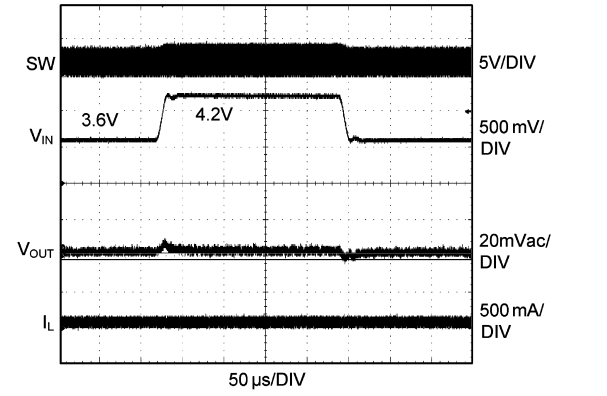


Figure 27. Line Transient Response

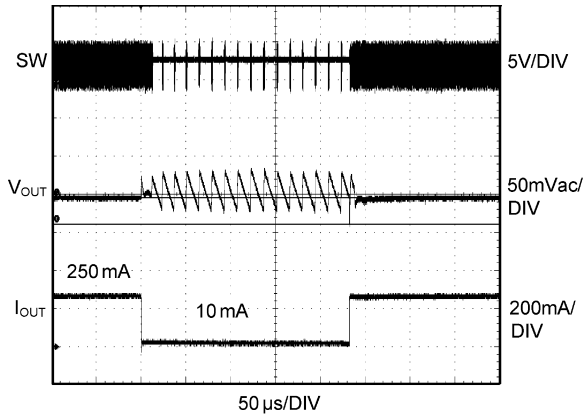


Figure 28. Load Transient Response

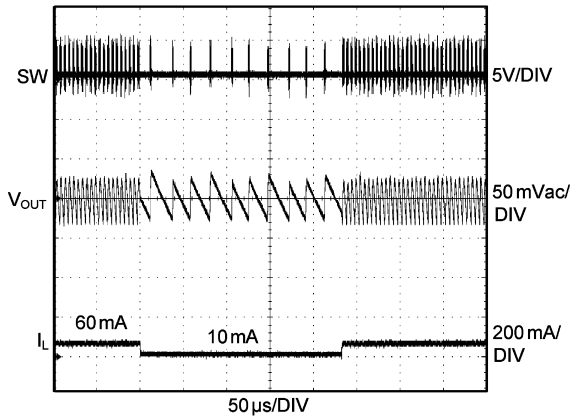


Figure 29. Load Transient Response

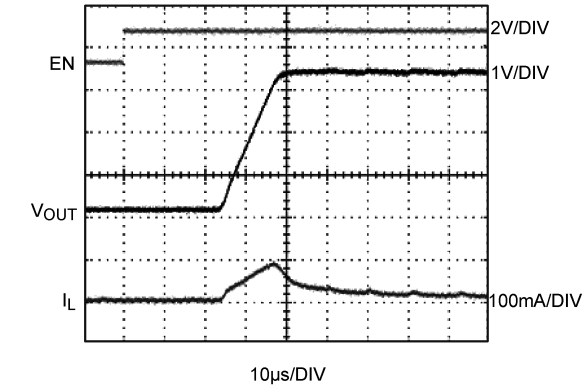


Figure 30. Start-Up

9 Power Supply Recommendations

The LM3242 device is designed to operate from an input voltage supply range between 2.7 V and 5.5 V. This input supply must be well regulated.

10 Layout

10.1 Layout Guidelines

PC board layout is critical to successfully designing a DC-DC converter into a product. As much as a 20-dB improvement in RX noise floor can be achieved by carefully following recommended layout practices. A properly planned board layout optimizes the performance of a DC-DC converter and minimizes effects on surrounding circuitry while also addressing manufacturing issues that can have adverse impacts on board quality and final product yield.

10.1.1 PCB Considerations

Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. Erroneous signals could be sent to the DC-DC converter device, resulting in poor regulation or instability. Poor layout can also result in re-flow problems leading to poor solder joints between the DSBGA package and board pads. Poor solder joints can result in erratic or degraded performance of the converter.

10.1.1.1 Energy Efficiency

Minimize resistive losses by using wide traces between the power components and doubling up traces on multiple layers when possible.

10.1.1.2 EMI

By its very nature, any switching converter generates electrical noise, and the circuit board designer's challenge is to minimize, contain, or attenuate such switcher-generated noise. A high-frequency switching converter, such as the LM3242, switches Ampere level currents within nanoseconds, and the traces interconnecting the associated components can act as radiating antennas. The following guidelines are offered to help to ensure that EMI is maintained within tolerable levels.

To minimize radiated noise:

- Place the LM3242 switcher, its input capacitor, and output filter inductor and capacitor close together, and make the interconnecting traces as short as possible.
- Arrange the components so that the switching current loops curl in the same direction. During the first half of each cycle, current flows from the input filter capacitor, through the internal PFET of the LM3242 and the inductor, to the output filter capacitor, then back through ground, forming a current loop. In the second half of each cycle, current is pulled up from ground, through the internal synchronous NFET of the LM3242 by the inductor, to the output filter capacitor and then back through ground, forming a second current loop. Routing these loops so the current curls in the same direction prevents magnetic field reversal between the two half-cycles and reduces radiated noise.
- Make the current loop area(s) as small as possible.

To minimize ground-plane noise:

- Reduce the amount of switching current that circulates through the ground plane: Connect the ground bumps of the LM3242 and its input filter capacitor together using generous component-side copper fill as a pseudo-ground plane. Then connect this copper fill to the system ground-plane (if one is used) with multiple vias. These multiple vias help to minimize ground bounce at the LM3242 by giving it a low-impedance ground connection.

To minimize coupling to the DC-DC converter's own voltage feedback trace:

- Route noise sensitive traces, such as the voltage feedback path, as directly as possible from the switcher FB pad to the VOUT pad of the output capacitor, but keep it away from noisy traces between the power components.

To decouple common power supply lines, series impedances may be used to strategically isolate circuits:

- Take advantage of the inherent inductance of circuit traces to reduce coupling among function blocks, by way of the power supply traces.
- Use star connection for separately routing VBATT to PVIN and VBATT_PA.
- Inserting a single ferrite bead in-line with a power supply trace may offer a favorable tradeoff in terms of board area, by allowing the use of fewer bypass capacitors.

Layout Guidelines (continued)

10.1.2 Manufacturing Considerations

The LM3242 package employs a 9-pin (3 mm × 3 mm) array of 250 micron solder balls, with a 0.4-mm pad pitch. A few simple design rules go a long way to ensuring a good layout.

- Pad size must be 0.225 ± 0.02 mm. Solder mask opening must be 0.325 ± 0.02 mm.
- As a thermal relief, connect to each pad with 7 mil wide, 7 mil long traces, and incrementally increase each trace to its optimal width. Symmetry is important to ensure the solder bumps re-flow evenly (refer to TI Application Note AN-1112 *DSBGA Wafer Level Chip Scale Package* (SNVA009).

10.1.3 LM3242 Evaluation Board

The following figures are drawn from a 4-layer board design, with notes added to highlight specific details of the DC-DC switching converter section.

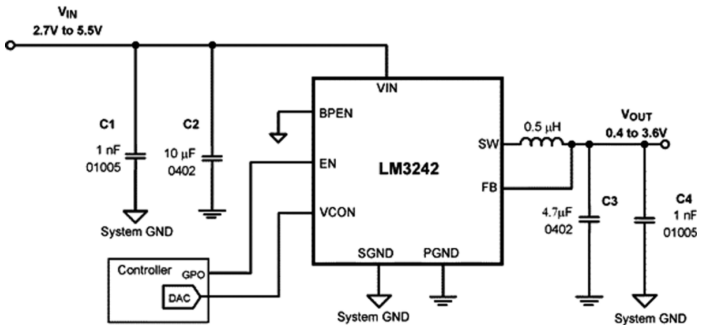


Figure 31. Simplified LM3242 RF Evaluation Board Schematic

1. Bulk Input Capacitor C2 must be placed closer to LM3242 than C1.
2. Add a 1nF (C1) on input of LM3242 for high frequency filtering.
3. Bulk Output Capacitor C3 must be placed closer to LM3242 than C4.
4. Add a 1nF (C4) on output of LM3242 for high frequency filtering.
5. Connect both GND terminals of C1 and C4 directly to System GND layer of phone board.
6. Connect bumps SGND (A2), NC (B2), BPEN (C1) directly to System GND.
7. Use 0402 caps for both C2 and C3 due to better high frequency filtering characteristics over 0603 capacitors.
8. TI has seen some improvement in high frequency filtering for small bypass caps (C1 and C4) when they are connected to System GND instead of same ground as PGND. These capacitors must be 01005 case size for minimum footprint and best high frequency characteristics.

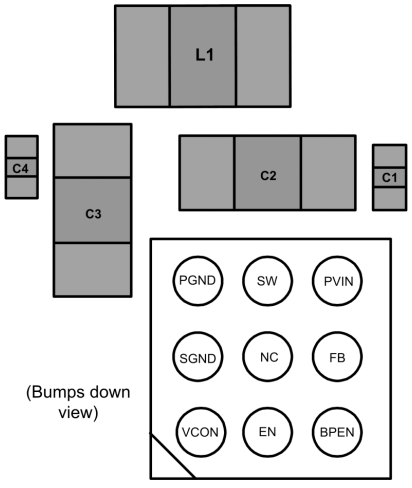


Figure 32. LM3242 Recommended Parts Placement (Top View)

Layout Guidelines (continued)

10.1.3.1 Component Placement

- PVIN
  1. Use a star connection from PVIN to LM3242 and PVIN to PA VBATT connection (V_{CC1}). Do not daisy-chain PVIN connection to LM3242 circuit and then to PA device PVIN connection.
- TOP LAYER
  1. Place a via in LM3242 SGND(A2), BPEN(C1) pads to drop and connect directly to System GND Layer 4.
  2. Place two vias at LM3242 SW solder bump to drop VSW trace to Layer 3.
  3. Connect C2 and C3 capacitor GND pads to PGND bump on LM3242 using a star connection. Place vias in C2 and C3 GND pads that connect directly to System GND Layer 4.
  4. Add 01005/0201 capacitor footprints (C1, C4) to input/output of LM3242 for improved high frequency filtering. C1 and C4 GND pads connect directly to System GND Layer 4.
  5. Place three vias at L1 inductor pad to bring up VSW trace from Layer 3 to top Layer.
- LAYER 2
  1. Make FB trace at least 10 mils (0.254 mm) wide.
  2. Isolate FB trace away from noisy nodes and connect directly to C3 output capacitor. Place a via in LM3242 SGND(A2), BPEN(C1) pads to drop and connect directly to System GND Layer 4.
- LAYER 3
  1. Make VSW trace at least 15 mils (0.381 mm) wide.
- LAYER 4 (System GND
  1. Connect C2 and C3 PGND vias to this layer.
  2. Connect C1 and C4 GND vias to this layer.
  3. Connect LM3242 SGND(A2), BPEN(C1), NC(B2) pad vias to this layer.

10.2 Layout Examples

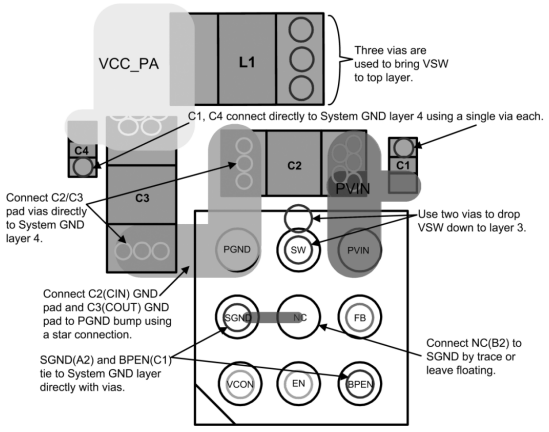


Figure 33. Board Layer 1 – PVIN and PGND Routing

Layout Examples (continued)

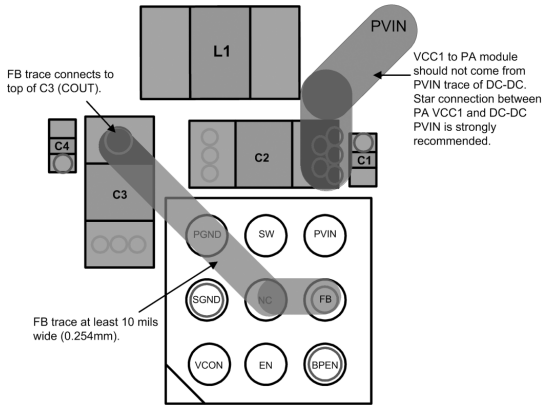


Figure 34. Board Layer 2 – FB and PVIN Routing

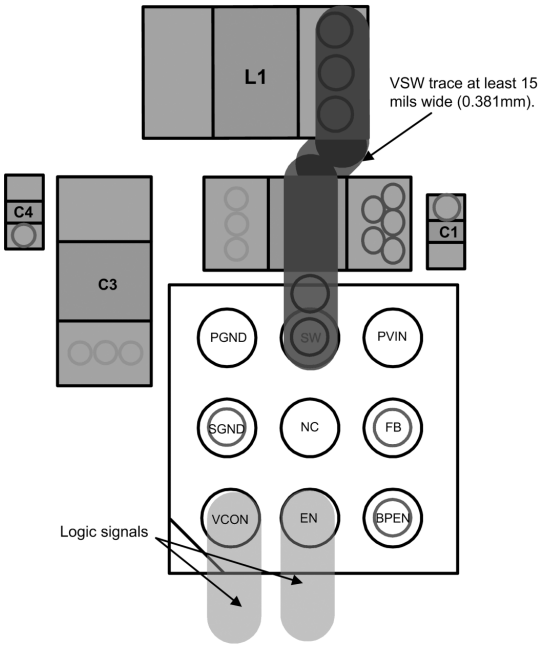


Figure 35. Board Layer 3 – SW, VCON and EN Routing

Layout Examples (continued)

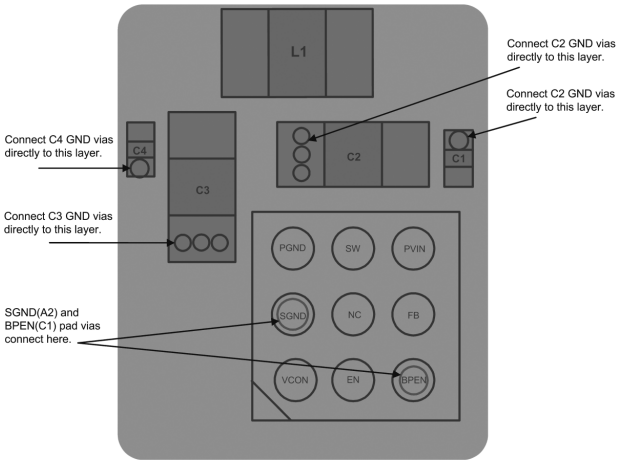


Figure 36. Board Layer 4 – System GND Plane

10.3 DSBGA Package Assembly and Use

Use of the DSBGA package requires specialized board layout, precision mounting and careful re-flow techniques, as detailed in Texas Instruments Application Note 1112. Refer to the section *Surface Mount Assembly Considerations.* For best results in assembly, alignment ordinals on the PC board must be used to facilitate placement of the device. The pad style used with DSBGA package must be the NSMD (non-solder mask defined) type. This means that the solder-mask opening is larger than the pad size. This prevents a lip that otherwise forms if the solder-mask and pad overlap, from holding the device off the surface of the board and interfering with mounting. See SNVA009 for specific instructions how to do this.

The 9-bump package used for LM3242 has 250-micron solder balls and requires 0.225-mm pads for mounting on the circuit board. The trace to each pad must enter the pad with a 90°angle to prevent debris from being caught in deep corners. Initially, the trace to each pad must be 7 mil wide, for a section approximately 7 mil long, as a thermal relief. Then each trace must neck up or down to its optimal width. The important criterion is symmetry. This ensures the solder bumps on the LM3242 re-flow evenly and that the device solders level to the board. In particular, special attention must be paid to the pads for bumps A3 and C3. Because VIN and GND are typically connected to large copper planes, inadequate thermal reliefs can result in late or inadequate re-flow of these bumps.

The DSBGA package is optimized for the smallest possible size in applications with red or infrared opaque cases. Because the DSBGA package lacks the plastic encapsulation characteristic of larger devices, it is vulnerable to light. Backside metallization and/or epoxy coating, along with front-side shading by the printed circuit board, reduce this sensitivity. However, the package has exposed die edges. In particular, DSBGA devices are sensitive to light, in the red and infrared range, shining on the package's exposed die edges.

Adding a 10-nF capacitor between VCON and ground is recommended for non-standard ESD events or environments and manufacturing processes. It prevents unexpected output voltage drift.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Documentation Support

11.2.1 Related Documentation

For additional information, see the following:

TI Application Note AN-1112 *DSBGA Wafer Level Chip Scale Package* (SNVA009).

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
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11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3242TME/NOPB	ACTIVE	DSBGA	YFQ	9	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-30 to 90	SN	Samples
LM3242TMX/NOPB	ACTIVE	DSBGA	YFQ	9	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-30 to 90	SN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

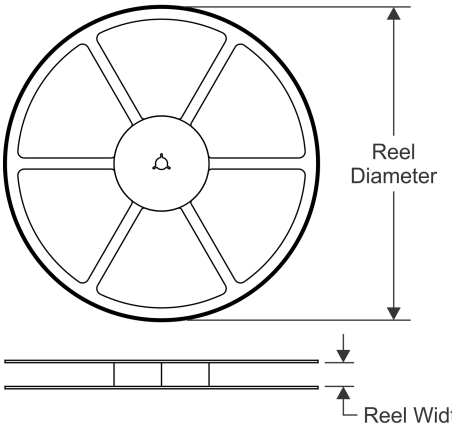
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

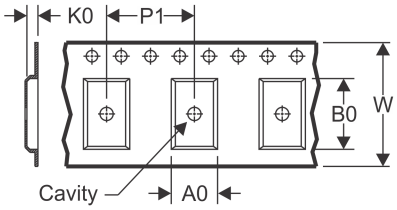
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

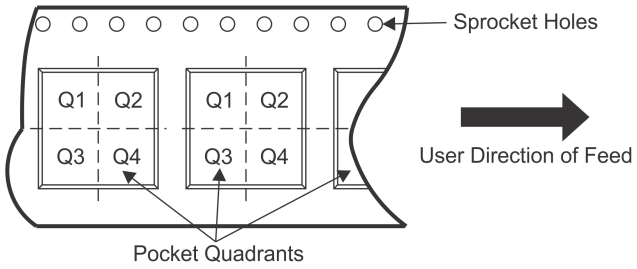


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

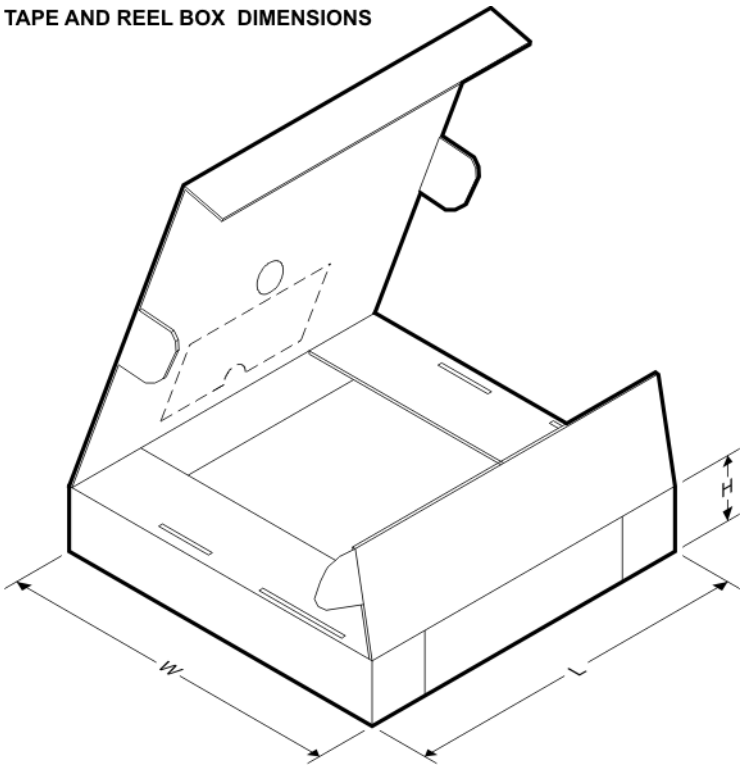
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3242TME/NOPB	DSBGA	YFQ	9	250	178.0	8.4	1.57	1.57	0.76	4.0	8.0	Q1
LM3242TMX/NOPB	DSBGA	YFQ	9	3000	178.0	8.4	1.57	1.57	0.76	4.0	8.0	Q1

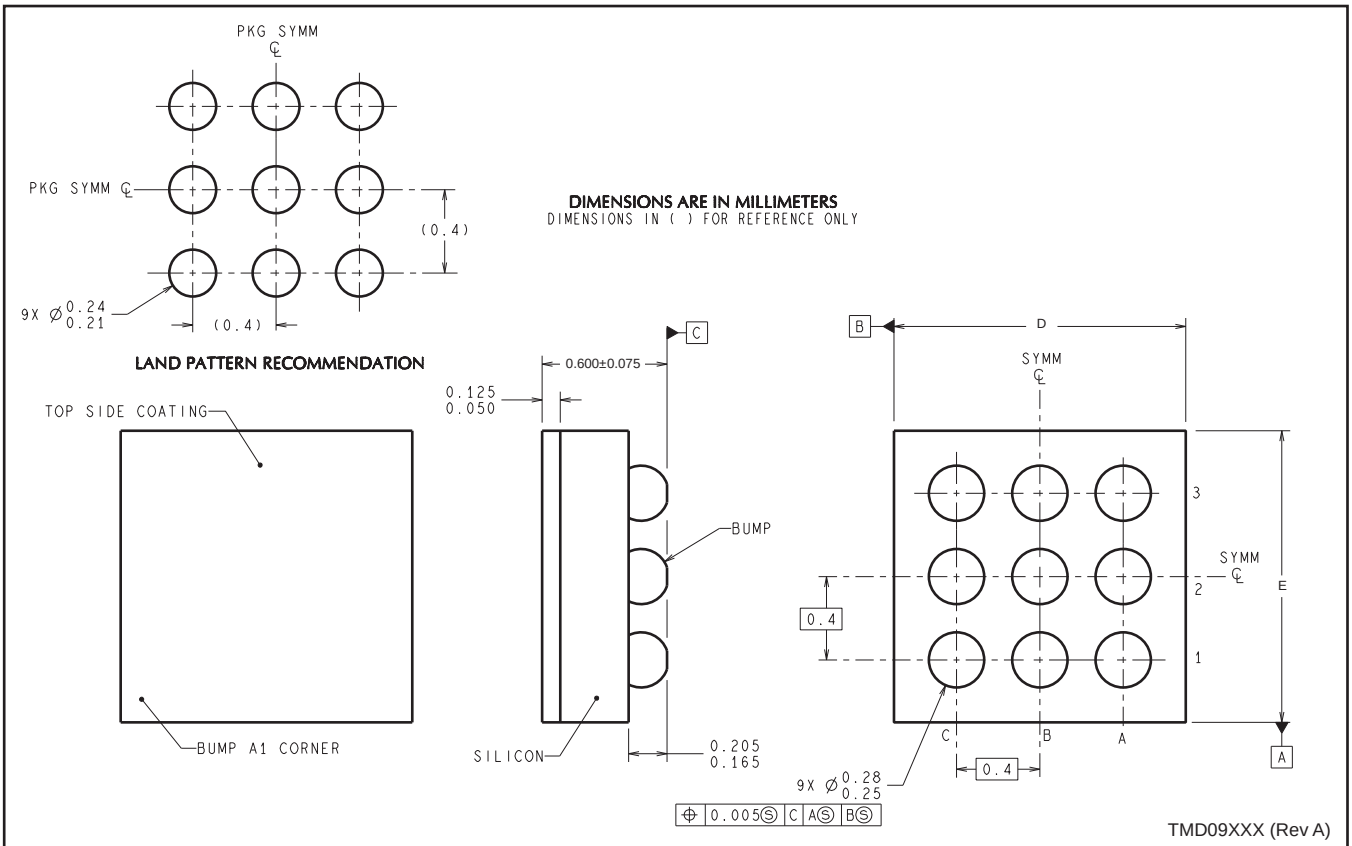
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3242TME/NOPB	DSBGA	YFQ	9	250	208.0	191.0	35.0
LM3242TMX/NOPB	DSBGA	YFQ	9	3000	208.0	191.0	35.0

YFQ0009



D: Max = 1.51 mm, Min = 1.45 mm

E: Max = 1.385 mm, Min =1.325 mm

4215077/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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