



# N-Channel 30 V (D-S) MOSFET With Schottky Diode



PRODUCT SUMMARY							
V <sub>DS</sub> (V)	30						
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 10 \text{ V}$	0.0027						
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 4.5 \text{ V}$	0.0040						
Q <sub>g</sub> typ. (nC)	17.5						
I <sub>D</sub> (A) a, g	60						
Configuration	Single						

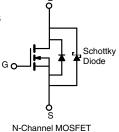
#### **FEATURES**

- TrenchFET® Gen IV power MOSFET
- SkyFET<sup>®</sup> with monolithic Schottky diode
- 100 % R<sub>q</sub> and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



### **APPLICATIONS**

- Personal computers and servers
- Synchronous buck
- Synchronous rectification
- DC/DC conversion



ORDERING INFORMATION	
Package	PowerPAK SO-8
Lead (Pb)-free and halogen-free	SiRC06DP-T1-GE3

PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V <sub>DS</sub>	30	V	
Gate-source voltage		V <sub>GS</sub>	+20, -16	v	
	T <sub>C</sub> = 25 °C		<b>60</b> g		
Continuous dusin surrent (T. 150 °C)	T <sub>C</sub> = 70 °C	_	60 <sup>g</sup>		
Continuous drain current (T <sub>J</sub> = 150 °C)	T <sub>A</sub> = 25 °C	I <sub>D</sub>	32 b, c		
	T <sub>A</sub> = 70 °C		25.6 <sup>b, c</sup>		
Pulsed drain current (t = 300 μs)		I <sub>DM</sub>	100	A	
Continuous source-drain diode current	T <sub>C</sub> = 25 °C		60 g		
	T <sub>A</sub> = 25 °C	I <sub>S</sub>	7.1 <sup>b, c</sup>		
Single pulse avalanche current	1 00 mll	I <sub>AS</sub>	15		
Single pulse avalanche energy  L = 0.3 mH		E <sub>AS</sub>	11.25	mJ	
	T <sub>C</sub> = 25 °C		50		
Manian and a sure discipation	T <sub>C</sub> = 70 °C	_	32	14/	
Maximum power dissipation	T <sub>A</sub> = 25 °C	P <sub>D</sub>	5 b, c	W	
	T <sub>A</sub> = 70 °C		3.2 b, c		
Operating junction and storage temperature range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	%0	
Soldering recommendations (peak temperature) d, e			260	°C	

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient b,f	t ≤ 10 s	$R_{thJA}$	20	25	°C/W
Maximum junction-to-case (drain)	Steady state	$R_{thJC}$	1.9	2.5	C/ VV

#### Notes

- a. Based on  $T_C = 25 \, ^{\circ}C$
- b. Surface mounted on 1" x 1" FR4 board
- c. t = 10 s
- d. See solder profile (<a href="www.vishay.com/doc?73257">www.vishay.com/doc?73257</a>). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- f. Maximum under steady state conditions is 70 °C/W
- g. Package limit

# Vishay Siliconix

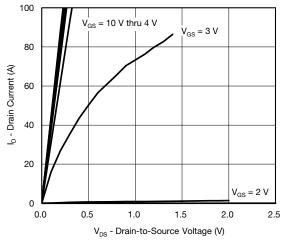
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-source breakdown voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	30	-	-		
Drain-source breakdown voltage (transient) <sup>c</sup>	V <sub>DSt</sub>	V <sub>GS</sub> = 0 V, I <sub>D(aval)</sub> = 15 A, t <sub>transcient</sub> ≤ 50 ns	36	-	-	V	
Gate-source threshold voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1	-	2.1		
Gate-source leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = +20, -16 V	-	-	± 100	nA	
Zana anaka walka na dinaka awana t		V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V	-	0.02	0.20	А	
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C	-	0.13	1	mA	
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	30	-	-	Α	
Drain accuracy on atota vaciationas 3	0	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 15 A	-	0.0022	0.0027	0	
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 10 A	-	0.0032	0.0040	10 Ω	
Forward transconductance <sup>a</sup>	9fs	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 15 A	-	120	-	S	
Dynamic <sup>b</sup>							
Input capacitance	C <sub>iss</sub>		-	2455	-		
Output capacitance	Coss	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V, f = 1 MHz	-	350	-	ne.	
Reverse transfer capacitance	C <sub>rss</sub>	V <sub>DS</sub> = 13 V, V <sub>GS</sub> = 0 V, I = I IVID2	-	60	-	pF	
C <sub>rss</sub> /C <sub>iss</sub> ratio		]	-	0.025	0.050		
<del>-</del>	0	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 15 A	-	38.5	58		
Total gate charge	$Q_g$	V 15VV 45VI 15A	-	17.5	27		
Gate-source charge	Q <sub>gs</sub>	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 15 \text{ A}$	-	6.3	-	nC	
Gate-drain charge	Q <sub>gd</sub>		-	2.8	-		
Output charge	Q <sub>oss</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V	-	29	-		
Gate resistance	$R_g$	f = 1 MHz	0.4	1.15	2	Ω	
Turn-on delay time	t <sub>d(on)</sub>		-	12	24		
Rise time	t <sub>r</sub>	$V_{DD} = 15 \text{ V}, R_L = 1.5 \Omega$	-	14	28		
Turn-off delay time	t <sub>d(off)</sub>	$I_D \cong 10 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	-	23	46	1	
Fall time	t <sub>f</sub>	]	-	8	16		
Turn-on delay time	t <sub>d(on)</sub>		-	29	58	ns	
Rise time	t <sub>r</sub>	$V_{DD} = 15 \text{ V}, R_L = 1.5 \Omega$	-	50	100		
Turn-off delay time	t <sub>d(off)</sub>	$I_D\cong 10$ A, $V_{GEN}=4.5$ V, $R_g=1$ $\Omega$	-	20	40		
Fall time	t <sub>f</sub>	]	-	9	18		
Drain-Source Body Diode Characteristic	s						
Continuous source-drain diode current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	-	-	60	^	
ulse diode forward current (t = 100 µs)			-	-	100	A	
Body diode voltage	V <sub>SD</sub>	I <sub>S</sub> = 5 A	-	0.47	0.7	V	
Body diode reverse recovery time	t <sub>rr</sub>		-	31	62	ns	
Body diode reverse recovery charge	Q <sub>rr</sub>	I <sub>F</sub> = 10 A, di/dt = 100 A/μs,	-	19	38	nC	
Reverse recovery fall time	t <sub>a</sub>	T <sub>J</sub> = 25 °C	-	16	-	ns	
Reverse recovery rise time	t <sub>b</sub>	† †	-	15	-		

### Notes

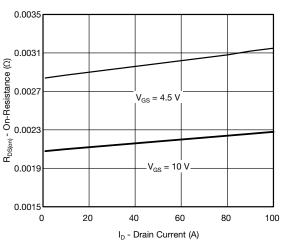
- a. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 %
- b. Guaranteed by design, not subject to production testing
- c.  $T_{CASE} = 25$  °C; Expected voltage stress during 100 % UIS test. Production data log is not available

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

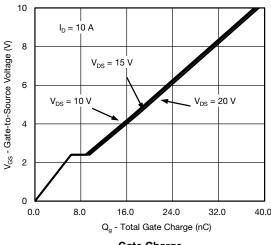




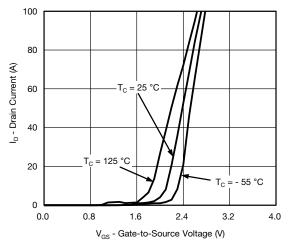
### **Output Characteristics**



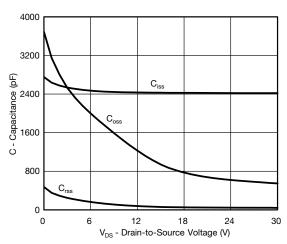
## On-Resistance vs. Drain Current



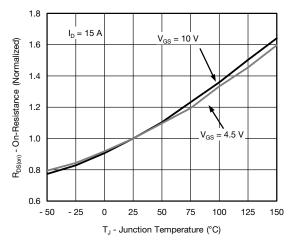
**Gate Charge** 



**Transfer Characteristics** 

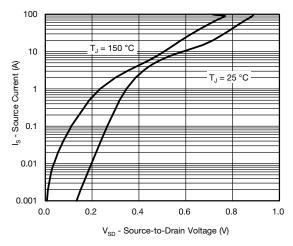


## Capacitance

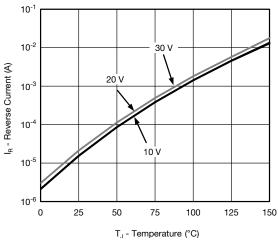


On-Resistance vs. Junction Temperature

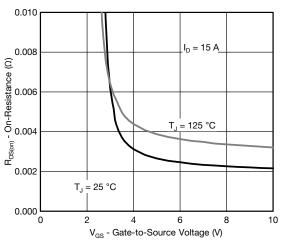




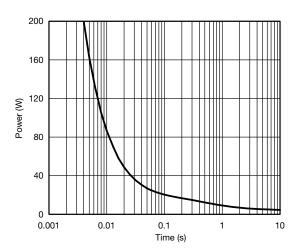
### Source-Drain Diode Forward Voltage



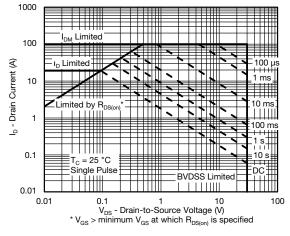
**Reverse Current vs. Junction Temperature** 



On-Resistance vs. Gate-to-Source Voltage

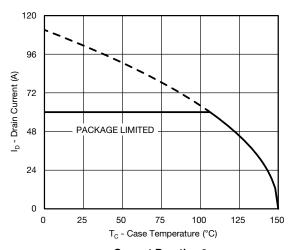


Single Pulse Power, Junction-to-Ambient

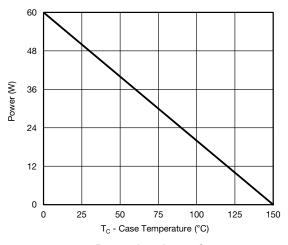


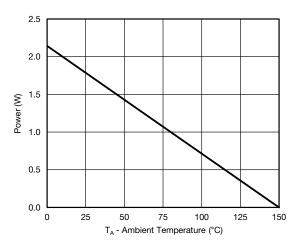
Safe Operating Area





Current Derating a





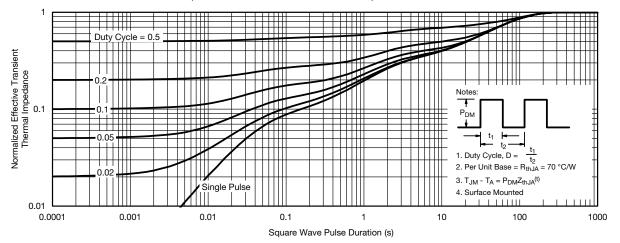
Power, Junction-to-Case

Power, Junction-to-Ambient

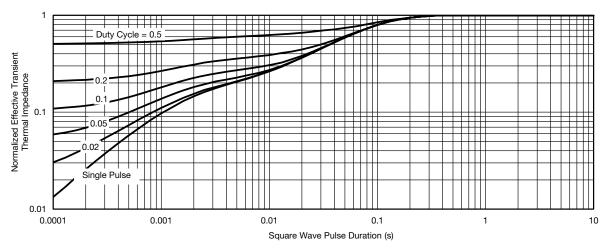
#### Note

a. The power dissipation P<sub>D</sub> is based on T<sub>J</sub> max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit





Normalized Thermal Transient Impedance, Junction-to-Ambient

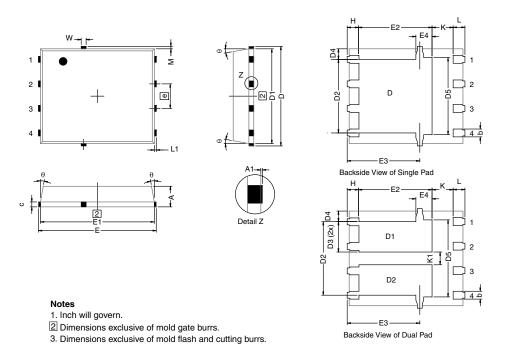


Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see <a href="https://www.vishay.com/ppg?62942">www.vishay.com/ppg?62942</a>.



# PowerPAK® SO-8, (Single/Dual)

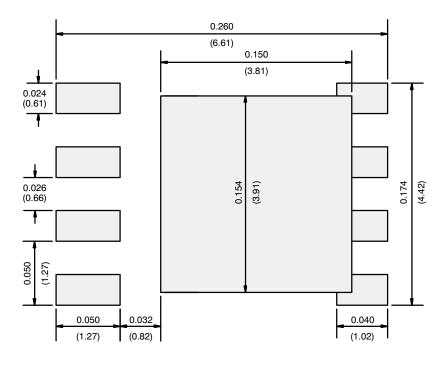


DIM.		MILLIMETERS		INCHES			
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX	
Α	0.97	1.04	1.12	0.038	0.041	0.044	
A1		-	0.05	0	-	0.002	
b	0.33	0.41	0.51	0.013	0.016	0.020	
С	0.23	0.28	0.33	0.009	0.011	0.013	
D	5.05	5.15	5.26	0.199	0.203	0.207	
D1	4.80	4.90	5.00	0.189	0.193	0.197	
D2	3.56	3.76	3.91	0.140	0.148	0.154	
D3	1.32	1.50	1.68	0.052	0.059	0.066	
D4		0.57 typ.		0.0225 typ.			
D5		3.98 typ.		0.157 typ.			
E	6.05	6.15	6.25	0.238	0.242	0.246	
E1	5.79	5.89	5.99	0.228	0.232	0.236	
E2	3.48	3.66	3.84	0.137	0.144	0.151	
E3	3.68	3.78	3.91	0.145	0.149	0.154	
E4		0.75 typ.			0.030 typ.		
е		1.27 BSC		0.050 BSC			
K		1.27 typ.		0.050 typ.			
K1	0.56	-	-	0.022	-	-	
Н	0.51	0.61	0.71	0.020	0.024	0.028	
L	0.51	0.61	0.71	0.020	0.024	0.028	
L1	0.06	0.13	0.20	0.002	0.005	0.008	
θ	0°	=	12°	0°	-	12°	
W	0.15	0.25	0.36	0.006	0.010	0.014	
M	0.125 typ.			0.005 typ.			

Revison: 13-Feb-17 1 Document Number: 71655



## RECOMMENDED MINIMUM PADS FOR PowerPAK® SO-8 Single



Recommended Minimum Pads Dimensions in Inches/(mm)

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APPLICATION NOTE



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