

SN74LVC16373A 16-Bit Transparent D-Type Latch With 3-State Outputs

1 Features

- Member of the Texas Instruments Widebus™ Family
- Operates From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 4.2 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- I_{off} Supports Live-Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 1000-V Charged-Device Model (C101)

2 Applications

- Servers
- PCs and Notebooks
- Network Switches
- Wearable Health and Fitness Devices
- Telecom Infrastructures
- Electronic Points of Sale

3 Description

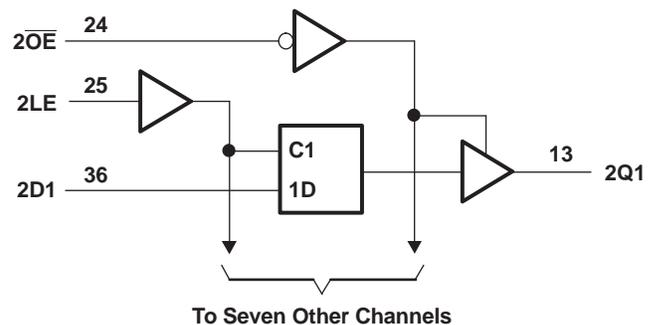
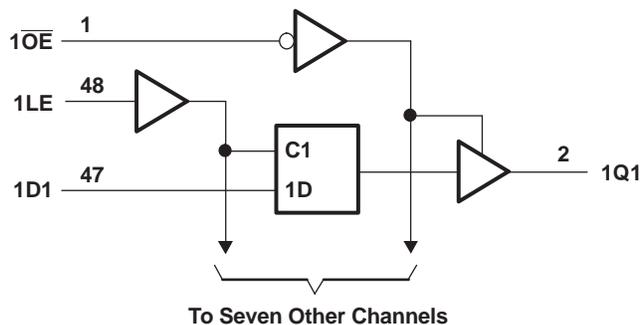
The SN74LVC16373A device is a 16-bit transparent D-type latch which is designed for 1.65-V to 3.6-V V_{CC} operation.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---------------|---------------------------|--------------------|
| SN74LVC16373A | TSSOP (48) | 12.50 mm × 6.10 mm |
| | TVSOP (48) | 9.70 mm × 4.40 mm |
| | SSOP (48) | 15.80 mm × 7.49 mm |
| | BGA MICROSTAR JUNIOR (56) | 7.00 mm × 4.50 mm |
| | BGA MICROSTAR JUNIOR (54) | 8.00 mm × 5.50 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic



Pin numbers shown are for the DGG, DGV, and DL packages.



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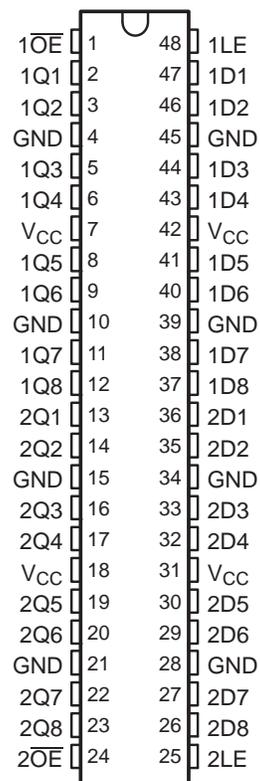
5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision A (September 2005) to Revision B | Page |
|---|-------------|
| • Updated document to new TI data sheet format | 1 |
| • Removed Ordering Information table | 1 |
| • Added Applications | 1 |
| • Added Device Information table | 1 |
| • Added Handling Ratings table | 6 |
| • Changed MAX ambient temperature to 125°C | 7 |
| • Added Thermal Information table | 7 |
| • Added Typical Characteristics | 9 |

6 Pin Configuration and Functions

DGG, DGV, OR DL PACKAGE
(TOP VIEW)



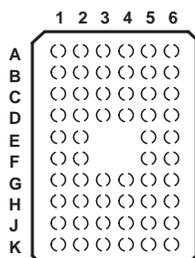
Pin Functions

| PIN | | I/O | DESCRIPTION |
|-----|-----------------|-----|---------------|
| NO. | NAME | | |
| 1 | \overline{OE} | I | Output Enable |
| 2 | 1Q1 | O | 1Q1 Output |
| 3 | 1Q2 | O | 1Q2 Output |
| 4 | GND | — | Ground Pin |
| 5 | 1Q3 | O | 1Q3 Output |
| 6 | 1Q4 | O | 1Q4 Output |
| 7 | VCC | — | Power Pin |
| 8 | 1Q5 | O | 1Q5 Output |
| 9 | 1Q6 | O | 1Q6 Output |
| 10 | GND | — | Ground Pin |
| 11 | 1Q7 | O | 1Q7 Output |
| 12 | 1Q8 | O | 1Q8 Output |
| 13 | 2Q1 | O | 2Q1 Output |
| 14 | 2Q2 | O | 2Q2 Output |
| 15 | GND | — | Ground Pin |
| 16 | 2Q3 | O | 2Q3 Output |
| 17 | 2Q4 | O | 2Q4 Output |
| 18 | VCC | — | Power Pin |
| 19 | 2Q5 | O | 2Q5 Output |
| 20 | 2Q6 | O | 2Q6 Output |

Pin Functions (continued)

| PIN | | I/O | DESCRIPTION |
|-----|-------------------|-----|-----------------|
| NO. | NAME | | |
| 21 | GND | — | Ground Pin |
| 22 | 2Q7 | O | 2Q7 Output |
| 23 | 2Q8 | O | 2Q8 Output |
| 24 | 2 \overline{OE} | O | Output Enable 2 |
| 25 | 2LE | I | Latch Enable 2 |
| 26 | 2D8 | I | 2D8 Input |
| 27 | 2D7 | I | 2D7 Input |
| 28 | GND | — | Ground Pin |
| 29 | 2D6 | I | 2D6 Input |
| 30 | 2D5 | I | 2D5 Input |
| 31 | VCC | — | Power Pin |
| 32 | 2D4 | I | 2D4 Input |
| 33 | 2D3 | I | 2D3 Input |
| 34 | GND | — | Ground Pin |
| 35 | 2D2 | I | 2D2 Input |
| 36 | 2D1 | I | 2D1 Input |
| 37 | 1D8 | I | 1D8 Input |
| 38 | 1D7 | I | 1D7 Input |
| 39 | GND | — | Ground Pin |
| 40 | 1D6 | I | 1D6 Input |
| 41 | 1D5 | I | 1D5 Input |
| 42 | VCC | — | Power Pin |
| 43 | 1D4 | I | 1D4 Input |
| 44 | 1D3 | I | 1D3 Input |
| 45 | GND | — | Ground Pin |
| 46 | 1D2 | I | 1D2 Input |
| 47 | 1D1 | I | 1D1 Input |
| 48 | 1LE | I | Latch Enable 1 |

**GQL OR ZQL PACKAGE
(TOP VIEW)**

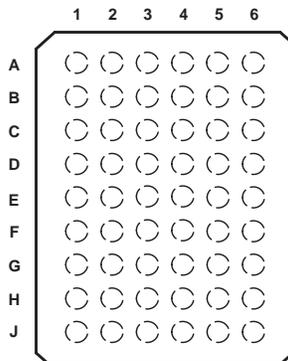


Pin Assignments⁽¹⁾ (56-Ball GQL or ZQL Package)

| | 1 | 2 | 3 | 4 | 5 | 6 |
|----------|------------------|-----|-----------------|-----------------|-----|-----|
| A | $\overline{1OE}$ | NC | NC | NC | NC | 1LE |
| B | 1Q2 | 1Q1 | GND | GND | 1D1 | 1D2 |
| C | 1Q4 | 1Q3 | V _{CC} | V _{CC} | 1D3 | 1D4 |
| D | 1Q6 | 1Q5 | GND | GND | 1D5 | 1D6 |
| E | 1Q8 | 1Q7 | | | 1D7 | 1D8 |
| F | 2Q1 | 2Q2 | | | 2D2 | 2D1 |
| G | 2Q3 | 2Q4 | GND | GND | 2D4 | 2D3 |
| H | 2Q5 | 2Q6 | V _{CC} | V _{CC} | 2D6 | 2D5 |
| J | 2Q7 | 2Q8 | GND | GND | 2D8 | 2D7 |
| K | $\overline{2OE}$ | NC | NC | NC | NC | 2LE |

(1) NC – No internal connection

**GRD OR ZRD PACKAGE
(TOP VIEW)**



Pin Assignments⁽¹⁾ (54-Ball GRD or ZRD Package)

| | 1 | 2 | 3 | 4 | 5 | 6 |
|----------|-----|-----|------------------|-----------------|-----|-----|
| A | 1Q1 | NC | $\overline{1OE}$ | 1LE | NC | 1D1 |
| B | 1Q3 | 1Q2 | NC | NC | 1D2 | 1D3 |
| C | 1Q5 | 1Q4 | V _{CC} | V _{CC} | 1D4 | 1D5 |
| D | 1Q7 | 1Q6 | GND | GND | 1D6 | 1D7 |
| E | 2Q1 | 1Q8 | GND | GND | 1D8 | 2D1 |
| F | 2Q3 | 2Q2 | GND | GND | 2D2 | 2D3 |
| G | 2Q5 | 2Q4 | V _{CC} | V _{CC} | 2D4 | 2D5 |
| H | 2Q7 | 2Q6 | NC | NC | 2D6 | 2D7 |
| J | 2Q8 | NC | $\overline{2OE}$ | 2LE | NC | 2D8 |

(1) NC – No internal connection

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|-----------------|---|--------------------|-----------------------|------|
| V _{CC} | Supply voltage range | –0.5 | 6.5 | V |
| V _I | Input voltage range ⁽²⁾ | –0.5 | 6.5 | V |
| V _O | Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾ | –0.5 | 6.5 | V |
| V _O | Voltage range applied to any output in the high or low state ⁽²⁾⁽³⁾ | –0.5 | V _{CC} + 0.5 | V |
| I _{IK} | Input clamp current | V _I < 0 | –50 | mA |
| I _{OK} | Output clamp current | V _O < 0 | –50 | mA |
| I _O | Continuous output current | | ±50 | mA |
| | Continuous current through each V _{CC} or GND | | ±100 | mA |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

7.2 Handling Ratings

| | | MIN | MAX | UNIT | |
|--------------------|---------------------------|--|-----|------|---|
| T _{stg} | Storage temperature range | –65 | 150 | °C | |
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾ | 0 | 2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾ | 0 | 1000 | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | | MIN | MAX | UNIT |
|-----------------|-------------------------------------|------------------------------------|------------------------|------------------------|------|
| V _{CC} | Supply voltage | Operating | 1.65 | 3.6 | V |
| | | Data retention only | 1.5 | | |
| V _{IH} | High-level input voltage | V _{CC} = 1.65 V to 1.95 V | 0.65 × V _{CC} | | V |
| | | V _{CC} = 2.3 V to 2.7 V | 1.7 | | |
| | | V _{CC} = 2.7 V to 3.6 V | 2 | | |
| V _{IL} | Low-level input voltage | V _{CC} = 1.65 V to 1.95 V | | 0.35 × V _{CC} | V |
| | | V _{CC} = 2.3 V to 2.7 V | | 0.7 | |
| | | V _{CC} = 2.7 V to 3.6 V | | 0.8 | |
| V _I | Input voltage | | 0 | 5.5 | V |
| V _O | Output voltage | High or low state | 0 | V _{CC} | V |
| | | High-impedance state | 0 | 5.5 | |
| I _{OH} | High-level output current | V _{CC} = 1.65 V | | –4 | mA |
| | | V _{CC} = 2.3 V | | –8 | |
| | | V _{CC} = 2.7 V | | –12 | |
| | | V _{CC} = 3 V | | –24 | |
| I _{OL} | Low-level output current | V _{CC} = 1.65 V | | 4 | mA |
| | | V _{CC} = 2.3 V | | 8 | |
| | | V _{CC} = 2.7 V | | 12 | |
| | | V _{CC} = 3 V | | 24 | |
| Δt/Δv | Input transition rise and fall rate | | | 10 | ns/V |
| T _A | Operating free-air temperature | | –40 | 125 | °C |

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

7.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | DL | UNIT |
|-------------------------------|--|---------|------|
| | | 48 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 68.4 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 34.7 | |
| R _{θJB} | Junction-to-board thermal resistance | 41.0 | |
| Ψ _{JT} | Junction-to-top characterization parameter | 12.3 | |
| Ψ _{JB} | Junction-to-board characterization parameter | 40.4 | |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | n/a | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP ⁽¹⁾ | MAX | UNIT | |
|--------------------------|--|-----------------|-----------------------|--------------------|------|------|----|
| V _{OH} | I _{OH} = -100 μA | 1.65 V to 3.6 V | V _{CC} - 0.2 | | | V | |
| | I _{OH} = -4 mA | 1.65 V | 1.2 | | | | |
| | I _{OH} = -8 mA | 2.3 V | 1.7 | | | | |
| | I _{OH} = -12 mA | 2.7 V | 2.2 | | | | |
| | | 3 V | 2.4 | | | | |
| I _{OH} = -24 mA | 3 V | 2.2 | | | | | |
| V _{OL} | I _{OL} = 100 μA | 1.65 V to 3.6 V | | | 0.2 | V | |
| | I _{OL} = 4 mA | 1.65 V | | | 0.45 | | |
| | I _{OL} = 8 mA | 2.3 V | | | 0.7 | | |
| | I _{OL} = 12 mA | 2.7 V | | | 0.4 | | |
| | I _{OL} = 24 mA | 3 V | | | 0.55 | | |
| I _I | V _I = 0 to 5.5 V | 3.6 V | | | ±5 | μA | |
| I _{off} | V _I or V _O = 5.5 V | 0 | | | ±10 | μA | |
| I _{OZ} | V _O = 0 to 5.5 V | 3.6 V | | | ±10 | μA | |
| I _{CC} | V _I = V _{CC} or GND | 3.6 V | I _O = 0 | | | 20 | μA |
| | 3.6 V ≤ V _I ≤ 5.5 V ⁽²⁾ | | | | | 20 | |
| ΔI _{CC} | One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND | 2.7 V to 3.6 V | | | 500 | μA | |
| C _i | V _I = V _{CC} or GND | 3.3 V | | | 5 | pF | |
| C _o | V _O = V _{CC} or GND | 3.3 V | | | 6.5 | pF | |

 (1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

(2) This applies in the disabled state only.

7.6 Timing Requirements

 over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

| | | V _{CC} = 1.8 V ± 0.15 V | | V _{CC} = 2.5 V ± 0.2 V | | V _{CC} = 2.7 V | | V _{CC} = 3.3 V ± 0.3 V | | UNIT |
|-----------------|-----------------------------|----------------------------------|-----|---------------------------------|-----|-------------------------|-----|---------------------------------|-----|------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _w | Pulse duration, LE high | 3.3 | | 3.3 | | 3.3 | | 3.3 | | ns |
| t _{su} | Setup time, data before LE↓ | 1.6 | | 1.2 | | 1.7 | | 1.7 | | ns |
| t _h | Hold time, data after LE↓ | 1 | | 1.1 | | 1.2 | | 1.2 | | ns |

7.7 Switching Characteristics

 over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

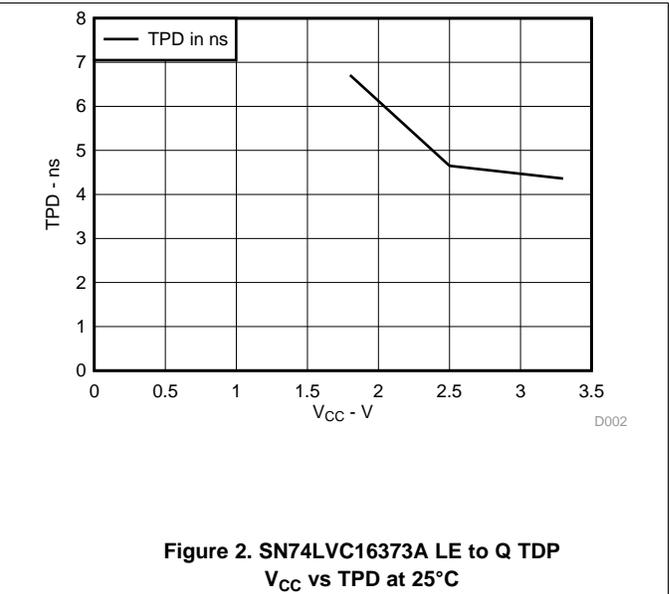
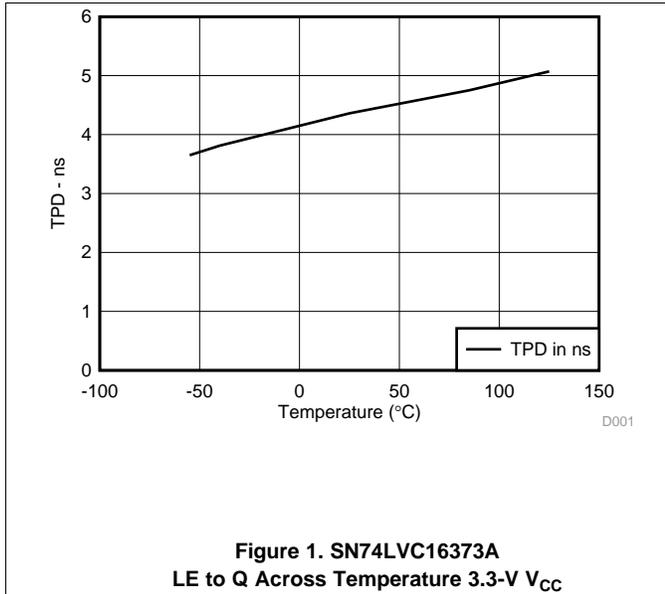
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 1.8 V ± 0.15 V | | V _{CC} = 2.5 V ± 0.2 V | | V _{CC} = 2.7 V | | V _{CC} = 3.3 V ± 0.3 V | | UNIT |
|------------------|------------------------|-------------|----------------------------------|-----|---------------------------------|-----|-------------------------|-----|---------------------------------|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _{pd} | D | Q | 1.5 | 6.4 | 1 | 4.2 | 1 | 4.9 | 1.6 | 4.2 | ns |
| | LE | | 1.5 | 7.1 | 1 | 4.8 | 1 | 5.3 | 2.1 | 4.6 | |
| t _{en} | $\overline{\text{OE}}$ | Q | 1.5 | 6.7 | 1 | 4.7 | 1 | 5.7 | 1.3 | 4.7 | ns |
| t _{dis} | $\overline{\text{OE}}$ | Q | 1.5 | 8.4 | 1 | 5 | 1 | 6.3 | 2.5 | 5.9 | ns |

7.8 Operating Characteristics

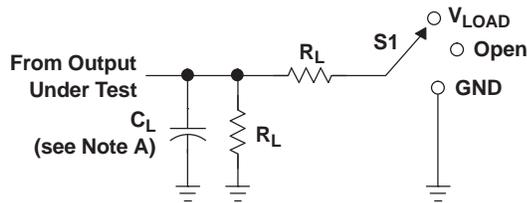
 T_A = 25°C

| PARAMETER | TEST CONDITIONS | V _{CC} = 1.8 V | V _{CC} = 2.5 V | V _{CC} = 3.3 V | UNIT | |
|---|------------------|-------------------------|-------------------------|-------------------------|------|----|
| | | TYP | TYP | TYP | | |
| C _{pd} Power dissipation capacitance per latch | Outputs enabled | f = 10 MHz | 32 | 35 | 39 | pF |
| | Outputs disabled | | 4 | 4 | 6 | |

7.9 Typical Characteristics



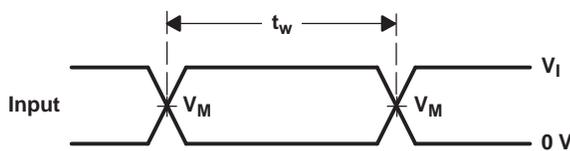
8 Parameter Measurement Information



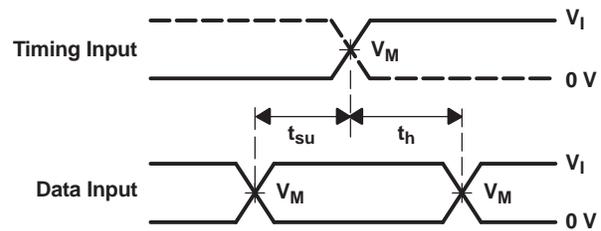
LOAD CIRCUIT

| TEST | S1 |
|-------------------|------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | V_{LOAD} |
| t_{PHZ}/t_{PZH} | GND |

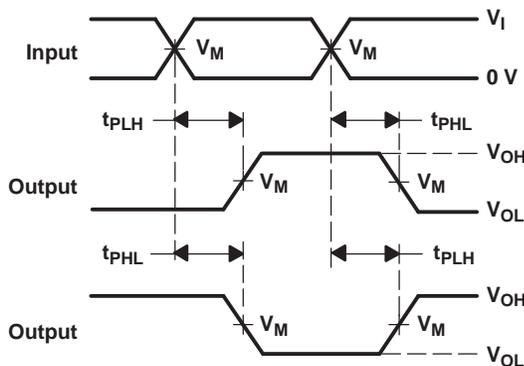
| V_{CC} | INPUTS | | V_M | V_{LOAD} | C_L | R_L | V_{Δ} |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
| | V_I | t_r/t_f | | | | | |
| $1.8\text{ V} \pm 0.15\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k Ω | 0.15 V |
| $2.5\text{ V} \pm 0.2\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| 2.7 V | 2.7 V | $\leq 2.5\text{ ns}$ | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| $3.3\text{ V} \pm 0.3\text{ V}$ | 2.7 V | $\leq 2.5\text{ ns}$ | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |



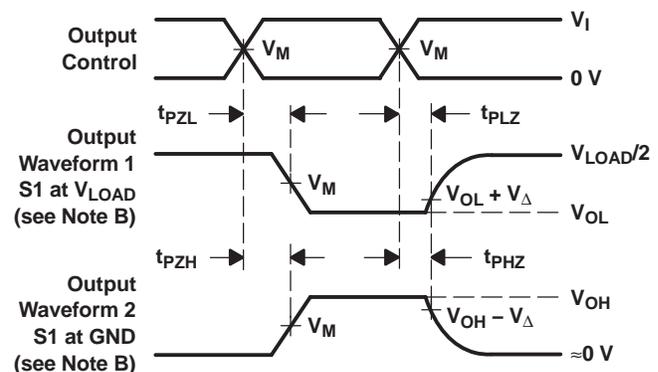
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

9 Detailed Description

9.1 Overview

The SN74LVC16373A device is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. The device can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components. \overline{OE} does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state. Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment. To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

9.2 Functional Block Diagram

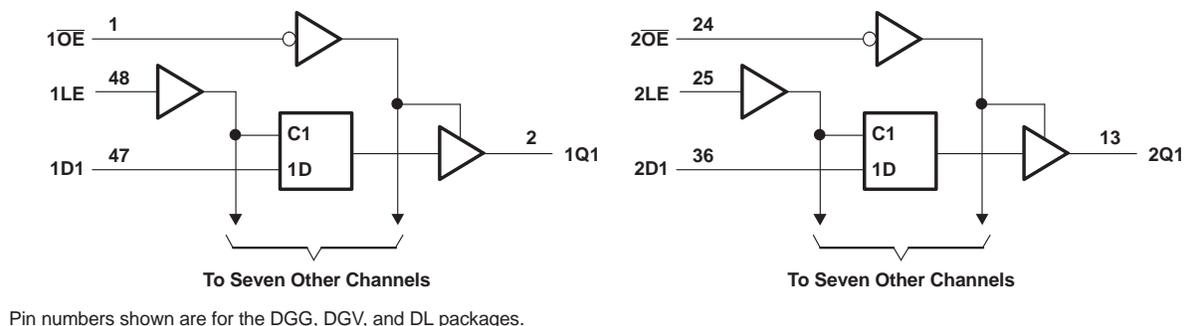


Figure 4. Logic Diagram (Positive Logic)

9.3 Feature Description

- Wide operating voltage range
 - Operates from 1.65 V to 3.6 V
- Allows down voltage translation
 - Inputs accept voltages to 5.5 V
- I_{off} feature
 - Allows voltages on the inputs and outputs when V_{CC} is 0 V

9.4 Device Functional Modes

Function Table
(Each Latch)

| INPUTS | | | OUTPUT Q |
|-----------------|----|---|-------------|
| \overline{OE} | LE | D | |
| L | H | H | H |
| L | H | L | L |
| L | L | X | Q_0 |
| H | X | X | Z |

10 Application and Implementation

10.1 Application Information

The SN74LVC16373A device is a high drive CMOS device that can be used for a multitude of bus-interface type applications where the data needs to be retained or latched. It can produce 24 mA of drive current at 3.3 V. Therefore, this device is ideal for driving multiple outputs and for high speed applications up to 100 Mhz. The inputs are 5.5 V tolerant allowing it to translate down to V_{CC} .

10.2 Typical Application

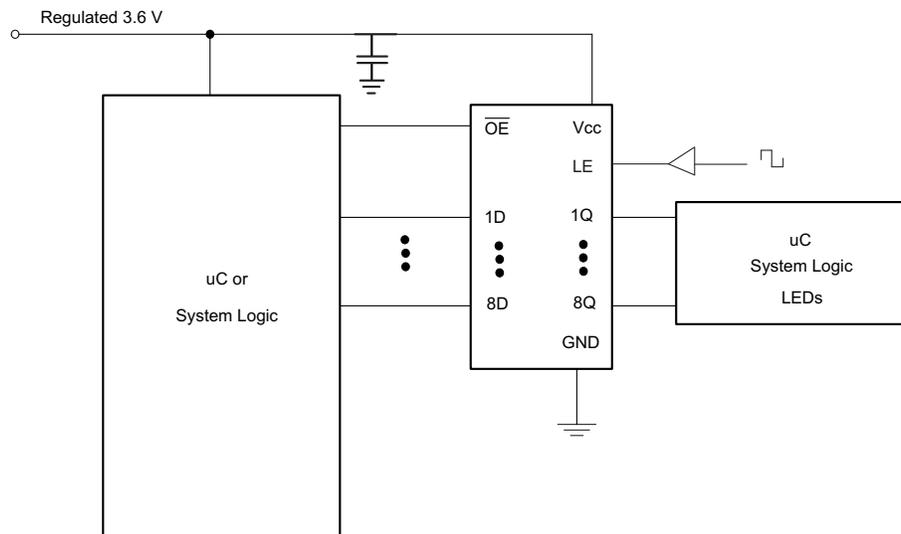


Figure 5. Typical Application Diagram

10.2.1 Design Requirements

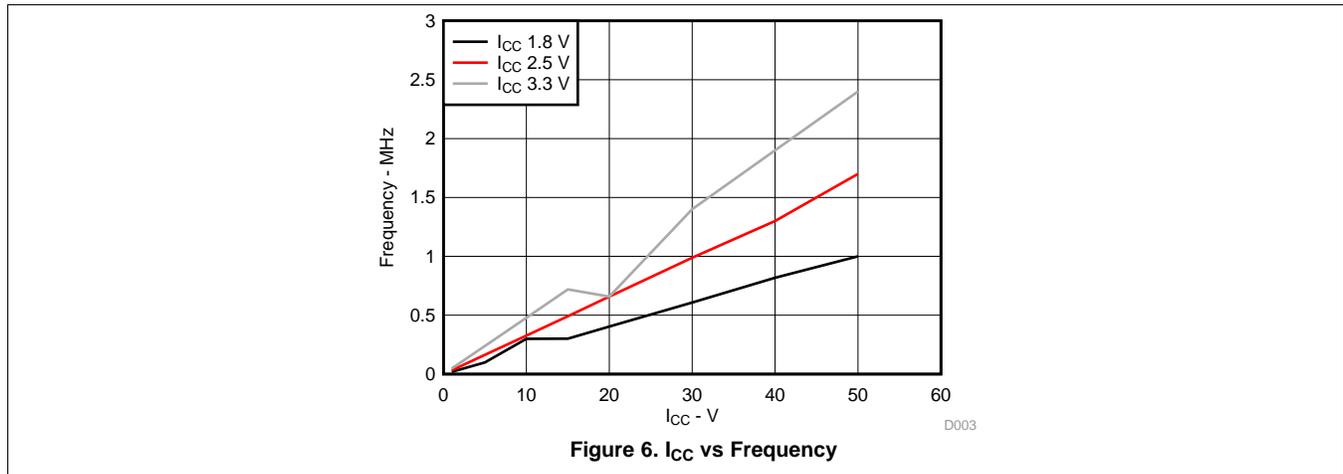
This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads; therefore, routing and load conditions should be considered to prevent ringing.

10.2.2 Detailed Design Procedure

1. Recommended Input Conditions
 - Rise time and fall time specs: See $(\Delta t/\Delta V)$ in the [Recommended Operating Conditions](#) table.
 - Specified high and low levels: See $(V_{IH}$ and $V_{IL})$ in the [Recommended Operating Conditions](#) table.
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC} .
2. Recommend Output Conditions
 - Load currents should not exceed 50 mA per output and 100 mA total for the part.
 - Outputs should not be pulled above V_{CC} .

Typical Application (continued)

10.2.3 Application Curves



11 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μf is recommended; if there are multiple V_{CC} pins, then 0.01 μf or 0.022 μf is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μf and a 1 μf are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

12 Layout

12.1 Layout Guidelines

When using multiple bit logic devices inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. [Figure 7](#) specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver.

12.2 Layout Example

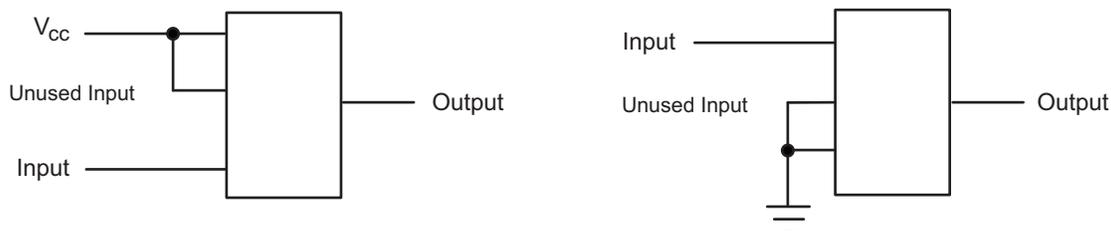


Figure 7. Layout Diagram

13 Device and Documentation Support

13.1 Trademarks

Widebus is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|-------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| 74LVC16373ADGGRG4 | ACTIVE | TSSOP | DGG | 48 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC16373A | Samples |
| 74LVC16373ADGVRE4 | ACTIVE | TVSOP | DGV | 48 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LD373A | Samples |
| SN74LVC16373ADGGR | ACTIVE | TSSOP | DGG | 48 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC16373A | Samples |
| SN74LVC16373ADGVR | ACTIVE | TVSOP | DGV | 48 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LD373A | Samples |
| SN74LVC16373ADL | ACTIVE | SSOP | DL | 48 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC16373A | Samples |
| SN74LVC16373ADLG4 | ACTIVE | SSOP | DL | 48 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC16373A | Samples |
| SN74LVC16373ADLR | ACTIVE | SSOP | DL | 48 | 1000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC16373A | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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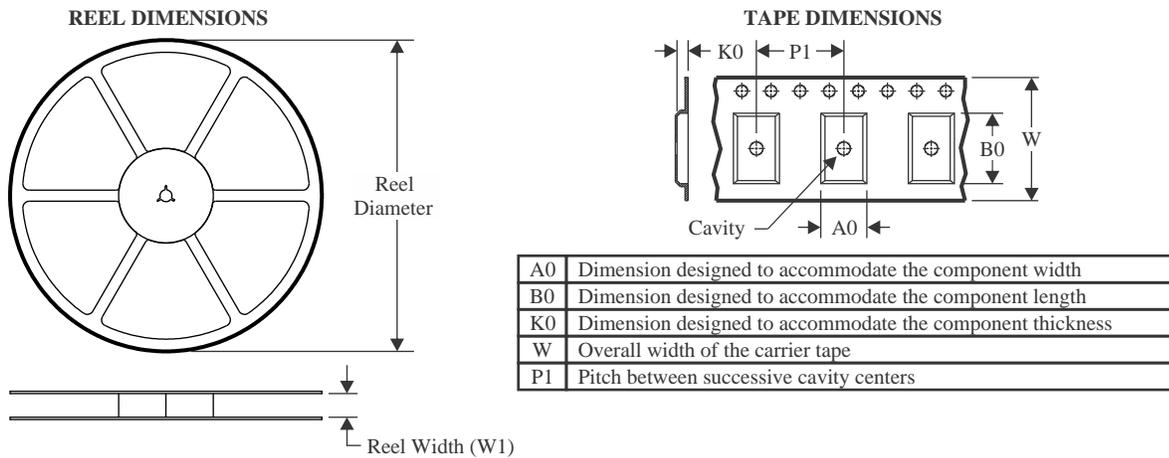
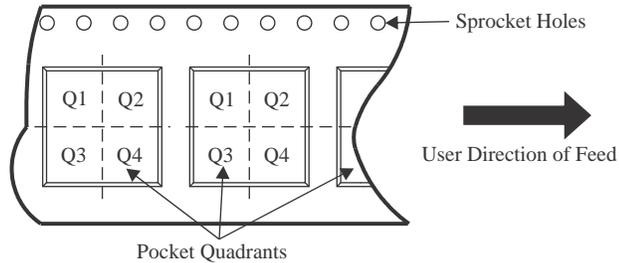
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC16373A :

- Enhanced Product: [SN74LVC16373A-EP](#)

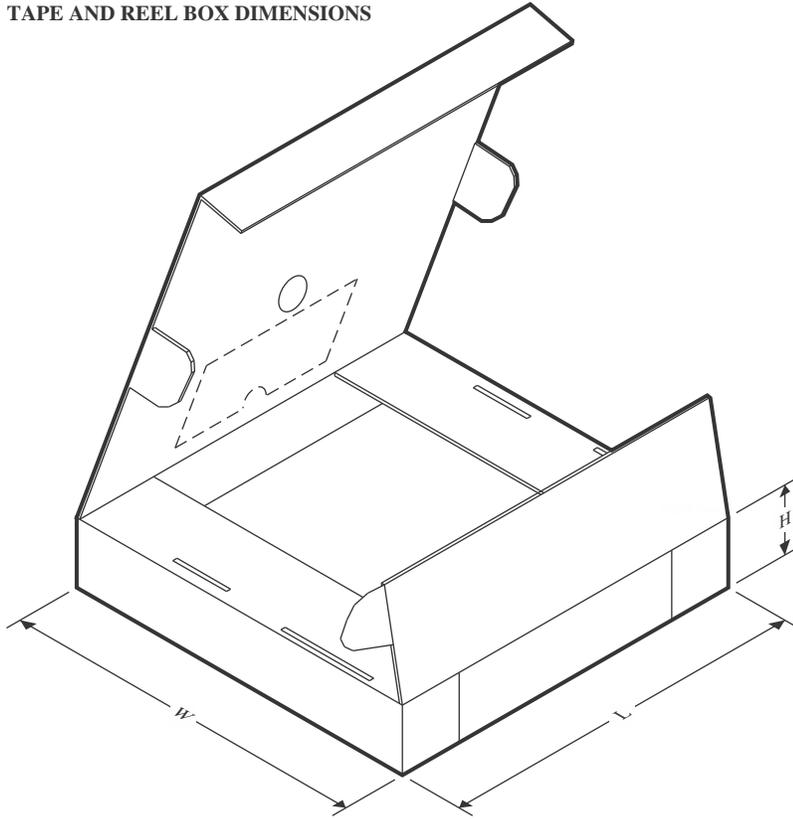
NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


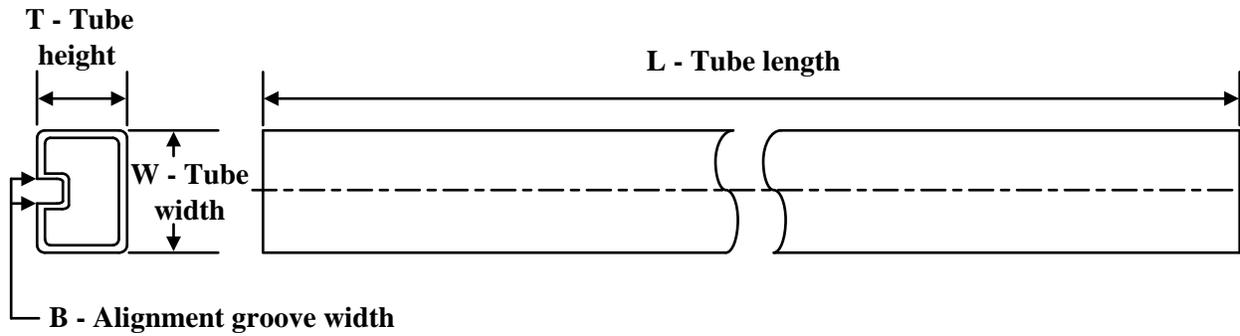
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVC16373ADGGR | TSSOP | DGG | 48 | 2000 | 330.0 | 24.4 | 8.6 | 13.0 | 1.8 | 12.0 | 24.0 | Q1 |
| SN74LVC16373ADGVR | TVSOP | DGV | 48 | 2000 | 330.0 | 16.4 | 7.1 | 10.2 | 1.6 | 12.0 | 16.0 | Q1 |
| SN74LVC16373ADLR | SSOP | DL | 48 | 1000 | 330.0 | 32.4 | 11.35 | 16.2 | 3.1 | 16.0 | 32.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVC16373ADGGR | TSSOP | DGG | 48 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74LVC16373ADGVR | TVSOP | DGV | 48 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LVC16373ADLR | SSOP | DL | 48 | 1000 | 367.0 | 367.0 | 55.0 |

TUBE


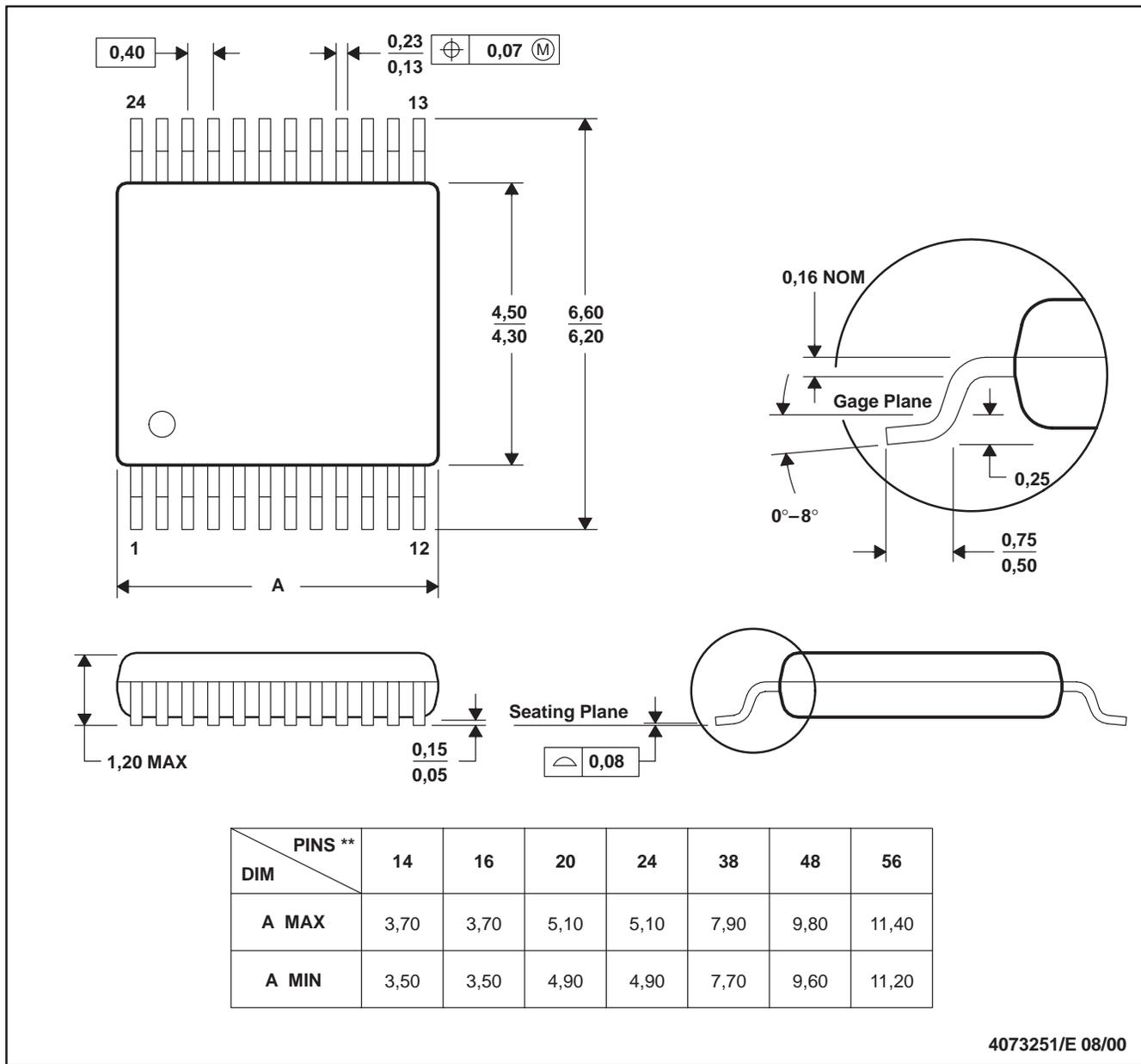
*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74LVC16373ADL | DL | SSOP | 48 | 25 | 473.7 | 14.24 | 5110 | 7.87 |
| SN74LVC16373ADLG4 | DL | SSOP | 48 | 25 | 473.7 | 14.24 | 5110 | 7.87 |

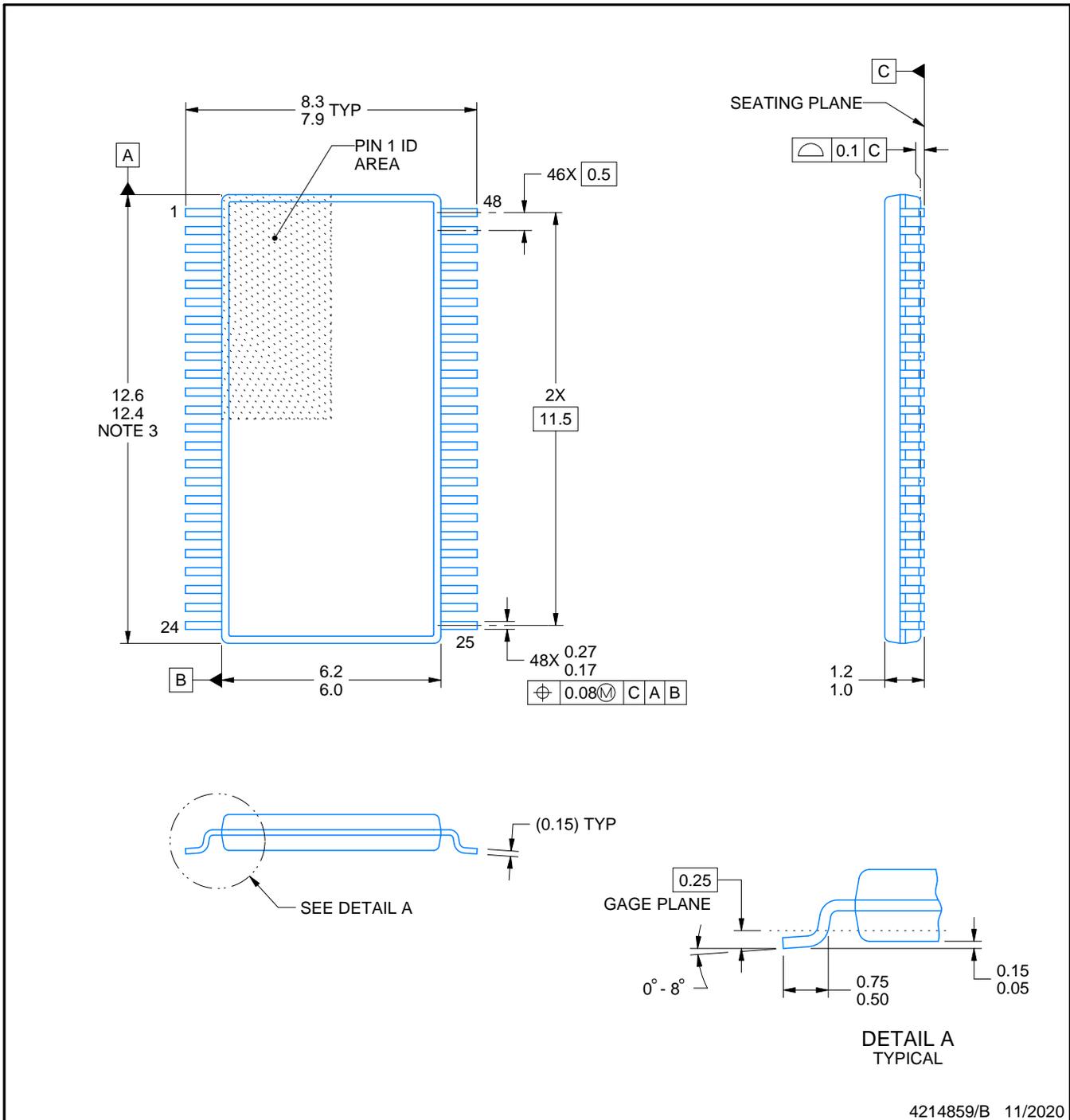
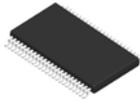
DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194



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NOTES:

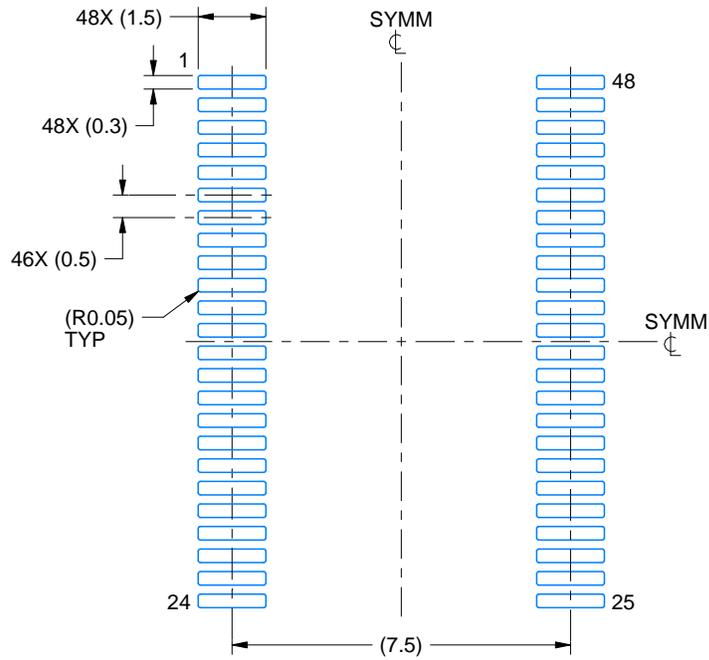
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

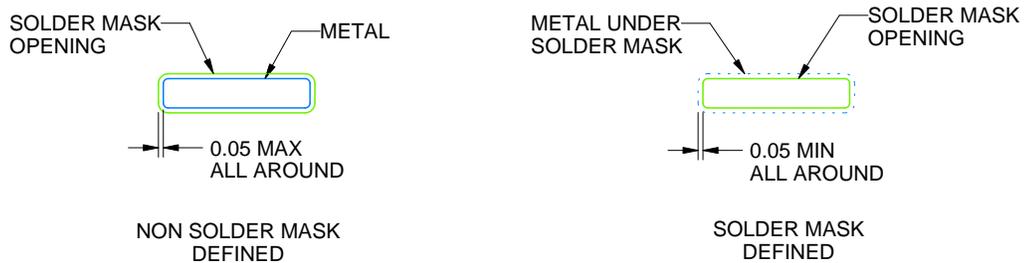
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

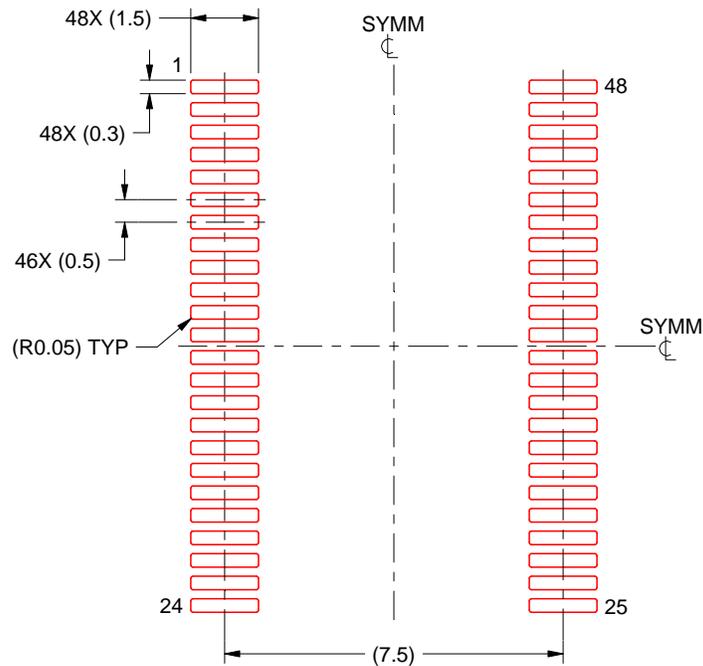
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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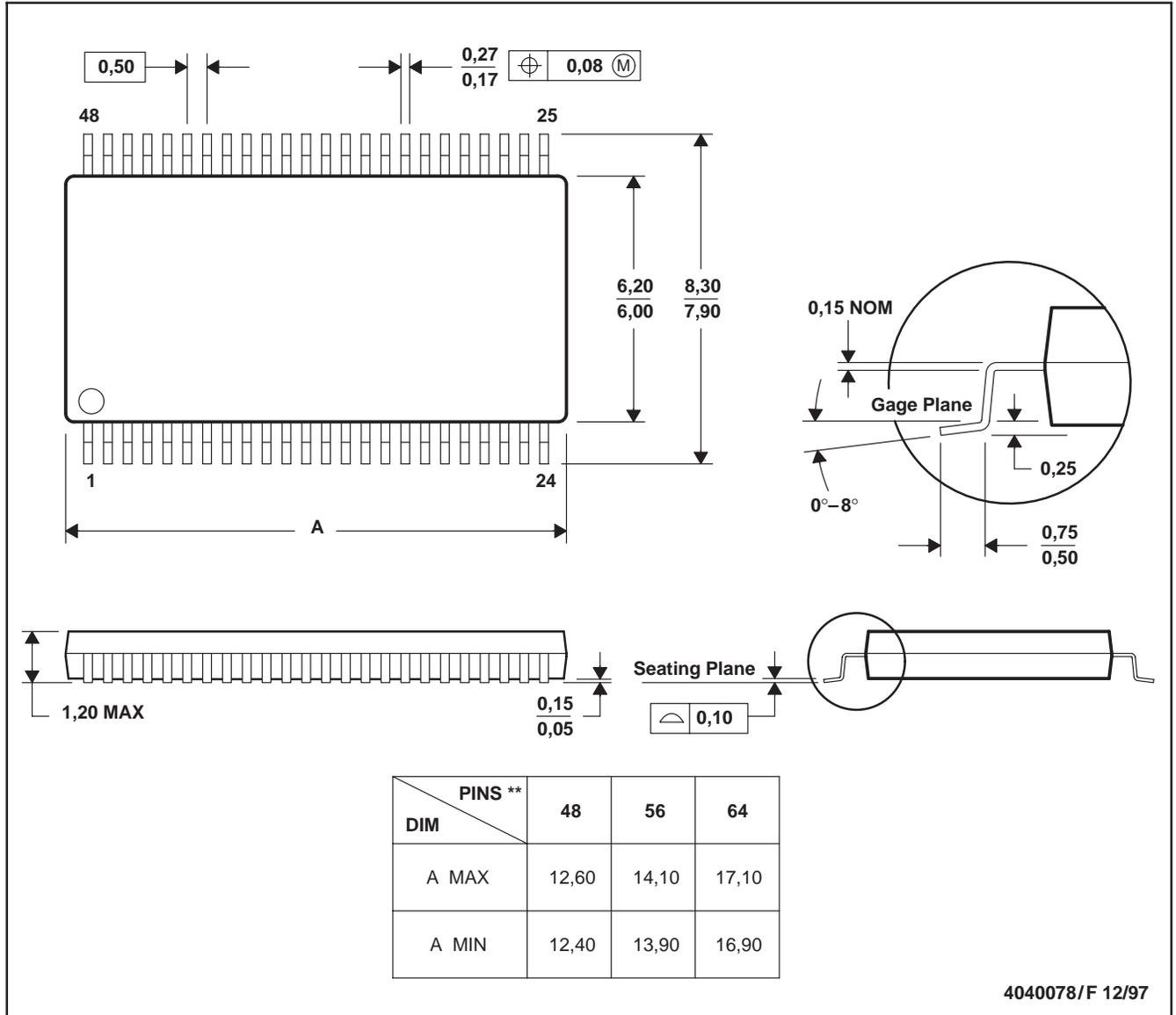
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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