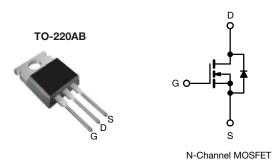
HALOGEN FREE



Power MOSFET



PRODUCT SUMMAI	RY	
V _{DS} (V)	10	00
$R_{DS(on)}(\Omega)$	V _{GS} = 10 V	0.16
Q _g max. (nC)	2	6
Q _{gs} (nC)	5.	.5
Q _{gd} (nC)	1	1
Configuration	Sin	gle

FEATURES

- Dynamic dV/dt rating
- Repetitive avalanche rated
- 175 °C operating temperature
- · Fast switching
- · Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free	IRF530PbF
Lead (Pb)-free and halogen-free	IRF530PbF-BE3

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise parameter		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V _{DS}	100		
Gate-source voltage			V _{GS}	± 20	- V
Ocation and distance and	V _{GS} at 10 V	T _C = 25 °C		14	A
Continuous drain current		$T_C = 25 ^{\circ}C$ $T_C = 100 ^{\circ}C$	I _D	10	
Pulsed drain current ^a		I _{DM}	56		
Linear derating factor			0.59	W/°C	
Single pulse avalanche energy ^b		E _{AS}	69	mJ	
Repetitive avalanche current a		I _{AR}	14	А	
Repetitive avalanche energy ^a			E _{AR}	8.8	mJ
Maximum power dissipation $T_C = 25 ^{\circ}C$		P_{D}	88	W	
Peak diode recovery dV/dt ^c		dV/dt	5.5	V/ns	
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +175		
Soldering recommendations (peak temperature) ^d For 10 s 300		300	°C		
Mounting toward	6-32 or M3 screw			10	lbf ⋅ in
Mounting torque				1.1	N⋅m

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. V_{DD} = 25 V, starting T_J = 25 °C, L = 528 μ H, R_g = 25 Ω , I_{AS} = 14 A (see fig. 12)
- c. $I_{SD} \le 14 \text{ A}$, $dI/dt \le 140 \text{ A/}\mu\text{s}$, $V_{DD} \le V_{DS}$, $T_J \le 175 \text{ °C}$
- d. 1.6 mm from case



Vishay Siliconix

THERMAL RESISTANCE RAT	INGS			
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R _{thJA}	-	62	
Case-to-sink, flat, greased surface	R _{thCS}	0.50	-	°C/W
Maximum junction-to-case (drain)	R _{thJC}	-	1.7	

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static						•	,
Drain-source breakdown voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		100	-	-	V
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	Reference t	to 25 °C, I _D = 1 mA	-	0.12	-	V/°C
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{C}$	_{GS} , I _D = 250 μA	2.0	-	4.0	V
Gate-source leakage	I _{GSS}	V _G	_S = ± 20 V	-	-	± 100	nA
Zana mata walka na dinaina muununt	,	V _{DS} = 100 V, V _{GS} = 0 V		-	-	25	,
Zero gate voltage drain current	I _{DSS}	V _{DS} = 80 V, V ₀	_{GS} = 0 V, T _J = 150 °C	-	-	250	μA
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 8.4 A ^b	-	-	0.16	Ω
Forward transconductance	9 _{fs}	V _{DS} = 50	O V, I _D = 8.4 A ^b	5.1	-	-	S
Dynamic							
Input capacitance	C _{iss}	$V_{GS} = 0 \text{ V}, V_{DS} = 25 \text{ V},$		-	670	-	pF
Output capacitance	C _{oss}			-	250	-	
Reverse transfer capacitance	C_{rss}	f = 1.0 I	MHz, see fig. 5	-	60	-	1
Total gate charge	Q_g			-	-	26	nC
Gate-source charge	Q_{gs}	V _{GS} = 10 V	I _D = 14 A, V _{DS} = 80 V, see fig. 6 and 13 ^b	-	-	5.5	
Gate-drain charge	Q_{gd}			-	-	11	
Turn-on delay time	t _{d(on)}			-	10	-	
Rise time	t _r	$V_{DD} = 50 \text{ V}, I_{D} = 14 \text{ A}$ $R_{g} = 12 \Omega, R_{D} = 3.6 \Omega, \text{ see fig. } 10^{\text{ b}}$		-	34	-	ns
Turn-off delay time	t _{d(off)}			-	23	-	
Fall time	t _f			-	24	-	
Gate input resistance	R_g	f = 1 MHz, open drain		1.0	-	4.7	Ω
Internal drain inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	الم
Internal source inductance	L _S			-	7.5	-	- nH
Drain-Source Body Diode Characteristic	cs						
Continuous source-drain diode current	I _S	showing the	MOSFET symbol showing the		-	14	Α
Pulsed diode forward current ^a	I _{SM}	integral reverse p - n junction diode		-	-	56	^
Body diode voltage	V_{SD}	T _J = 25 °C, I _S	_S = 14 A, V _{GS} = 0 V ^b	-	-	2.5	V
Body diode reverse recovery time	t _{rr}	T _ 2F °C	14 A dI/d+ = 100 A/c h	-	150	280	ns
Body diode reverse recovery charge	Q _{rr}	$T_J = 25 ^{\circ}\text{C}, I_F = 14 \text{A}, \text{dI/dt} = 100 \text{A/}\mu\text{s}^{\text{b}}$		-	0.85	1.7	μC
Forward turn-on time	t _{on}	Intrinsic turn	on time is negligible (turr	-on is do	minated b	y L _S and	L _D)

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Pulse width \leq 300 μ s; duty cycle \leq 2 %



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

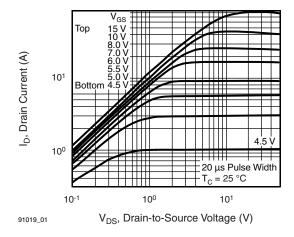


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

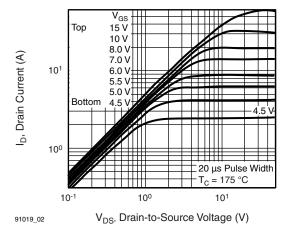


Fig. 2 - Typical Output Characteristics, $T_C = 175$ °C

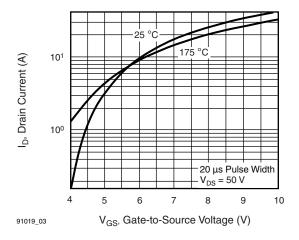


Fig. 3 - Typical Transfer Characteristics

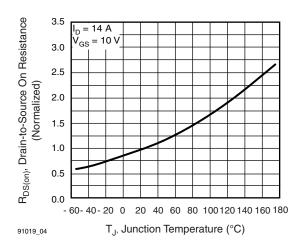


Fig. 4 - Normalized On-Resistance vs. Temperature

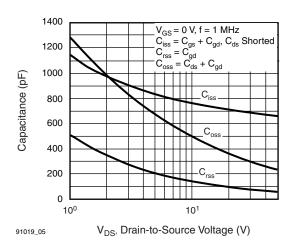


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

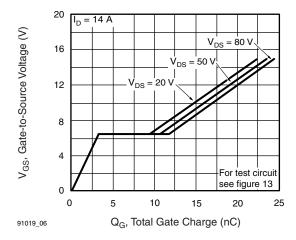


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



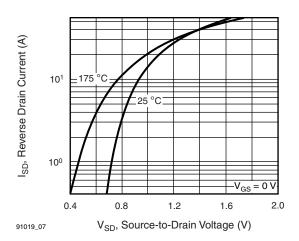


Fig. 7 - Typical Source-Drain Diode Forward Voltage

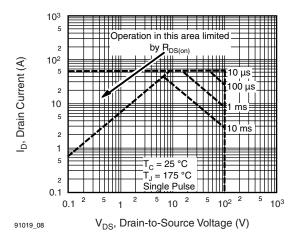


Fig. 8 - Maximum Safe Operating Area

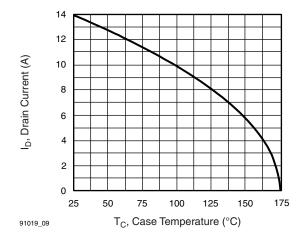


Fig. 9 - Maximum Drain Current vs. Case Temperature

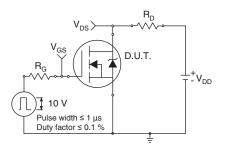


Fig. 10a - Switching Time Test Circuit

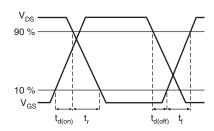


Fig. 10b - Switching Time Waveforms



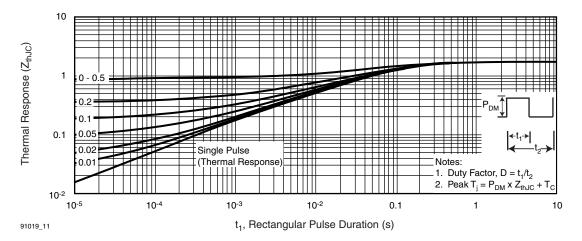


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

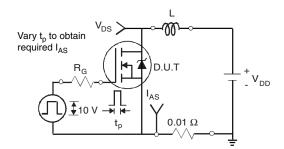


Fig. 12a - Unclamped Inductive Test Circuit

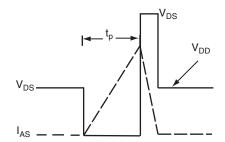


Fig. 12b - Unclamped Inductive Waveforms

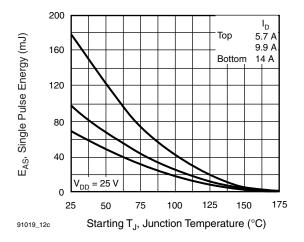


Fig. 12c - Maximum Avalanche Energy vs. Drain Current



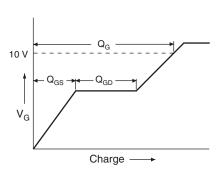


Fig. 13a - Basic Gate Charge Waveform

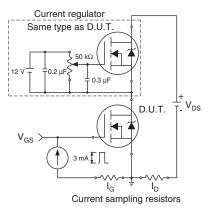
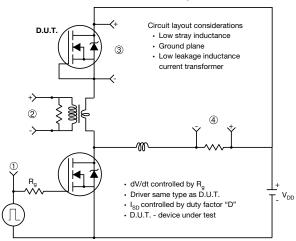


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



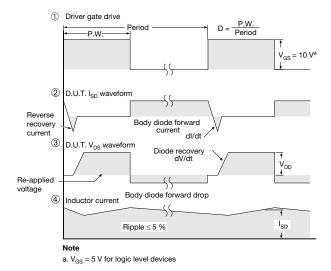
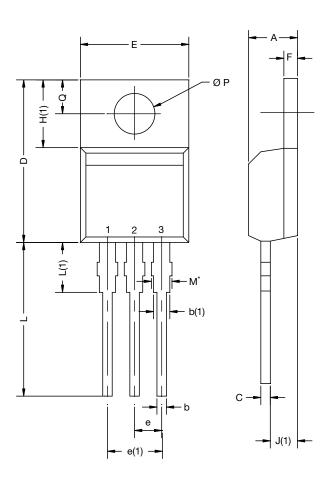


Fig. 14 - For N-Channel

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TO-220-1



DIM.	MILLIM	METERS	INC	HES
	MIN.	MAX.	MIN.	MAX.
Α	4.24	4.65	0.167	0.183
b	0.69	1.02	0.027	0.040
b(1)	1.14	1.78	0.045	0.070
С	0.36	0.61	0.014	0.024
D	14.33	15.85	0.564	0.624
Е	9.96	10.52	0.392	0.414
е	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.10	6.71	0.240	0.264
J(1)	2.41	2.92	0.095	0.115
L	13.36	14.40	0.526	0.567
L(1)	3.33	4.04	0.131	0.159
ØP	3.53	3.94	0.139	0.155
Q	2.54	3.00	0.100	0.118

Note

DWG: 6031

• $M^* = 0.052$ inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM



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